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A Four-Channel CMOS Front-End for Interference-Robust GNSS Receiver

Fang Han, Jian Gao, Xiaoran Li * and Zhiming Chen

School of Information and Electronics, Beijing Institute of Technology, Beijing 100081, China; hanfang@bit.edu.cn (F.H.); gj@bit.edu.cn (J.G.); czm@bit.edu.cn (Z.C.)

* Correspondence: xiaoran.li@bit.edu.cn; Tel.: +86-10-6891-8356

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Abstract: A four-channel receiver front-end is designed and implemented for interference- and jamming-robust global navigation satellite system (GNSS) in a 0.18-μm CMOS technology. The front-end consists of four identical RF-to-IF signal paths including low-noise amplifiers (LNAs), mixers and IF amplifiers. In addition, it also includes a phase-locked loop (PLL), which synthesizes the local oscillator (LO) signal, and a serial peripheral interface (SPI) for parameter adjustment. To improve the interference and jamming robustness, a novel linearity improvement technology and LO duty cycle adjustment method are applied in LNA and mixer design, respectively. The receiver achieves a gain of 40 dB, an input-referred third-order intercept point (IIP3) of −8 dBm and a jammer-to-signal power ratio (JSR) of 72 dB under 1.8-V and 3.3-V supply, while occupying a 4×5 mm^2 die area including the electrostatic discharge (ESD) I/O pads.

Keywords: CMOS; GNSS; wide-range derivative superposition; duty cycle adjustment

1. Introduction

Global navigation satellite system (GNSS) has been utilized to provide the position, velocity and/or time information in many applications such as aircraft navigation systems, automotive applications and portable devices [1,2]. With the increasing requirement in position accuracy, coverage and reliability, the front-end should be well designed to improve the performance of the GNSS receiver.

However, the main drawback for a conventional single-channel GNSS receiver is its poor performance in a multipath environment [3], which may cause frequency-selective fading. One promising way to solve this problem is to use multichannel structure. In addition, it may also benefit from nearby interference cancellation and digital beamforming algorithms to further suppress unwanted signals and increase the gain in the direction of the target satellites [4,5].

Moreover, the GNSS receiver is extremely vulnerable to various interference in the electromagnetic environment, which may exceed the allowable signal level of the internal module, thus causing the failure of positioning. Therefore, the gain is usually widely tunable in a traditional GNSS front-end so as to suppress unwanted interference and jamming as well as to achieve an optimal signal amplitude to enhance analog-to-digital converter (ADC) performance [6]. Two methods to control the gain of the front-end are generally utilized in the state-of-the-art works, one of which is to control through serial peripheral interface (SPI) manually [7], which is impractical in a commercial device, and the other is to tune by automatic gain control (AGC) through feedback network automatically [6,8]. However, the design procedure of AGC is rather complicated. Furthermore, although controlling the gain can maintain the receiver function under strong interference and jamming, the performance is severely sacrificed, causing inaccurate positioning analogous to terrible mobile communication under a harsh environment. In order to obtain precise positioning under such an environment, the design of a GNSS front-end with almost constant gain is proposed in [4] without sacrificing the performance when the

power of the signal is much lower than the interference or jammer, scaled by the jammer-to-signal power ratio (JSR). However, the JSR in [4] remains to be improved.

This manuscript describes the design and implementation of a four-channel GNSS front-end in a 0.18-μm standard CMOS process with a new linearity improvement technique applied in the low-noise amplifier (LNA) and with a novel local oscillator (LO) duty cycle adjustment method for a voltage-driven passive mixer in order to obtain better performance under strong in-band interference and jamming. Section 2 begins with describing the architecture and system design consideration of the front-end. Section 3 then presents the circuit implementations in detail. Experimental results are provided in Section 4, and the manuscript concludes with a summary in Section 5.

2. System Architecture

A detailed block diagram of the four-channel CMOS GNSS receiver is shown in Figure 1. Each channel of the RF front-end is composed of an off-chip LNA (modeling the GaAs LNA in the antenna), an off-chip Balun, an on-chip LNA, an off-chip image-rejection filter, a down-conversion mixer and an IF amplifier (IFA). Two-stage LNA, mixer, IFA of four channels and a PLL are integrated on a single chip. The received RF signal is first amplified by the two-stage LNA. After filtering by the image-rejection filter, the signal is down-converted to the IF frequency by the mixer and then amplified by the IFA. The output of the IFA is capable of driving an ADC with high input impedance. PLL provides four-channel LO signals for down-conversion. The bandgap reference (BGR) is applied for independent bias current and voltage required by each module of the system. Parameter adjustment is achieved by the SPI. An off-chip filter for image rejection of the RF band is employed for each channel, since an on-chip filter with such high image rejection ratio while meeting a bandwidth requirement can hardly be implemented for the specific application. The input impedance and output impedance are both matching to 100 Ω.

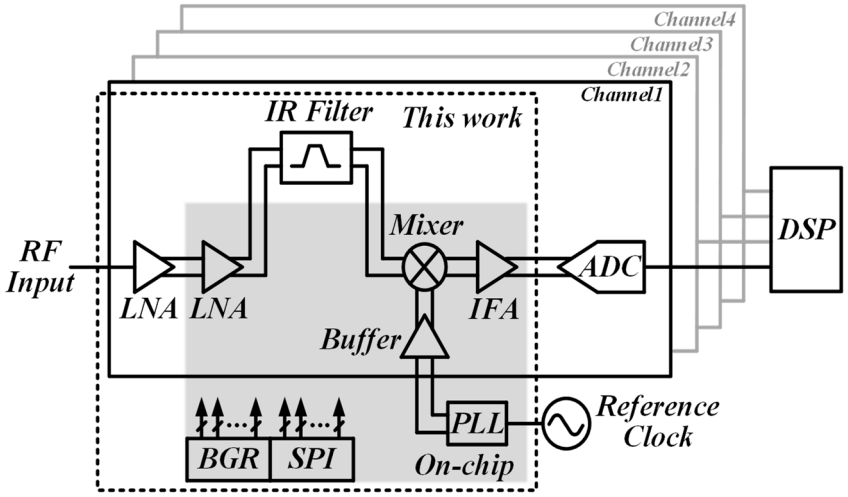

Figure 1. Diagram of the four-channel CMOS global navigation satellite system (GNSS) receiver.

Considering the limited transmitting power of the navigation satellite and the high propagation loss in space, the input power of the receiver is about −130 dBm [9–11]. The purpose of this work is to implement an RF front-end that can operate under a maximum in-band interference about −60 dBm, which corresponds to a JSR of 70 dB. Since the final output power of the receiver front-end has upper limits, when a strong interference signal enters the receiver, excessive gain will result in output power saturation. Besides, the extra high-order terms of the interference generated by the nonlinearity of the RF front-end further deteriorate the receiver performance. Thus, these extra higher-order terms should not be greater than the equivalent output noise floor of the RF front-end.

Due to the high dynamic range performance and the requirement to withstand strong interference, the receiver needs to achieve a low noise figure and a high output third-order intermodulation distortion (IMD3) with limited gain. In order to make full use of the dynamic range of ADC when strong interference exists, it is desired to have the ADC operating at full scale, which requires the output signal range of the IFA to be as large as possible. The corresponding output third-order intercept point (OIP3) should be considered under the condition of high output power.

3. Circuit Implementations

3.1. LNA

A two-stage LNA with a novel linearity improving method is proposed in this design. The relation between drain current and gate source voltage of a transistor can be written as $i_d = g_1 v_{gs} + g_2 {v_{gs}}^2 + g_3 {v_{gs}}^3$, where g_1 and g_n $(n > 1)$ stand for the transconductance and the nth order nonlinear coefficient, respectively. The principle of derivative superposition (DS) technology is to place two or more transistors in parallel and cancel the third-order derivation with each other to improve the linearity.

Conventional linearization methods are usually applied to improve the small-signal linearity performance. Figure 2a shows the basic schematic of the conventional derivative superposition technology [12] with two transistors in parallel, one of which works in weak-inversion region for g_3 compensation. However, the total g_3 will only approach or equal zero in a narrow region. When the input power increases, the amplitude of the signal applied to the gates of M_{main} and M_{C} will exceed g_3 compensation region, which means that large-signal nonlinearity may not be improved.

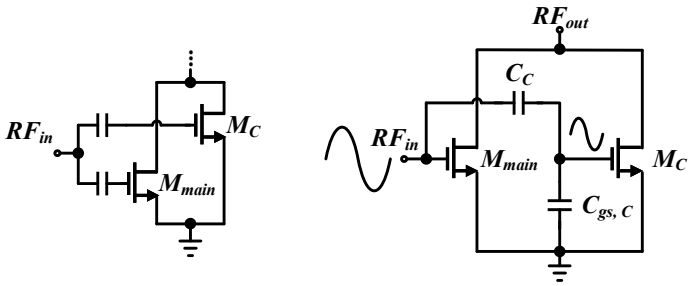

Figure 2. The derivative superposition technology with two transistors in parallel. (**a**) Conventional. (**b**) Proposed.

In order to make LNA maintain good linearity under high input power, and allow strong interference signal to enter LNA, the conventional method of DS cancellation is optimized. Two regions of g_3 curves are chosen, instead of only positive and negative peaks, so that the g_3 curve can off-set to zero within a wide range. To extend the g_3 cancellation region, a capacitor C_{C} is added to adjust the slope of g_3 curve of the compensation transistor M_{C}, as shown in Figure 2b. By carefully optimizing C_{C}, the IMD3 will dramatically increase [13].

The schematic of the proposed LNA is shown in Figure 3. Differential architecture is applied for better rejection of on-chip interference [14]. The main consideration is noise performance for the first stage and linearity for the second stage for a typical two-stage LNA. Therefore, the first stage uses an inductively degenerated cascode stage with fixed gain and input matching performed on-chip. The second stage uses a cascode amplifier with the wide-range DS technology to further improve the linearity.

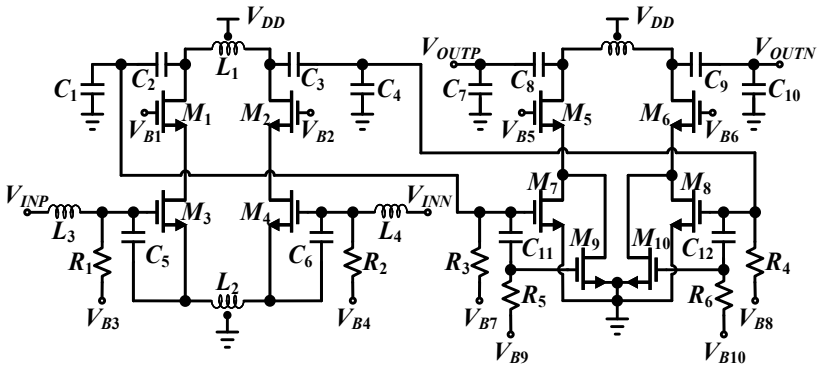

Figure 3. Circuit-level description of the designed two-stage low-noise amplifier (LNA).

3.2. Mixer

As shown in Figure 4a, a voltage-mode double-balanced passive mixer is applied for better linearity, power consumption and chip size, considering the requirements of GNSS front-end [15]. In addition, there is no DC current through the switches so that there is no $1/f$ noise [14]. The LNA output is coupled to the RF ports of the mixer through a capacitor, and each pair of the four transistors serves the function of connecting IF ports to the RF ports. M_1 and M_4 work together and are controlled by the LO signal generated from the PLL, while M_2 and M_3 are controlled by the inverse of the LO signal. A new LO waveform optimization method for a voltage-driven passive mixer is proposed.

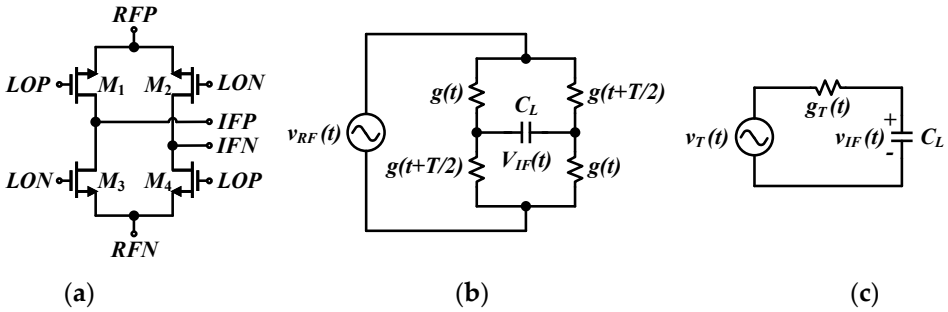

Figure 4. Double-balanced passive mixer. (**a**) Schematic. (**b**) Time-varying conductance equivalent circuit. (**c**) Thevenin equivalent circuit.

A brief analysis of the double-balanced passive mixer using time-varying conductance equivalent circuit and Thevenin equivalent circuit shown in Figure 4 is illustrated in [14]. The Thevenin equivalent voltage $v_T(t)$ and Thevenin equivalent impedance $g_T(t)$ can be derived using Equations (1) and (2):

$$v_T(t) = \frac{g(t) - g(t - T_{LO}/2)}{g(t) + g(t - T_{LO}/2)} v_{rf}(t) = m(t) v_{rf}(t), \tag{1}$$

$$g_T(t) = \frac{g(t) + g(t - T_{LO}/2)}{2}, \tag{2}$$

where $m(t)$ represents the mixing function, $v_{rf}(t)$ represents the RF port's voltage, T_{LO} is the time period of LO signal. Thus, the IF output can be expressed as:

$$v_{if}(t) = \frac{Z_L g_T(t)}{Z_L g_T(t) + 1} m(t) v_{rf}(t), \tag{3}$$

The following qualitative analysis in [10] is based on the assumption that $\overline{g_T} Z_L << 1$, which is typical for a current-driven passive mixer, where $\overline{g_T}$ is the average transconductance in one cycle

of $g_T(t)$. In contrast, for a voltage-driven passive mixer, when the load capacitance is less than 1pF, $\overline{g_T} Z_L >> 1$ is valid. Under such circumstance, Equation (3) can be simplifed as:

$$v_{if}(t) = m(t) v_{rf}(t), \tag{4}$$

where $m(t)$ can be considered as the conversion gain.

According to the relationship between the overlapping-point voltage V_{ip} of differential LO waveform and transistor threshold voltage V_{th}, $g(t)$ and $g_T(t)$ are shown in Figure 5a. $g_T(t)$ is greater than or equal to zero in any period, especially when $V_{ip} > V_{th}$, which will have a higher value. At the same time, a higher $g(t)$ can be achieved by increasing the *W*/*L* ratio of the transistor in order to obtain a larger and more stable $g_T(t)$.

The constant $\gamma = (V_{th} - V_{ip})/A_{LO}$ is introduced here to represent DC bias of the mixer, where $V_{ip} = V_{LO} - v_{rf}$, and A_{LO} is the LO amplitude. Under different overlapping-point voltage, there is a relationship between $m(t)$ and γ as shown in Figure 5b.

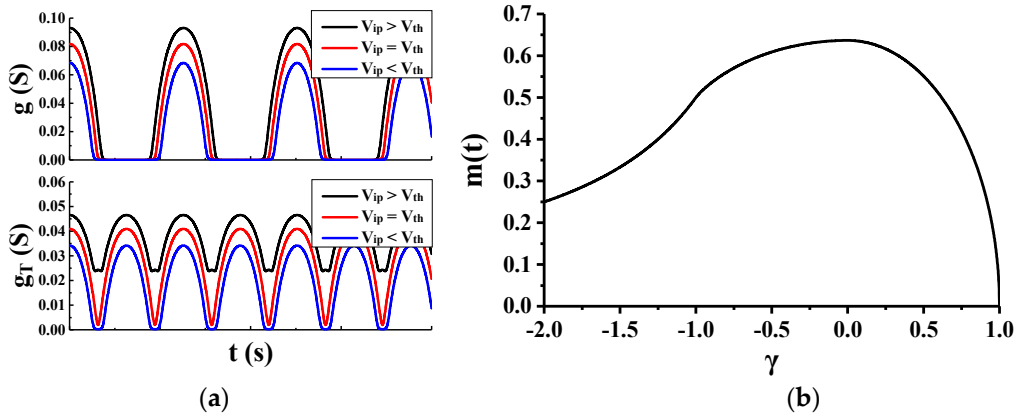

Figure 5. Analysis of double-balanced passive mixer. (**a**) Transistor conductance under different V_{ip}. (**b**) Relationship between $m(t)$ and γ.

For a square-wave LO, if the amplitude is large enough, regardless of the duty cycle, the mixer gain will not change with the amplitude of input signal. Therefore, the linearity of the passive mixer driven by square-wave LO is ideal. However, the amplitude of the input RF signal can no longer be ignored for a sinusoidal-wave LO. The mixer may switch between three working states: overlapping-point voltage is greater than, equal to or less than the transistor threshold voltage. Taylor series expansion can be further carried out for $m(t)$ under different regions of γ, and the first and third order coefficients as well as their ratio are calculated. When $-1 \leq \gamma < 0$, the passive mixer will get the best third-order intercept point. Since $\gamma = (V_{th} - V_{ip})/A_{LO}$, increasing the LO amplitude can weaken the change of γ with respect to v_{rf} and improve the gain stability, which indicates better linearity. On the other hand, by properly setting the overlapping-point voltage V_{ip}, γ can be kept in the range of $-1 \leq \gamma < 0$ under any voltage range of RF signal, so as to improve the linearity of mixer. Therefore, the proposed LO driving circuit is able to output full-scale signal with large duty cycle to minimize the change of the passive mixer gain.

3.3. IFA

As shown in Figure 1, the differential output of the mixer drives the IFA directly. As the distance between the satellite and receiver is far enough, a wide-range variable gain amplifier is not necessary here because the movement of signal source may have little influence on the signal power. As the last stage of the front-end, linearity is indispensable in the IFA design because of its significant influence on the linearity performance of the whole system.

The IFA consists of two stages, as shown in Figure 6. The input stage uses a transconductance amplifier to convert voltage signal to current signal, as shown in Figure 7. Because the impedance of PMOS transistor is much higher than an on-chip *LC* tank operating at intermediate frequency, M_5 and M_6 are used here as the load so that all the output current is fed into the second stage in order to improve the linearity performance [16]. R_9 and R_{10} are utilized as source degeneration so as to further improve linearity.

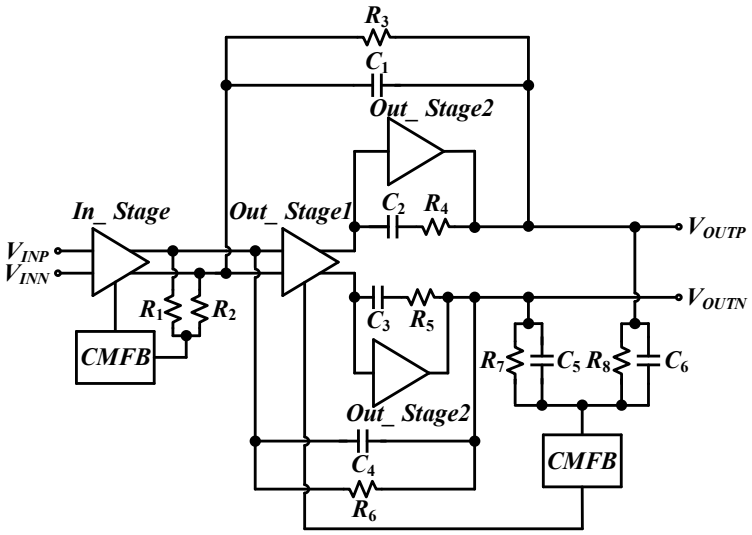

Figure 6. Architecture of the proposed IF amplifier (IFA).

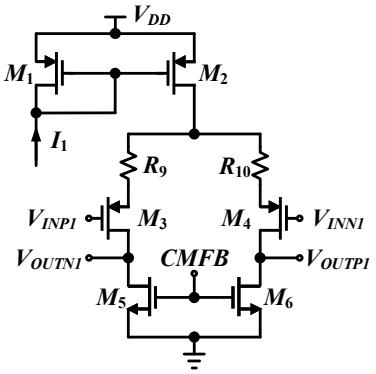

Figure 7. Transconductance amplifier in the input stage.

The output stage, as shown in Figure 6, is a two-stage amplifier with *RC* feedback, which consists of a traditional differential amplifier and a class-A push-pull amplifier to enhance linearity performance, as shown in Figure 8. The output of the IFA is capable to drive an ADC with high input impedance.

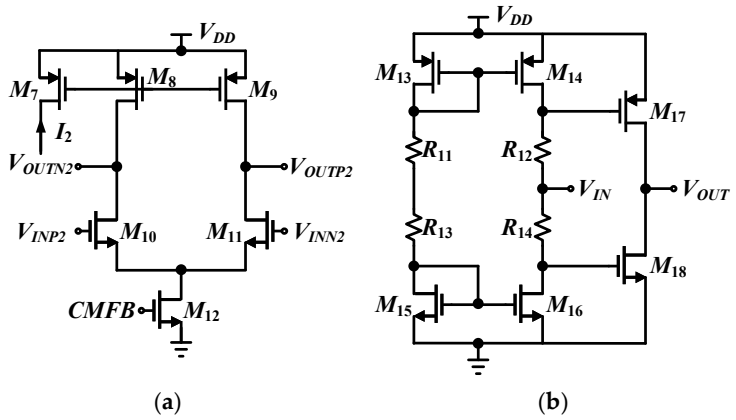

Figure 8. Output stage of IFA. (**a**) The traditional differential amplifier of the first stage. (**b**) The class-A push–pull amplifier of the second stage.

3.4. PLL

An integer-N PLL is implemented in the front-end in order to generate the LO signals for 1.2 GHz frequency band as shown in Figure 9, which includes a phase-frequency detector (PFD), a charge pump, a second-order loop filter, an *LC* voltage-controlled oscillator (VCO) with current-mode logic (CML) buffer, a divider chain with a differential to single-ended converter (D2C), a single-modulus counter divider and a multimodulus pulse-swallow divider. The reference frequency is 2 MHz. The loop bandwidth is designed to be 100 kHz.

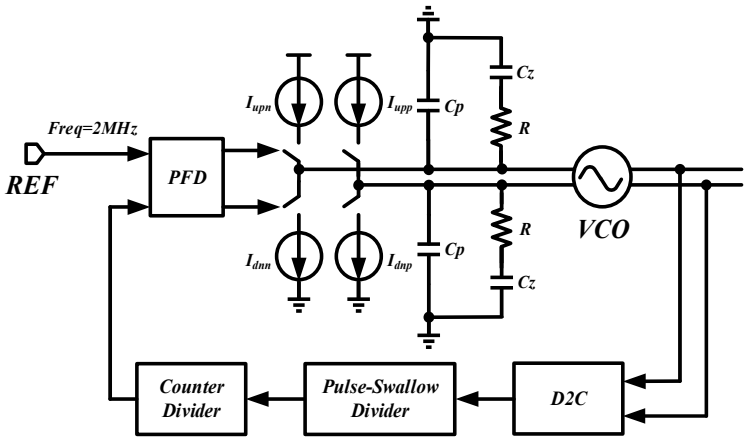

Figure 9. Integer-N PLL for local oscillator (LO) signal generation.

4. Measurement Results

The four-channel GNSS front-end is fabricated in a 0.18-µm CMOS technology, and the die microphotograph is shown in Figure 10. The total chip occupies an area of 4×5 mm^2, including pads.

The chip has been packaged using a standard 80-pin quad-flat no-leads (QFN) package and mounted on a test board. The RF input is matched with S_{11} better than −16 dB. The measured phase noise using spectrum analyzer is shown in Figure 11, which is about −126.26 dBc/Hz at 1 MHz frequency offset.

The measured maximum voltage gain of the front-end is about 40 dB with 0.14 dB gain ripple for four channels as shown in Figure 12. The linearity of the front-end is measured with a two-tone IP3 test as shown in Figure 13. The input-referred IIP3 is better than −8 dBm.

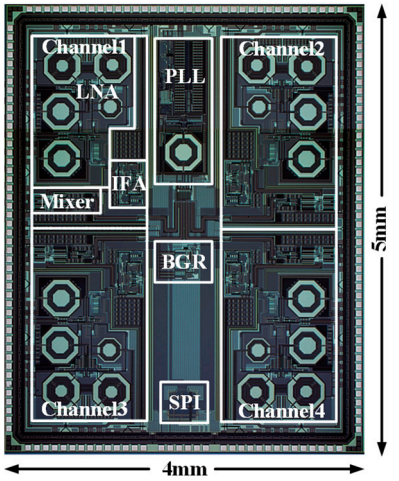

Figure 10. Microphotograph of the four-channel GNSS front-end.

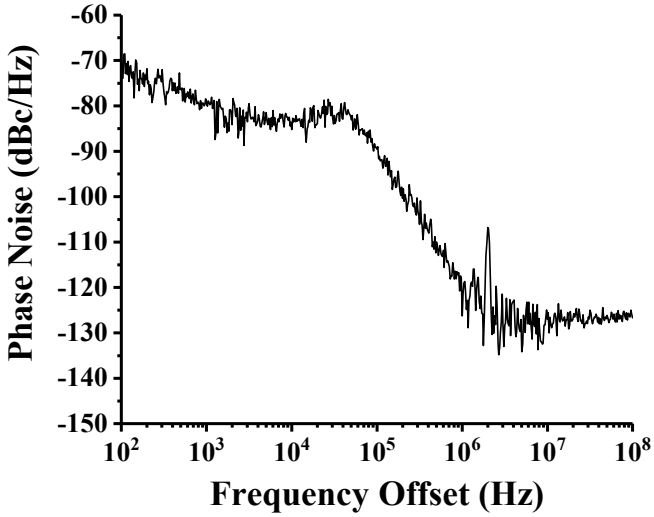

Figure 11. Measured phase noise of the on-chip PLL using spectrum analyzer.

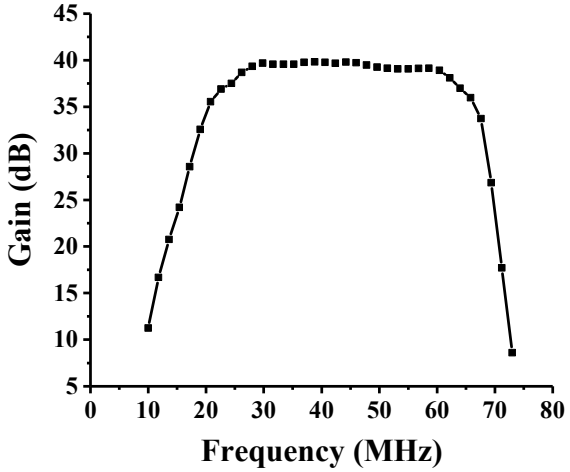

Figure 12. Measured gain of the GNSS receiver.

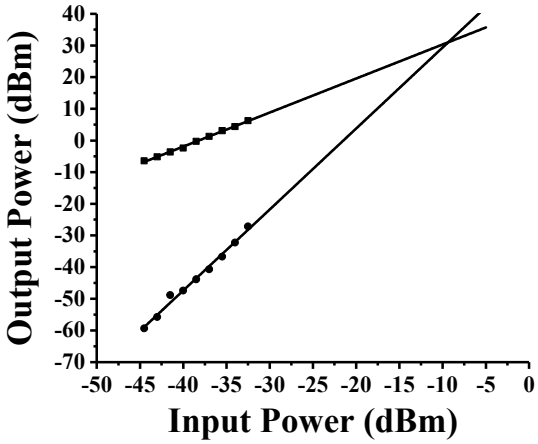

Figure 13. Measured IP3 results using two-tone test.

An off-chip LNA with a gain of 18 dB is applied to model the GaAs LNA in the antenna. The input noise floor can be calculated as −100 dBm using *kTB* approximately. Since the total gain of the off-chip LNA and front-end is 58 dB, the noise floor before ADC is −42 dBm. As shown in Figure 12, the third-order intermodulation is 42 dBc when the output is 0 dBm to make sure that the third-order harmonic of interference is lower than noise floor. The in-band interference before ADC should be 0 dBm, resulting in a −58 dBm interference for the whole receiver. Generally, the input power of the receiver is about −130 dBm. Thus, the jammer-to-signal power ratio (JSR) is derived as 72 dB. Table 1 summarizes the performances of the proposed GNSS receiver and compares it with the state-of-the-art designs.

Table 1. Comparison with previous works.

	This Work	**[4]**	**[6]**	**[17]**		**[18]**	
Process (nm)	180	180	180	130		130	
Number of Channels	4	4	2	1		1	
Frequency (GHz)	1.2	1.57	1.2/1.57	1.57		1.575	
Supply (V)	1.8/3.3	1.8/3.3	1.8	1.2	0.25	0.3	0.4
Gain (dB)	40 *	83	110 *	36 *	41.8	42.2	42.5
P_{-1dB} (dBm)	−18	−73.5	−42/−39	−31	−48	−47	−45.7
IIP3 (dBm)	−8	–	–	−19	−35.8	−35.2	−34
Phase noise at 1 MHz (dBc/Hz)	−126.26	−107	−122/−124	−104	−112.4	−112.5	−113.8
S_{11} (dB)	−16	–	−13/−12	<−10		<−10	
JSR (dB)	72	45	–	–		–	
Area (mm^2)	20	25	2.4	1.5		5.76	

* Voltage gain.

5. Conclusions

A four-channel interference-robust GNSS front-end is presented in this manuscript. The proposed GNSS front-end is implemented in a 0.18-µm CMOS technology with the chip area of 4×5 mm^2. A new wide-range derivative superposition technique is proposed for better LNA linearity—An LO waveform design method is applied to the voltage-driven passive mixer in order to further improve the linearity performance of the front-end. The proposed RF front-end achieves a gain of 40 dB, an IIP3 better than −8 dBm, an input S-parameter (S_{11}) better than −16 dB and a phase noise of the on-chip PLL of about −126.26 dBc/Hz at 1 MHz frequency offset from a 1.8/3.3 V power supply. The jammer-to-signal power ratio is up to 72 dB. The proposed front-end can work under strong interference and jamming environments and can be utilized to make a complete GNSS receiver system combined with ADC and digital signal processor (DSP), which can be integrated into portable and wearable devices for satellite navigation.

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