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Feasibility Study of Interleaving Approach for Quasi-Z-Source Inverter

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Abstract: This paper presents a comprehensive feasibility study of an interleaving approach for a quasi-Z-source inverter. The state-of-the-art approach revealed that an interleaving approach is often used to improve the efficiency and power density that can overcome the problem of oversized passive elements of quasi-Z-source-based converters. The focus is on the application of the interleaving approach in terms of the comparison of several important parameters of a quasi-Z-source inverter. Our analysis includes losses, capacitor and inductor sizes, as well as semiconductor costs. The theoretical comparison is based on the quasi-Z-source inverter model and the losses model. Simulation and experimental verification of theoretical statements are provided. It was found that a 40% reduction of inductor volume, along with 15–20% of efficiency improvements, are achievable. The results are discussed in the conclusion.

Keywords: impedance-source inverter; shoot-through; dc-dc converter; dc-ac converter

1. Introduction

The Google Little Box Challenge (GLBC) revealed extremely high interest in the topic of high-power density inverters for photovoltaic (PV) applications. It was demonstrated that the extremely high-power density of a power electronics converter is achievable [1,2]. The finalists demonstrated a similar approach using an interleaved full-bridge inverter, wide bandgap (WBG) semiconductors and an active power decoupling circuit [3–5]. However, this competition was intended for a converter designed with a narrow input voltage regulation range, whereas string solar inverters commonly have a wide input voltage regulation range. Most of the market solutions have two stages of energy conversion. Advances in WBG materials and their role in power electronics manufacturing have been phenomenal in the last decade. Large-scale manufacturing is also bringing overall costs down, and improving performance handling capability [6].

A Z-source inverter (ZSI) was introduced in 2003 [7] as a single-stage alternative. It was claimed that the converter overcomes the conceptual and theoretical barriers and limitations of the traditional voltage source inverter (VSI) and current source inverter (CSI). ZSIs utilize the shoot-through (ST) cross-conduction states to boost the input dc-voltage by switching on both the top and bottom switches of at least one inverter leg. These inverters can provide maximum power point tracking (MPPT) without any extra dc–dc converter. Their application in various fields is discussed in many papers [8–17].

At the same time, several papers [18–21] have disclosed the problems of Z-source networks. In particular, passive component size and overall efficiency are considered a bottleneck in Z-source-based solutions.

Our goal is to study the feasibility of the interleaving approach for a Z-source-based inverter with WBG semiconductors. Our specific aim is to find out if it is reasonable to use approaches applied in the GLBC competition for a Z-source-based inverter.

2. Description of a Case Study System with a Quasi-Z-Source Inverter

The solution in Figure 1 consists of an interleaved 2-level quasi-Z-source inverter (qZSI). Each part includes the quasi-Z-source (qZS) network represented by L_1 , D_1 , C_1 , L_2 and C_2 for the first branch and L_3 , D_2 , C_3 , L_4 and C_4 for the second branch. It also has full-SiC 2-level full-bridge inverters represented by switches S_1 – S_8 ; the output filter L_{F1} – L_{F4} ; C_F ; and L_{g1} and L_{g2} feeding the load or connected to the grid.



Figure 1. The 2-level interleaved quasi-z-source inverter (qZSI).

The 2-level qZSI is described in [22] as a three-phase PV inverter, while the 2-level solution is compared with the 3-level NPC for a single-phase application in [23]. According to the study, a full-SiC 2-level qZSI solution has a clear advantage over the 3-level NPC qZSI solution with Si MOSFETs, in terms of higher efficiency, along with the lower volume of the heatsink, while the volume of passive elements remains the same.

The interleaved 2-level qZSI for a single-phase PV application and the control approaches, including different modulation techniques, are discussed in detail in [23–27]. Our work is devoted to the feasibility study of the interleaving approach in terms of size, efficiency and the overall cost of the converter.

The parameters of the reference system are given in Table 1. The input voltage range is considered from 200 V to 600 V, and the converter was assumed to operate with a rated input current of up to 5 A. In this case, low-frequency (LF) power ripples are mitigated by means of the conventional decoupling capacitor C_{PV} . Many other decoupling techniques are available for this purpose [28–32]. The active power decoupling circuits are relevant for consideration in terms of power density improvements, but are still not effective in terms of the cost. A decoupling capacitor of up to 10 mF can provide the input current ripple of about 10–15% for string solar inverters, which in turn results in the PV panel's voltage ripple being no higher than 3–4% [33]. These numbers are sufficient to yield an MPPT efficiency of 99%, which is the industrial standard.

System Parameters	Values
Nominal power P _{nom} , W	1800
Nominal input voltage V _{nom} , V	200-600
Nominal input current Inom, A	5
Output RMS voltage V _{load} , V	230
Output current THD, %	<3
Input current ripple ΔI , %	<10

 Table 1. System parameters.

3. Component Selection and Comparison

In order to provide correct comparison, the passive and active components were selected according to the predefined parameters. The passive element values of the qZS network for both cases were calculated to provide the desired current and voltage ripple. Usually, the design procedure takes into account the high-frequency (HF) and LF ripple analysis [12]. In this case, the LF ripple is assumed to be eliminated by the input decoupling capacitor C_{PV} . At the same time, the value of the decoupling capacitor is considered to be the same for a single and an interleaved qZSI, and it has no direct impact on the interleaving study. In conclusion, it is required to select the passive components for proper HF ripple mitigation. In the case of a single qZSI, the inductors were selected for the continuous current mode in the basic operating points, which is taken into account in the following equation

$$L_1 = L_2 > = \frac{2 * V^{2_{\text{OUT}}} \cdot T_S}{K_L \cdot P} \cdot \frac{V_{\text{IN}} \left(V_{C_{\text{REF}}} - V_{\text{IN}} \right)}{V_{C_{\text{REF}}} \cdot \left(2 \cdot V_{C_{\text{REF}}} - V_{\text{IN}} \right)}$$
(1)

where L_{1, L_2} are the values of the qZS network inductance, V_{OUT} is the output voltage, V_{IN} is the input voltage, T_S is the switching period, K_L is the assumed HF ripple of the input current, P is the output power and V_{C_REF} is the reference capacitor voltage. A similar approach was applied for capacitor estimation

$$C_1 = \frac{P \cdot T_S}{2 \cdot K_{C1} \cdot V^{2_{OUT}}} \cdot \frac{V^{2_{C_{REF}}}}{V_{IN} \cdot \left(2 \cdot V_{C_{REF}} - V_{IN}\right)}$$
(2)

$$C_2 = \frac{P \cdot T_S}{2 \cdot K_{C2} \cdot V^{2_{OUT}}} \cdot \frac{V_{PL} \cdot \left(V_{C_{REF}} - V_{IN}\right)}{V_{IN} \cdot \left(2 \cdot V_{C_{REF}} - V_{IN}\right)}$$
(3)

where C_1 , C_2 are the values of the qZS network capacitors, and K_{C1} , K_{C2} are an assumed HF ripple of the capacitor voltage. Passive component values must be large enough to provide the demanded output current quality, converter controllability and low input current ripple in PV applications. Table 2 shows the values selected for our simulation and experimental verification.

Table 2. Passive elements selection.

	Interleaved qZSI	Single qZSI
HF current ripple, %	70	35
qZS inductance L_1 , L_2 , mH	0.9	0.9
Maximum current across inductance, A	3.4	5.9
Voltage ripple across C_1 , %	<1	<1
qZS capacitor C_1 , mF	0.68	1.36
Maximum voltage across capacitor C_1 , V	500	
Voltage ripple across C_2 , %	<1	<1
qZS capacitor C_2 , mF	1.5	3
Maximum voltage across capacitor C_2 , V	250	
Switching frequency, kHz	60	

As can be seen in the interleaved solution, the values of the inductances are the same, but the relative current ripple is increasing. This is explained by an average current decreasing by splitting the current between the two qZS channels. In this case, capacitor values can be selected twice smaller due to the power flow splitting.

The next task is to select proper active components. Splitting power flow between the two channels with the same resistance may reduce conduction losses up to two times. As a result, interleaving is an approach that enables converter design with extremely high efficiency and power density by means of N channel utilization [34,35]. Evidently, however, this leads to an increase in cost.

Our goal is to specify whether it is possible to design a cost-effective solution using the interleaving approach for the qZSI. Table 3 presents the selected active components and their main parameters. The distributed price was selected as a reference.

	Interleaved qZSI	Single qZSI	
Transistors			
Туре	C2M0160120D	C2M0080120D	
Blocking voltage, V	120	1200	
Total Gate Charge, nC	34	62	
Diode reverse recovery charge, nC	192	105	
Turn-on delay time, ns	9	11	
Rise time, ns	11	20	
Turn-off time delay, ns	16	23	
Fall time, ns	10	19	
Rds, mOhms	160	80	
Cost, Euro	7.5	15	
Diodes			
Туре	C4D05120A	C4D10120A	
Blocking voltage, V	1200		
Forward voltage drop, V	1.9	2.2	
Reverse recovery charge, nC	23	45	
Diode reverse recovery time	-	-	
Current, A	5	10	
Cost, Euro	5.04	10.13	

Table 3. Active elements selection.

As can be seen, all the semiconductors have the same blocking voltage. The nominal rated current is different, but the overall cost of active components is the same. In particular, C2M01612D is twice cheaper than C2M0080120D, but has twice larger drain-source resistance. This means that overall conduction losses in the transistors are expected to be the same.

At the same time, attention should be paid to the different dynamic characteristics. Table 2 shows that semiconductors with a smaller current rate have significantly better dynamic characteristics.

Figure 2 shows a comparative diagram for the estimation of the pros and cons of the interleaving approach for the qZSI. The method of comparison is described in several papers [18,21]; here, we used a modified version. Five parameters were used for comparison: weighted summarized losses of transistors T_L , weighted summarized losses of diodes D_L , weighted inductors volume Vol_L , weighted capacitors volume Vol_C and the weighted cost of semiconductors.

Summarized losses of the single transistor can be estimated by a simplified equation [36,37]

$$P_{\text{MOSFET}} = f \cdot \left(\frac{t_{\text{don}} + t_r + t_{\text{doff}} + t_f}{2} I_{\text{DS}} V_{\text{DS}} + \frac{5}{4} Q_{\text{rr}} V_{\text{DS}}\right) + I_{\text{RMS}}^2 \cdot R_{\text{DS}}$$
(4)

where I_{DS} is a peak current of the transistor averaged over a fundamental cycle, V_{DS} is an averaged peak drain-source voltage at the moment of switching, t_{don} is a turn-on delay time, t_r is a rise time, t_{doff} is a turn-off time delay, t_f is a fall time, R_{DS} is the resistance of the switch open channel, I_{RMS} is the root mean square current value of transistor for one period of the output voltage and Q_{rr} is a reverse recovery charge.

In a similar way, the summarized losses of the single diode can be estimated as in [38]

$$P_{\text{DIODE}} = I_F \cdot V_F + f \cdot V_{\text{DR}} \cdot (Q_r + t_R \cdot I)$$
(5)

where V_F is the forward voltage drop of the diode, I_F is the average current of the diode, V_{DR} is the diode reverse voltage, t_R is the diode reverse recovery time and Q_r is the reverse recovery charge.

The weighted values of losses are recalculated in the p.u. system, where the largest value of all values is taken as a unit. All the other values are converted through this reference unit. It relates to all other parameters shown in Figure 2.



Figure 2. The comparison of the interleaved qZSI versus the single qZSI in terms of weighted values of transistor losses, diode losses, volume of capacitors, volume of inductors and cost of transistors and diodes.

It is assumed that the volume of the magnetic elements is proportional to the maximum energy that can be accumulated. The same is true for the capacitors.

The total maximum energy that can be accumulated in the inductors is calculated as

$$E_L = \sum_{i=1}^{N_L} \frac{L_i \cdot I_{\text{MAXi}}^2}{2}$$
(6)

where L_i is the inductance value and I_{MAXi} is the maximum current value through the inductor.

The total maximum energy that can be accumulated in the capacitors is calculated as

$$E_{\rm CW} = \sum_{i=1}^{N_{\rm C}} \frac{C_i \cdot V_{\rm MAXi}^2}{2} \tag{7}$$

where C_i is the capacitance value and V_{MAXi} is the maximum voltage value across the capacitor.

The weighted values of volumes are also recalculated in the p.u. system. It can be seen that the use of the interleaving approach leads to the reduction of the inductor volume. According to Equation (1), the inductance value of the single and the interleaved qZSI remains the same. On the one hand, in the interleaved approach, the power flow through each qZS network is decreased twice, while on the other hand it is assumed that the HF ripple of each inductor in the interleaving approach can be up to two times higher. Phase shifting between the currents of each channel compensates for the ripple increasing.

Despite the inductance value of each single inductor being the same for both solutions, according to Equation (6), the maximum energy of the interleaved inductors can be significantly smaller, due to the split current between the two channels.

Furthermore, Figure 2 shows that the interleaving approach may not only provide smaller magnetic elements, but also better efficiency due to the improved dynamic parameters of the semiconductors. It shows that the reduction of losses in active components is expected to be about 30%. These data correspond to the 200 V input voltage and the total input power of 1800 W.

4. Simulation and Experimental Study

In order to verify the theoretical statements, we conducted a simulation and an experimental study. The parameters of the selected topologies are shown in Tables 2 and 3. The main goal of the simulation study was to verify the calculation of the passive elements and to demonstrate the interleaving approach for ripple cancellation. In all cases, the switching frequency was about 60 kHz.

PSIM software was used as a simulation tool. Figure 3 shows our simulation results with the ST implementation at the 200 V input voltage and 1800 W total power. The input current of each channel, along with the summarized input current in the interleaved qZSI solution, are shown in Figure 3a. On the right side (Figure 3b), the input current of a single qZSI is shown. The figure shows that in the interleaved solution, the input current is slightly smaller than in the single solution. Figure 3c,d show output current waveforms, and how the output current is distributed between the two channels. Taking into account the maximum currents through the inductors and corresponding maximum energy accumulated in the inductors, we can claim that the interleaved solution enables a size reduction of about 40%.



Figure 3. Simulation results of the interleaved (a,c) and the single qZSI (b,d).

At the same time, the most important outcomes are found in the experimental study. A detailed experimental study of a single qZSI is presented in [23]. In the experimental study, we focused on the interleaved qZSI and its comparison with the single 2-level qZSI.

Figure 4 shows the experimental setup of the interleaved qZSI. It comprises two independent channels. The experimental setup also includes measurement equipment, such as the programmable DC power supply (PV array simulator) Chroma 62150H-1000S, a power analyzer YOKOGAVA WT1800 and an oscilloscope Tektronix MSO 4034B.



Figure 4. Experimental setup of the interleaved qZSI.

The dependence of the experimentally measured efficiency on the input voltage with constant input current is illustrated in Figure 5. This shows that the interleaved qZSI has higher efficiency than the single qZSI, which corresponds to the theoretical expectation. At the same time, the improvement of the efficiency is lower than that which was theoretically predicted. This can be explained by non-optimized prototyping and additional losses in the passive components, including wires and connectors.



Figure 5. Efficiency evaluation of the single qZSI and the interleaved qZSI under different input voltage and constant input current.

Experimental data in Figure 6 finalize the verification. The first case (Figure 6a, b) corresponds to the dc source input voltage.

The figures show the input current of each channel, along with the output voltage. A significant double frequency ripple can be seen in both qZSI channels, which is not fully compensated by the interleaving approach. Further double-frequency ripple mitigation is assumed to be achieved by a decoupling capacitor.

On the other hand, in the second case (Figure 6b), the advantage of the interleaving approach is much more obvious, and also has influence on the double frequency ripple. Figure 6c shows the common output current and the distribution between the channels. However, the current distribution between the qZSI channels is not symmetrical, which is explained by the limited tolerance of magnetic components that were essential in the open loop test.

The loss distribution in the interleaved qZSI is shown in Figure 6d. It corresponds to the same operation point with 200 V input voltage and 1 kW input power. As can be seen, significant losses come from the qZS diodes.



Figure 6. Experimental results of the interleaved qZSI: with an ideal dc source (200 V input voltage) (**a**,**b**), and with a photovoltaic (PV) panel as an input source (**c**), losses distribution in the operation point 200 V, 1 kW (**d**).

Finally, Figure 7a shows the back side of the PCB of the single channel with the heatsink of the qZS diode, while Figure 7b shows the thermal picture that corresponds to the operation point with 200 V input voltage and 1 kW input power.



Figure 7. Printed circuit board (PCB) of one single channel with the heatsink of the qZS diode (**a**) and its thermal picture in the operation point 200 V, 1 kW (**b**).

As can be seen, significant losses come from the qZS diodes whose heatsink is the hottest point (about 70 $^{\circ}$ C). The analysis of the thermal picture, along with the current measurements, compose the background for the analysis of loss distribution.

5. Conclusions

This work is devoted to the feasibility study of the interleaving approach for the qZSI, taking into account losses, the size of the components and semiconductor costs.

It was demonstrated that the interleaving approach may significantly reduce inductor size and cost by up to 40%. It is also shown that better efficiency can be achieved at the same cost of power semiconductor components. In our case study system, the losses were reduced by 15–20%.

However, these benefits do not guarantee a competitive advantage in mass industrial production. It is necessary to take into account the cost of auxiliary components and the need to control the symmetry of each channel, which will lead to an increase in the number of current sensors. A reliable conclusion can only be obtained in preparation for industrial production, taking into account the cost of all components.

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