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A Fully Integrated Compact Outphasing CMOS Power Amplifier Using a Parallel-Combining Transformer with a Tuning Inductor Method

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Received: 16 December 2019; Accepted: 28 January 2020; Published: 3 February 2020

Abstract: This work presents a compact on-chip outphasing power amplifier with a parallel-combining transformer (PCT). A series-combining transformer (SCT) and PCT are analyzed as power-combining transformers for outphasing operations. Compared to the SCT, which is typically used for on-chip outphasing combiners, the PCT is much smaller. The outphasing operations of the transformer combiners and class-D switching PAs are also analyzed. A tuning inductor method is proposed to improve the efficiency of class-D power amplifiers (PAs) with power-combining transformers in the out-of-phase mode. The proposed PA was implemented with a standard 0.18 µm CMOS process. The measured maximum drain efficiency is 37.3% with an output power of 22.4 dBm at 1.7 GHz. A measured adjacent channel leakage ratio (ACLR) of less than −30 dBc is obtained for a long-term evolution (LTE) signal with a bandwidth of 10 MHz.

Keywords: power amplifier (PA); outphasing; parallel-combining transformer; outphasing combiner; CMOS

1. Introduction

Power-combining techniques are widely used in the design of power amplifiers (PAs) to sum the power from individual linear PAs. Figure 1 shows a block diagram of a radio frequency (RF) transmitter, including a PA with a power-combining transformer. For on-chip power-combining techniques, many studies have used power-combining transformers, such as series-combining transformers (SCTs) and parallel-combining transformers (PCTs) [1–5].

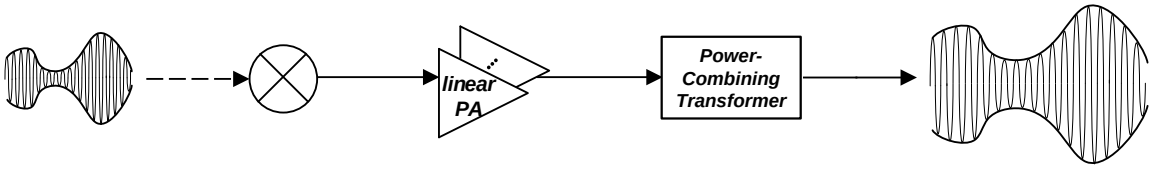

Figure 1. Power amplifier with a power-combining transformer in a transmitter.

A PA is a major consumer of power in an RF transceiver. Thus, there has been increasing demand for studies on PA structures to increase battery lifetime. One promising approach is outphasing, which is also known as linear amplification using nonlinear components [6–11]. In an outphasing

system, two constant amplitude signals in an outphasing PA can be combined using isolation or non-isolation power combiners, as shown in Figure 2. An isolation combiner [12], such as a Wilkinson combiner, provides good linearity because there is less interaction between two adjacent PAs. However, it has poor efficiency because the RF power is wasted when the phase angle of the outphasing signals is large. In contrast, a non-isolation combiner reduces the power dissipation by improving the wasted power in the combined outphasing signal. However, conventional non-isolation combiners typically require bulky quarter-wave transmission lines, which are difficult to integrate on a chip [13].

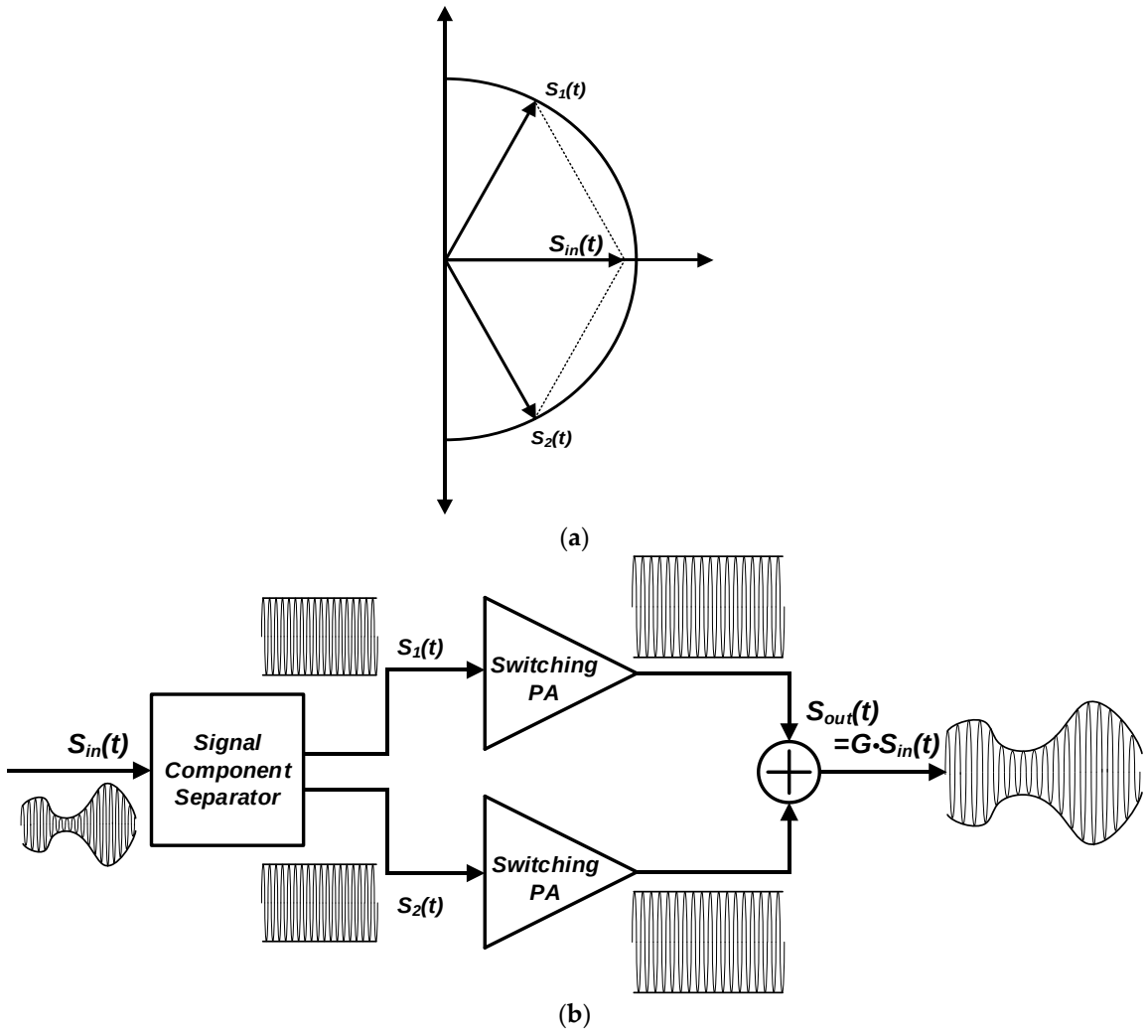

Figure 2. Outphasing principle and outphasing power amplifier (PA) architecture. (**a**) outphasing vector diagram, (**b**) outphasing architecture.

SCTs and PCTs can combine several individual amplifiers to increase the output power level, but only the SCT structure has been used for on-chip non-isolation outphasing PAs [14–16]. However, a PCT is typically much smaller than an SCT. When a PCT is incorporated in the circuit design, the required die area can be reduced compared with that of an SCT.

In this paper, we analyze the outphasing operation for SCT and PCT power-combining transformers, and propose a compact on-chip outphasing PA with a PCT. By analyzing SCT and PCT power-combining transformers with non-ideal transformer models as outphasing combiners, we verify that the outphasing summation property can be obtained with a smaller die area by using the PCT structure. In addition, we analyze the outphasing operation of class-D PAs with an outphasing

combiner using an SCT or PCT. A tuning inductor method is also proposed to improve the performance in out-of-phase mode.

This paper is organized as follows. Section 2 shows the analysis of the SCT and PCT as outphasing combiners and system simulation results using non-ideal SCT and PCT models. In Section 3, the analyses for the outphasing operation of transformers and class-D switching PAs are described, and a tuning inductor method is presented. Section 4 explains the circuit design. The measured results are discussed in Section 5, followed by the conclusion in Section 6.

2. Outphasing Combiner Using Power-Combining Transformers

Figure 2 illustrates the basic outphasing principle of the operation and outphasing PA architecture. The amplitude and phase modulated signal $S_{in}(t) = A(t)cos[\omega t + \phi(t)]$ can be separated into two constant-amplitude phase modulated signals:

$$S_1(t) = \frac{A_{max}}{2} cos[\omega t + \phi(t) + \theta(t)] \quad (1)$$

$$S_2(t) = \frac{A_{max}}{2} cos[\omega t + \phi(t) - \theta(t)] \quad (2)$$

where $S_1(t) + S_2(t) = S_{in}(t)$, $\boldsymbol{\omega}$ is the angular frequency, $A(t)$ is the amplitude of the signal of $S_{in}(t)$, $\phi(t)$ is the phase of the signal of $S_{in}(t)$, and A_{max} is the maximum value of A. The amplitude information of $S_{in}(t)$ is translated into the outphasing angle $\theta(t)$ by the following equation:

$$\theta(t) = cos^{-1}\left[\frac{A(t)}{A_{max}}\right] \text{ or } A(t) = A_{max} cos\ \theta(t) \quad (3)$$

The amplitude and phase modulated input signal $S_{in}(t)$ is decomposed into two constant-amplitude phase modulated signals, $S_1(t)$ and $S_2(t)$. Thus, switching PAs can be used to amplify $S_1(t)$ and $S_2(t)$, as shown in Figure 2. The two amplified signals from the two switching PAs are summed through an outphasing combiner to reconstruct the original signal with increased amplitude. To reconstruct the desired signal properly through the outphasing combiner, the condition of Equation (3) must be met for the amplitude of the combined signal. Thus, the summation property can be achieved when the amplitude through the output combiner is proportional to $cos\theta$ [14,15].

Isolation or non-isolation combiners can be used for outphasing combiners. An isolation combiner such as a Wilkinson combiner typically has low efficiency, so non-isolation combiners are widely used to achieve high efficiency. Transformer-based combiners have been applied as on-chip outphasing combiners because of the useful characteristics of a typical transformer, such as impedance matching, DC isolation, and signal summation. However, in previous research, only SCTs have been used for on-chip outphasing combiners, and their operation was analyzed with an ideal model of a transformer [14,15].

In this work, the operations of SCTs and PCTs as outphasing combiners are analyzed with non-ideal models of the transformer. Figure 3a shows an SCT with an equivalent non-ideal model. The operations of the outphasing combiner with switching PAs are also shown in Figure 3a, where the output signals of class-D PAs are modeled as voltage sources. The operation of class-D or class-F PAs is less sensitive to load variation [17–19], so they are preferred for outphasing PAs when considering linearity performance. A class-F PA requires multiple bulky resonant circuits, so class-D PAs are widely used for on-chip outphasing PAs [14–16].

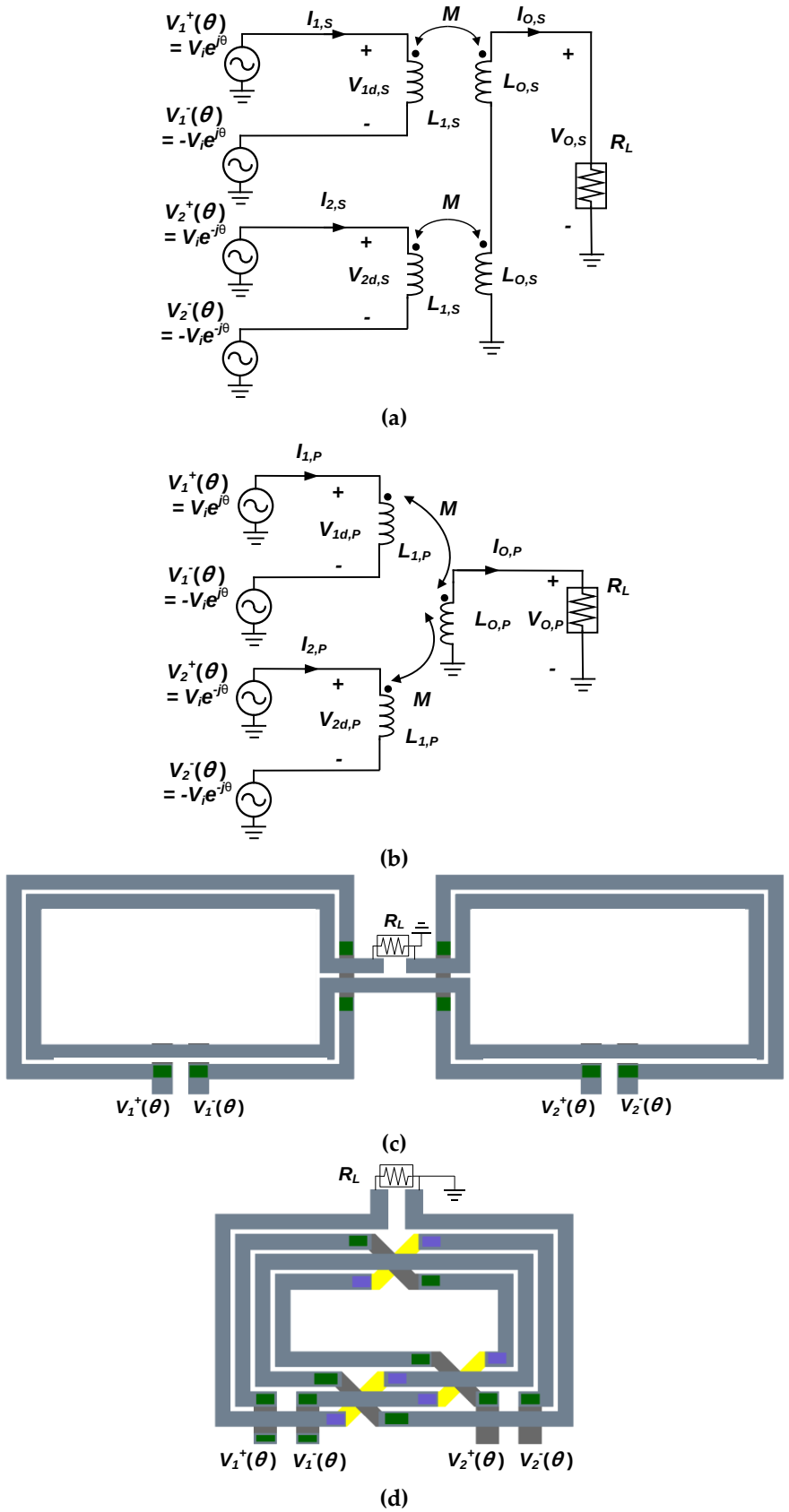

Figure 3. Outphasing operation for series-combining transformer (SCT) and parallel-combining transformer (PCT): (**a**) SCT with non-ideal model; (**b**) PCT with non-ideal model; (**c**) example layout for SCT; (**d**) example layout for PCT.

The input voltages of the outphasing combiner are $V_1(\theta) = V_i e^{j\theta}$ and $V_2(\theta) = V_i e^{-j\theta}$, where θ is the outphasing angle. For the differential case, the input voltages of the combiner are ${V_1}^+(\theta) = V_i e^{j\theta}$, ${V_1}^-(\theta) = -V_i e^{j\theta}$, ${V_2}^+(\theta) = V_i e^{-j\theta}$, and ${V_2}^-(\theta) = -V_i e^{-j\theta}$. As shown in Figure 3a, the voltage differences between the positive and negative parts of the primary winding are:

$$\begin{array}{c} V_{1d,S} = {V_1}^+(\theta) - {V_1}^-(\theta) = 2V_i(cos\theta + jsin\theta), \\ V_{2d,S} = {V_2}^+(\theta) - {V_2}^-(\theta) = 2V_i(cos\theta - jsin\theta) \end{array} \quad (4)$$

In the case of an SCT with the equivalent lumped model, the voltages at the primary and secondary windings are:

$$V_{1d,S} = j\omega L_{1,S} I_{1,S} - j\omega M I_{O,S} \text{ and } V_{2d,S} = j\omega L_{1,S} I_{2,S} - j\omega M I_{O,S} \quad (5)$$

$$V_{O,S} = I_{O,S} R_L = j\omega M(I_{1,S} + I_{2,S}) - 2j\omega L_{O,S} I_{O,S} \quad (6)$$

Using Equations (4), (5), and (6), the following relationship can be found:

$$\begin{array}{c} V_{1d,S} + V_{2d,S} = j\omega L_{1,S}(I_{1,S} + I_{2,S}) - 2j\omega M I_{O,S}, \\ I_{1,S} + I_{2,S} = \dfrac{V_{1d,S} + V_{2d,S} + 2j\omega M I_{O,S}}{j\omega L_{1,S}} = \dfrac{4V_i cos\theta + 2j\omega M I_{O,S}}{j\omega L_{1,S}} \end{array} \quad (7)$$

The relation for the output current can be derived from Equations (6) and (7) thus:

$$I_{O,S} = \frac{\frac{4MV_i cos\theta}{L_{1,S}}}{-\frac{2j\omega M^2}{L_{1,S}} + 2j\omega L_{O,S} + R_L} \quad (8)$$

The output voltage at the secondary winding is:

$$V_{O,S} = \left(\frac{4M/L_{1,S}}{-(2j\omega M^2/L_{1,S}) + 2j\omega L_{O,S} + R_L}\right) R_L V_i cos\theta. \quad (9)$$

The output voltage is proportional to $cos\theta$, and the outphasing summation property is satisfied. The desired signal can be reconstructed through the SCT combiner.

In the case of a PCT with an equivalent lumped model, as shown in Figure 3b, the voltages at the primary and secondary windings are:

$$V_{1d,P} = j\omega L_{1,P} I_{1,P} - j\omega M I_{O,P} \text{ and } V_{2d,P} = j\omega L_{1,P} I_{2,P} - j\omega M I_{O,P} \quad (10)$$

$$-j\omega M I_{1,P} - j\omega M I_{2,P} + (j\omega L_{O,P} + R_L) I_{O,P} = 0 \quad (11)$$

The relation for the output current can be derived from Equations (4), (10), and (11) thus:

$$I_{O,P} = \frac{\frac{4MV_i cos\theta}{L_{1,P}}}{-\frac{2j\omega M^2}{L_{1,P}} + j\omega L_{O,P} + R_L} \quad (12)$$

The output voltage at the secondary winding is:

$$V_{O,P} = I_{O,P} R_L = \left(\frac{4M/L_{1,P}}{-(2j\omega M^2/L_{1,P}) + j\omega L_{O,P} + R_L}\right) R_L V_i cos\theta \quad (13)$$

Thus, the outphasing summation property can be obtained using the PCT structure as well.

Example layouts for the SCT and PCT cases are shown in Figure 3c,d to compare their required die areas. The sizes of the layouts for the SCT and PCT are 0.425 × 1.6 mm and 0.425 × 0.715 mm,

respectively. Because a PCT is typically much smaller than an SCT, the required die area can be reduced by using a PCT as an outphasing combiner.

Simulations are performed using an Advanced Design System (ADS) to verify their outphasing operation. A diagram of the simulation setup is shown in Figure 4. A 16QAM OFDM signal is separated in MATLAB, and the separated outphasing signals are incorporated in the ADS simulation. Four outphasing signals are generated using the ideal balun, and an output signal is obtained with non-ideal SCT or PCT models. The simulated output constellations and spectrums are shown in Figure 5 for the SCT and PCT. Because the outphasing summation property can be obtained using both the SCT and PCT combiners, the desired ideal signals are reconstructed for both cases.

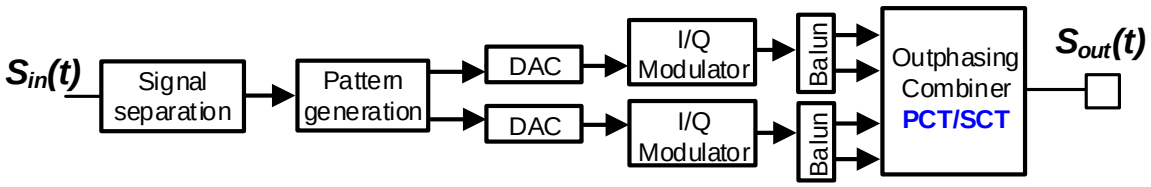

Figure 4. Block diagram for simulations of the outphasing combiner.

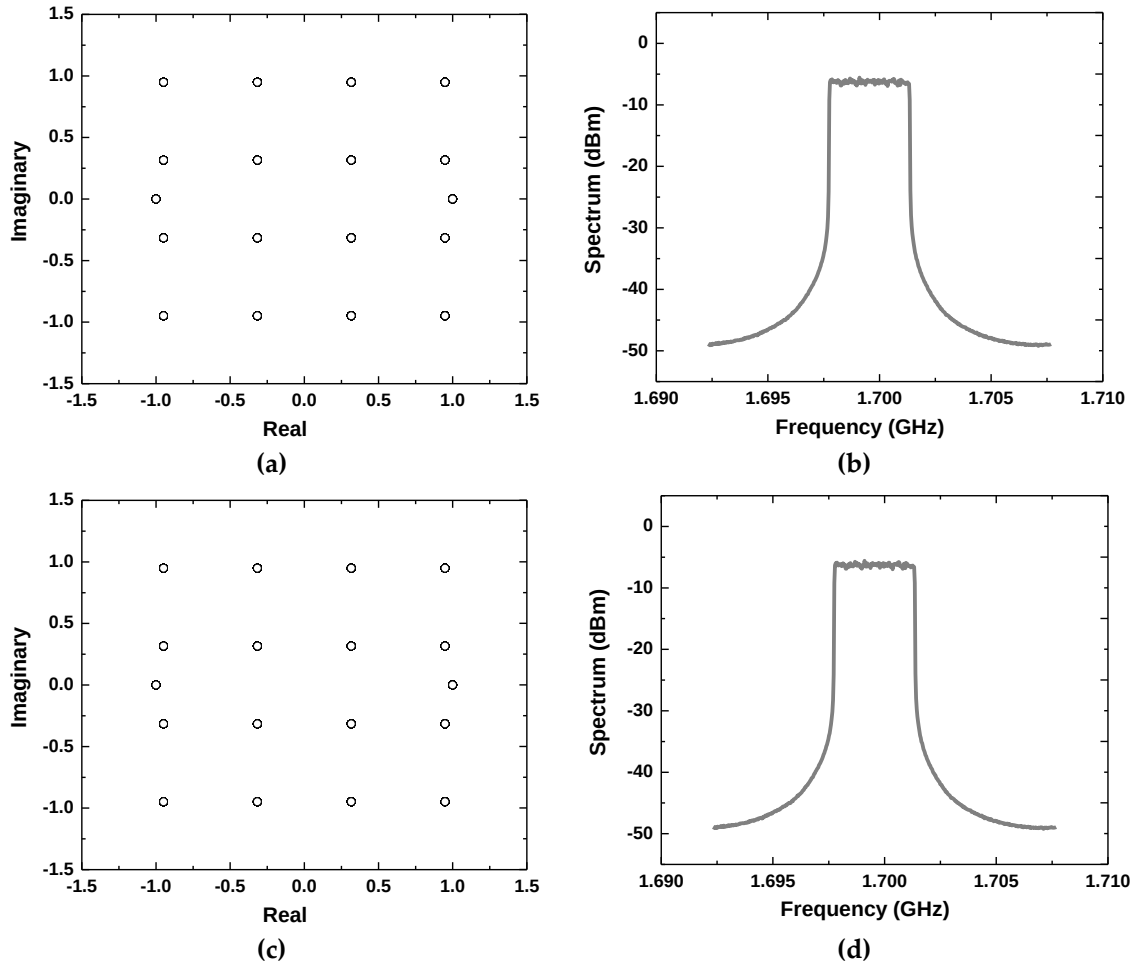

Figure 5. Simulated results of the outphasing combiners: (**a**) output constellation of the SCT; (**b**) output spectrum of the SCT; (**c**) output constellation of the PCT; (**d**) output spectrum of the PCT.

To evaluate the passive efficiencies of the SCT and PCT cases, electromagnetic (EM) simulations were performed using the ADS momentum for the example layouts in Figure 3. For the design of the SCT and PCT, a 3.4 μm thick Cu top layer was used. The efficiencies of the SCT and PCT cases are

compared in Figure 6. The efficiency of the PCT case is similar to that of the SCT case in the frequency range of 1.7–2 GHz.

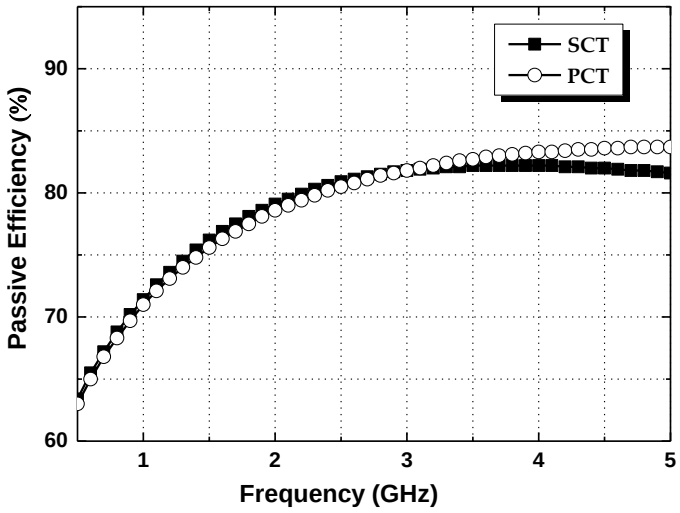

Figure 6. Simulated efficiency characteristics of SCT and PCT.

3. Outphasing Operation of Transformer Combiner and Class-D Switching PA

3.1. Outphasing Operation of Power-Combing Transformer

The $cos\theta$ term is an in-phase component of two separated outphasing signals. The in-phase components add up at the output. As shown in Equation (3), $sin\theta$ is an out-of-phase component of two outphasing signals, which is not required for the reconstruction of the signal. In addition, at the back-off level, as the outphasing is increased, the in-phase component ($cos\theta$) is decreased, and the out-of-phase component ($sin\theta$) is increased, resulting in greater power loss. Thus, to increase the efficiency, the components of $sin\theta$ (out-of-phase components) generated from a unit class-D PA should be minimized.

To consider the power loss of the transformer, the loss resistors $R_{1,P}$ and $R_{O,P}$ are added in Figure 7a. The power loss in each primary winding can be expressed as ${I_{1,P}}^2 R_{1,P}$. The current $I_{1,P}$ flowing through the primary winding can be expressed as:

$$\begin{aligned} I_{1,P} &= \frac{V_{1d,P} + j\omega M I_{O,P}}{j\omega L_{1,P} + 2R_{1,P}} \\ &= \frac{j2V_i}{j\omega L_{1,P} + 2R_{1,P}} sin\theta + \frac{2V_i}{j\omega L_{1,P} + 2R_{1,P}} \left(1 + \frac{j2\omega M^2 R_L / L_{1,P}}{-(2j\omega M^2 / L_{1,P}) + j\omega L_{O,P} + R_{O,P} + R_L}\right) cos\theta \end{aligned} \tag{14}$$

To improve the power loss at the back-off level, the $sin\theta$ component needs to be removed. These components can be removed from $I_{1,P}$ when two input signals for the SCT or PCT are exchanged in Figure 7b. The voltage differences between the positive and negative parts of the primary windings are:

$$V_{1d,P} = V_{2d,P} = 2V_i cos\theta \tag{15}$$

$I_{1,P}$ is expressed using Equation (15) as:

$$I_{1,P} = \frac{2V_i}{j\omega L_{1,P} + 2R_{1,P}} \left(1 + \frac{j2\omega M^2 R_L / L_{1,P}}{-(2j\omega M^2 / L_{1,P}) + j\omega L_{O,P} + R_{O,P} + R_L}\right) cos\theta \tag{16}$$

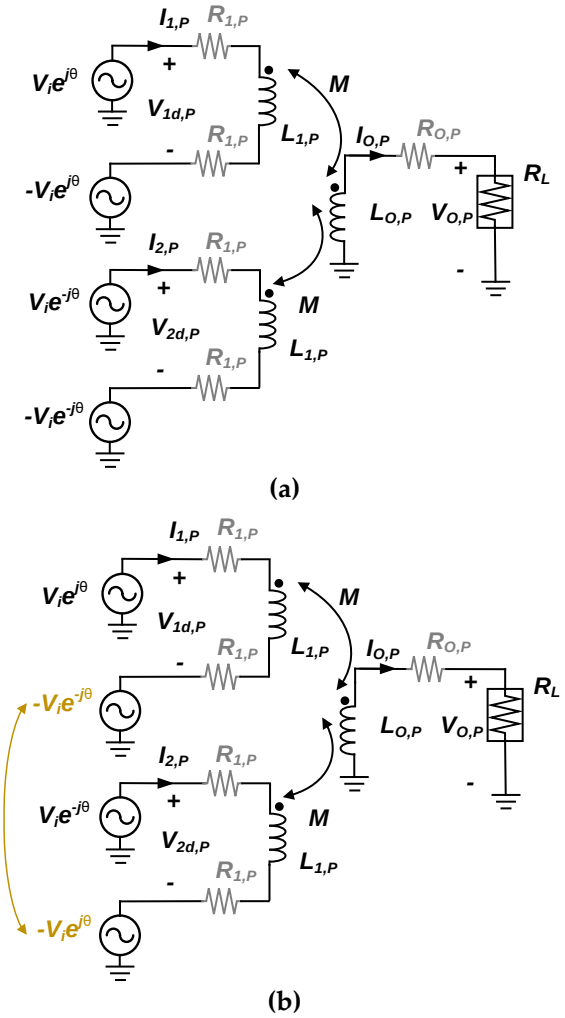

Figure 7. (**a**) A non-ideal PCT model with typical input feeding structure; (**b**) a non-ideal PCT model with the proposed input feeding structure.

The $sin\theta$ component is removed, resulting in an improvement for power loss.

The relationships for $V_{1d,P} + V_{2d,P}$ and $I_{1,P} + I_{2,P}$ are the same as in the case of Figure 3b, without considering the loss resistors $R_{1,P}$ and $R_{O,P}$. Therefore, the expression for the output voltage in Figure 7b is the same as Equation (13). Thus, the desired output signal can be restored. The change of the input feeding order to improve the efficiency at the back-off has been explained in a previous study [14] using the case of an SCT with an equivalent T-model.

3.2. Outphasing Operation of Class-D Switching PAs with Power-Combining Transformer

The outphasing operation of the switching PA with the SCT or PCT is analyzed in terms of in-phase and out-of-phase components of the outphasing signals. Figure 8 shows multiple class-D PAs with output parasitic capacitance. For designs of the PAs, the size of device is typically large to generate high output power. In this case, the output capacitance of the device is also large, and should be incorporated into the operation of the PA. The operation for in-phase components is illustrated in Figure 8a.

In the in-phase mode, the operation is the same as in the differential case. The equivalent reflected transformer model for the input side can be translated into a parallel inductor and resistor. For the operation of a differential class-D PA with a parallel resonant circuit, the output capacitor is tuned out with the reflected parallel inductor L_{eq}. With this operation, the in-phase component of the signal is delivered to the parallel resistor R_{eq}.

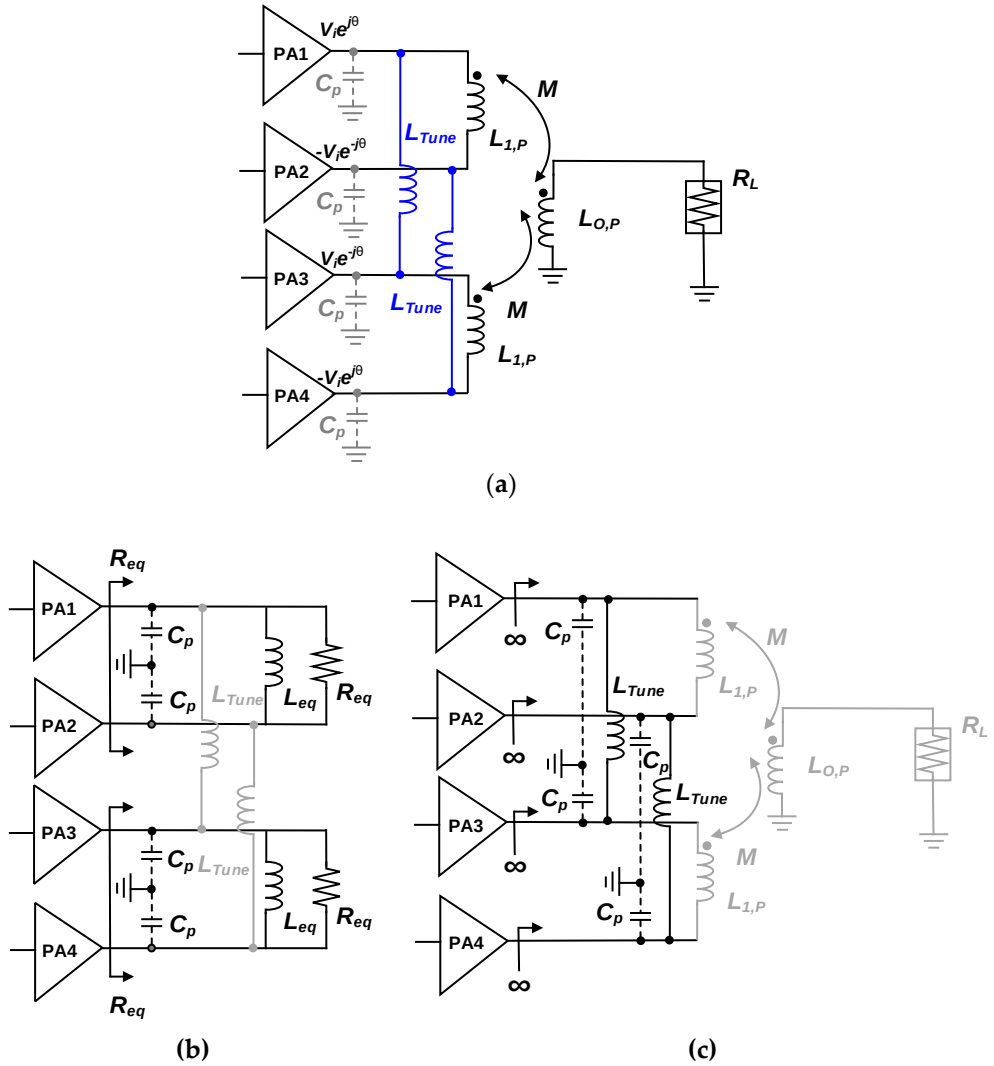

Figure 8. (**a**) Proposed structure for class-D PA with PCT; (**b**) in-phase mode; (**c**) out-of-phase mode.

For the out-of-phase mode, the equivalent circuit is shown in Figure 8c. The voltage potentials are the same for two transformer inputs of the PCT (the outputs of PA1 and PA2 or the outputs of PA3 and PA4). Therefore, no current flows through the input primary winding of the PCT. The efficiency at the back-off level is decreased by the effect of parasitic capacitors. Thus, to improve efficiency at the back-off level, a class-D PA with a power-combining transformer for the outphasing system is proposed. In the proposed architecture, additional tuning inductors, L_{Tune}, are added to remove the effect of the parasitic capacitance in the out-of-phase mode. These parallel resonant circuits provide very high impedances, resulting in the reduced contribution of the out-of-phase components. In addition, the voltage potentials are the same for the outputs of PA1 and PA3 (or the outputs of PA2 and PA4) in the in-phase mode, so no current flows through the tuning inductors. Thus, the operation of the in-phase mode is not affected by L_{Tune}.

4. Circuit Design

To implement a compact outphasing CMOS PA, a PCT outphasing combiner is designed. Figure 9 shows the layout of the PCT. The size of the PCT is 0.745×0.515 mm^2. Transformers are designed with a 2.34 µm thick Al top metal layer in a standard 0.18 µm CMOS process. The transformer windings use 30 µm wide lines and 5 µm spacing. A turn ratio of 1:2 is selected to provide impedance transformation. Because all primary and secondary windings are concentrated in a smaller space, the size of the PCT

can be much smaller than that of the SCT. To estimate its performance, EM simulations are performed using the ADS momentum. The simulated inductances of each primary winding and secondary winding are 1.35 nH and 3.25 nH, respectively, at 1.7 GHz. The EM simulated PCT achieves a coupling factor of 0.71.

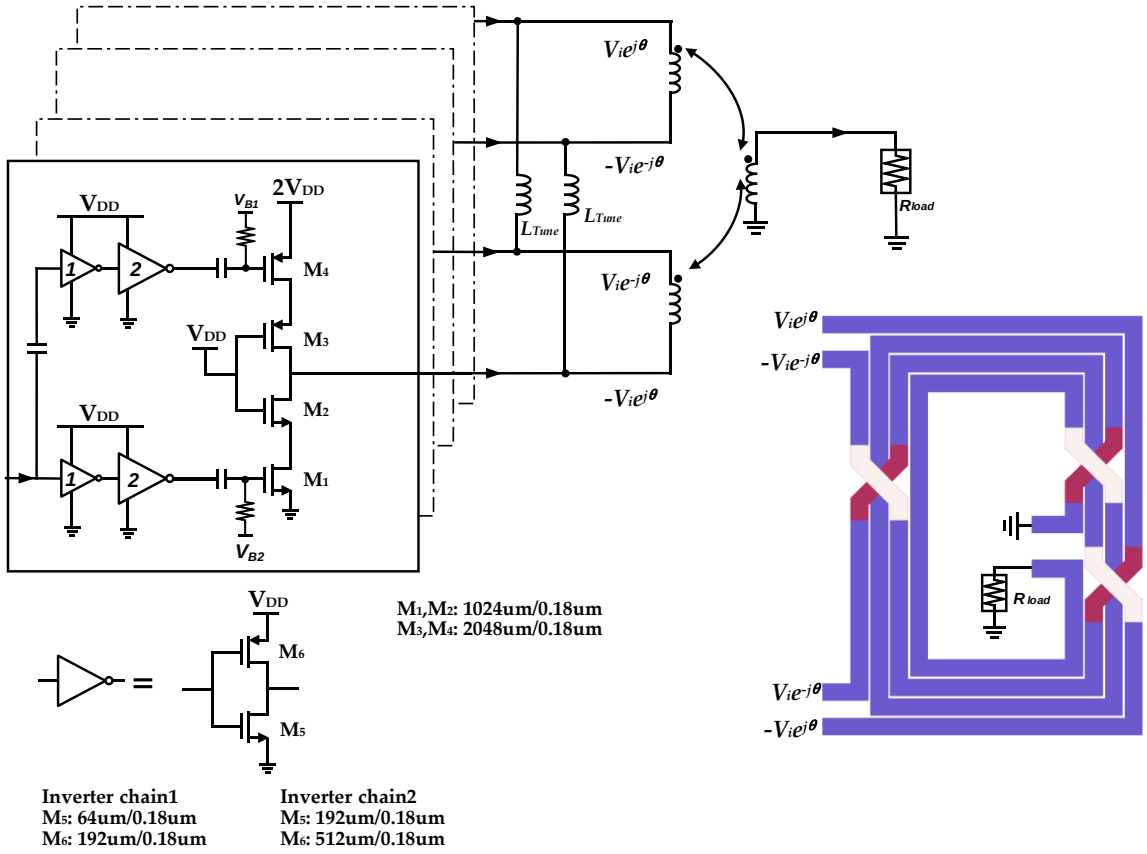

Figure 9. Schematic of the proposed outphasing PA using the parallel-combining transformer.

The proposed outphasing system is designed with four class-D PAs using the proposed PCT. Figure 9 also shows a simplified schematic of the class-D PA and its associated circuits, including the inverter chain. The four outphasing PAs are connected to positive or negative parts of the two primary windings of the PCT. A cascoded inverter-based class-D PA using thin-gate devices is designed using a 3.6 V supply. Thin-gate devices of L = 0.18 μm are used to minimize on-resistance as well as parasitic capacitances of the transistor. To increase output power from each unit class-D PA, the cascoded inverter topology is adopted, which allows an output voltage swing of twice the nominal supply voltage (V_{DD} = 1.8 V). The transistor widths of NMOS (M_1/M_2) and PMOS (M_3/M_4) on each unit class-D PA are 1024 μm and 2048 μm, respectively, as shown in Figure 9. Each inverter chain operates with a 1.8 V supply.

The two tuning inductors shown in Figure 9 are added between the drains of two class-D PAs to improve the back-off efficiency. The EM simulated tuning inductance, L_{Tune}, is 2.15 nH at 1.7 GHz. Figure 10 shows the simulated efficiency versus output power with and without tuning inductors. An EM simulated transformer model is used for the circuit simulations. The results show that the proposed PA, with tuning inductors, improves the efficiency performance by approximately 10% at the 6-dB back-off level (55-mW output power) of the output power. Figure 11 shows the simulated output voltage waveforms of each class-D PA. The simulated voltage waveforms of the class-D PAs are not degraded with the variation of the outphasing angle because of the tuning inductor method.

Thus, the efficiency performance can be higher when the outphasing angle is increased, as shown in Figure 10.

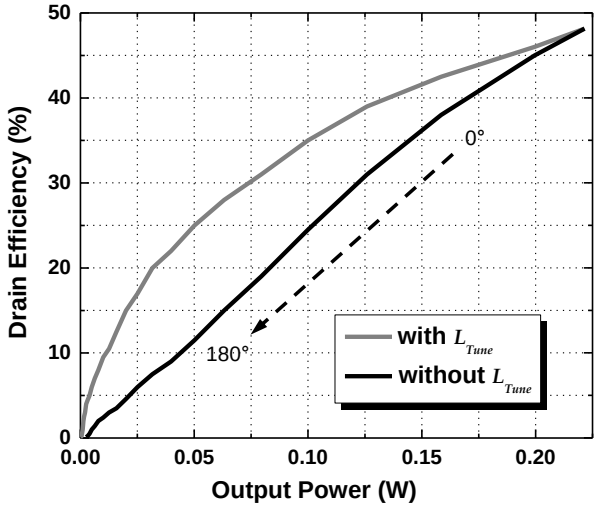

Figure 10. Simulated drain efficiency versus output power.

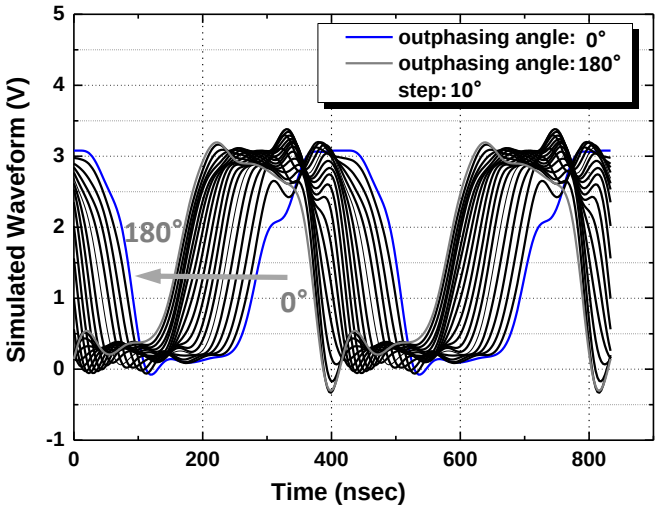

Figure 11. Simulated waveforms of the drain voltage.

5. Measurement Results

To verify its operation of the proposed outphasing CMOS PA using the compact PCT with a tuning inductor method, a fully integrated outphasing CMOS PA was fabricated using a standard 0.18 μm CMOS process. A die photograph of the implemented PA is shown in Figure 12. The chip area is 1.2×1.6 mm^2, including the input and output PADs.

The signal decomposition into $V_1(\theta)$ and $V_2(\theta)$ was performed using MATLAB, as shown in Figure 13. The decomposed data were downloaded into a pattern generator and fed to a dual-RF channel TSW3084 board with digital-to-analog converters (DAC3484) [20,21]. To generate the differential signals, external baluns (BALH-0006) were used. Thus, two differential RF signals ($V_1{}^+(\theta)$, $V_1{}^-(\theta)$, $V_2{}^+(\theta)$, and $V_2{}^-(\theta)$) were applied to the test chip. The offset of the path mismatch between the paths for $V_1(\theta)$ and $V_2(\theta)$ was measured with a signal analyzer, and corrections for the offsets were applied to the pattern generator.

Figure 14 shows the measured output power and drain efficiency (DE) according to the outphasing angle variation at 1.7 GHz. A maximum DE of 37.3% was achieved with an output power of 173 mW

(22.4 dBm) with V_{DD} = 1.8 V and $2V_{DD}$ = 3.6 V. The DE is defined as output power divided by DC power consumption of the final class-D PA stage. The measured DE versus output power is shown in Figure 15. The maximum power-added efficiency (PAE) was 26.5%, where the PAE is defined as output power divided by the DC power consumption of the final class-D PA stage and all inverter chains. The measured PAE is approximately 10% lower than DE in this work, but that is caused by the non-optimization of the two-stage inverter chain. In addition, the device size of the inverter chain using a 0.18 μm CMOS process will be larger than other works using a nanometer CMOS process, resulting in the large driving loss. If it is well-optimized further, and implemented using a nanometer CMOS process, PAE can be readily improved.

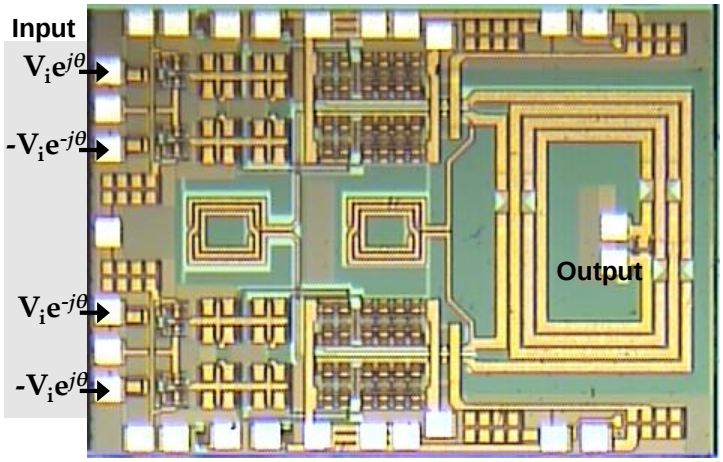

Figure 12. Die photograph of on-chip outphasing CMOS PA.

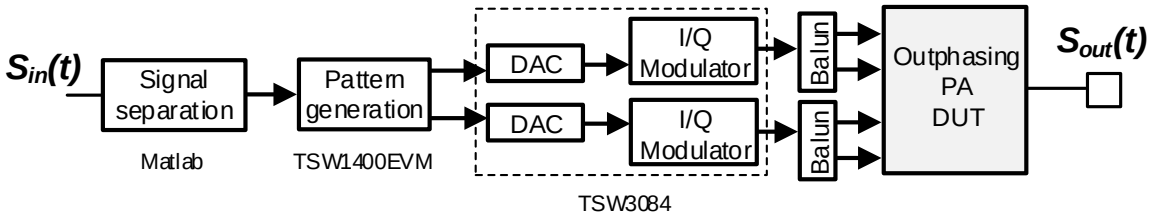

Figure 13. Block diagram for measurement of the outphasing PA.

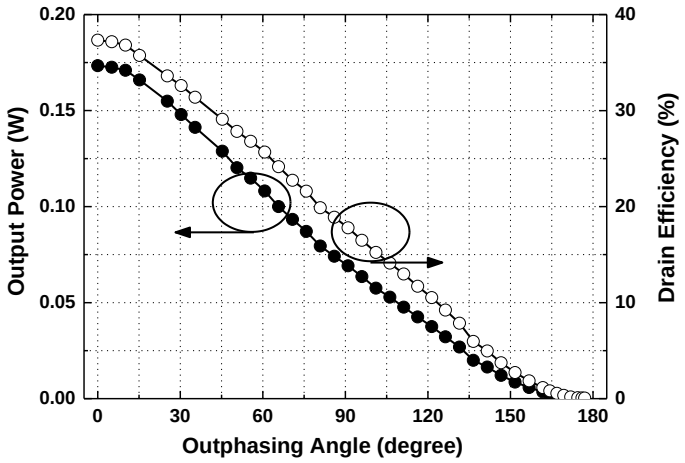

Figure 14. Measured output power and drain efficiency versus outphasing angle.

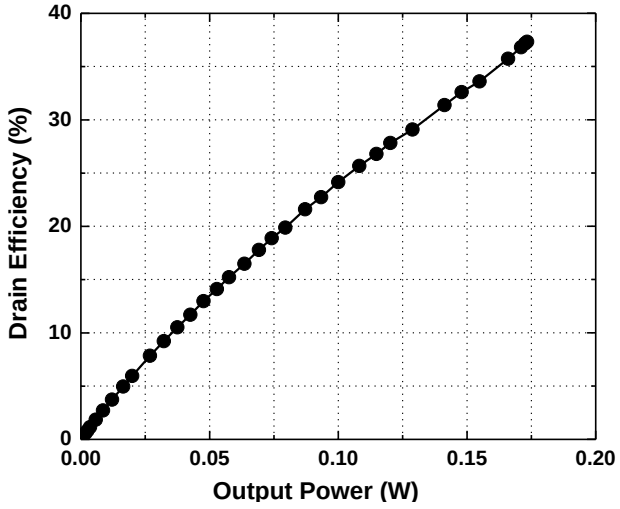

Figure 15. Measured drain efficiency versus output power.

A modulated signal measurement was performed with a long-term evolution (LTE) signal with 10 MHz bandwidth, as shown in Figure 16. Without a digital pre-distortion (DPD) applied, the adjacent channel leakage ratio (ACLR) of the proposed outphasing PA was obtained at less than −30 dBc, up to 13.81 dBm, with a $2V_{DD}$ of 3.6 V. Because the summation property can be obtained using the PCT outphasing combiner, the output signal was properly reconstructed. To check the capability of wide-frequency operation, the LTE signal was also tested at 1.9 GHz. By increasing the supply voltage, the linear output power could be increased. An ACLR of less than −30 dBc was obtained at up to 17.48 dBm, with $2V_{DD}$ = 3.8 V at 1.9 GHz.

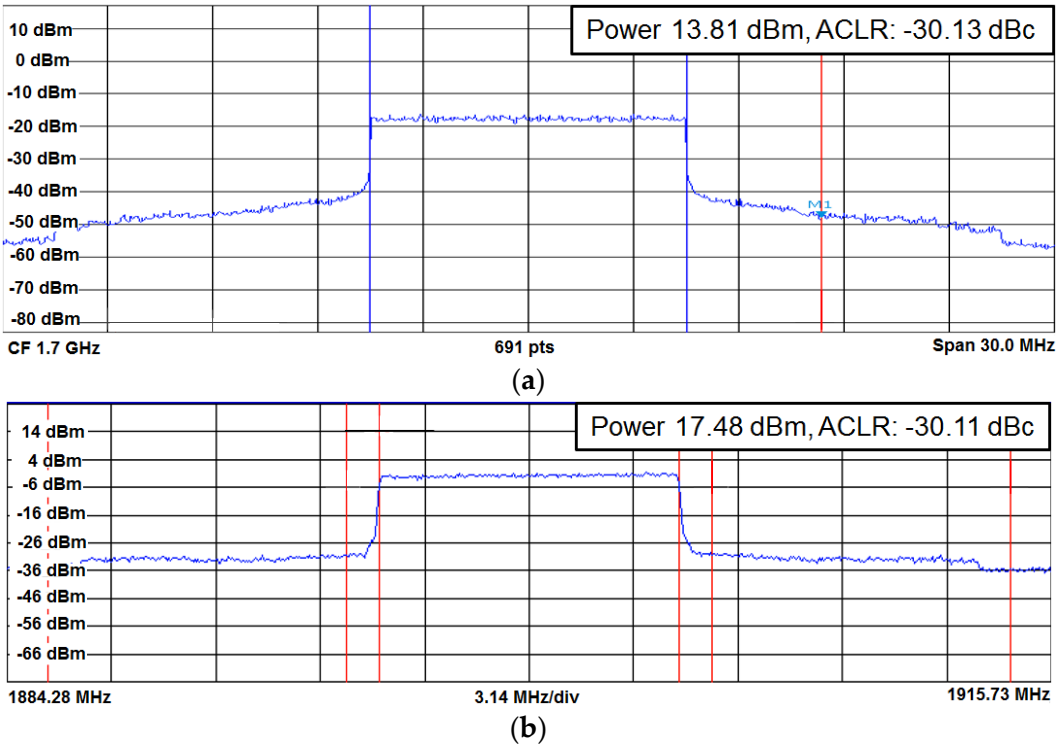

Figure 16. Measured PA output spectrum for the long-term evolution (LTE) signal: (**a**) 13.81 dBm with $2V_{DD}$ = 3.6 V at 1.7 GHz; (**b**) 17.48 dBm with $2V_{DD}$ = 3.8 V at 1.9 GHz.

Table 1 shows a comparison of this work with state-of-the-art outphasing CMOS PAs. The implementation methods of outphasing combiners are also indicated in Table 1. In [21,22], off-chip baluns and multiple inductors and capacitors are required for the construction of the outphasing combiners, and thus the outphasing combiners were implemented using off-chip lumped elements on the printed circuit boards (PCBs). In [14], an additional off-chip output balun is required on the PCB, and its loss was de-embedded during the measurement procedure. For fully integrated outphasing combiners, only SCT structures have been previously used [15,16]. In this work, a CMOS outphasing combiner that uses a PCT structure is proposed. In addition, the PCT structure, in its role as an outphasing combiner, is analyzed using non-ideal transformer models and verified with measurement results. Because the PCT structure can be approximately half the size of the SCT, as shown in Figure 3, an implemented outphasing combiner using a PCT structure can save the required die area. Among the CMOS outphasing PAs using fully integrated outphasing combiners, the size of the outphasing combiner in this work is much smaller than those in other works.

Table 1. Performance comparison with outphasing CMOS PAs.

Ref.	Integrated Combiner	Combiner (size: mm^2)	Tech. (nm)	Freq. (GHz)	$P_{OUT, MAX.}$ (dBm)	PAE (%) @ $P_{OUT, MAX.}$
[14]	Partially integrated	SCT (0.471 *) w/ external balun *	32	2.4	25.3	35
[15]	Yes	SCT (1.551 *)	45	2.4	31.5	27
[16]	Yes	SCT (0.706 *)	130	1.85	32.0	15.3 (20.1 †)
[21]	No	N.A.	45	2.4	29.5	43.52 (46.76 †)
[22]	No	N.A.	45	2.4	31.6	43.7 (49.2 †)
This work	Yes	PCT (0.384)	180	1.7	22.4	26.5 (37.3 †)

* graphically estimated, † drain efficiency, * loss has been de-embedded.

6. Conclusions

In this study, a compact on-chip outphasing CMOS PA using PCT was proposed and evaluated for 0.18 μm CMOS technology. To obtain outphasing summation operation with a small die area, the proposed on-chip outphasing CMOS PA with PCT was designed. The operations of the SCT and PCT as on-chip outphasing combiners were analyzed using non-ideal transformer models. In addition, the operations of a class-D PA with outphasing transformer combiners (e.g., SCT and PCT) were analyzed in the in-phase and out-of-phase modes. A tuning inductor method was proposed to improve the power loss in the operation of the out-of-phase mode. Without DPD, an ACLR of −30 dBc was obtained for a 10 MHz bandwidth LTE signal. For fully integrated outphasing PAs, the size of the outphasing combiner in this work is much smaller than other works. The results indicate that the proposed outphasing combiner is an attractive candidate for compact outphasing transmitters.

Author Contributions: S.-E.C. performed circuit design and experiments under the supervision of O.L., H.A. performed the experiments. J.H., K.-W.K., I.N., and J.C. provided significant comments and technical feedback throughout the research. O.L. conceived of the methodology and wrote the paper. All authors analyzed the data and edited the manuscript. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This work was supported by the Basic Science Research Program through the National Research Foundation of Korea, funded by the Ministry of Science, ICT & Future Planning under Grant No. 2017R1A2B1004726, and by the Ministry of Science and ICT, Korea, under the Information Technology Research Center Support Program under Grant No. IITP-2019-2017-0-01635, and was supervised by the Institute for Information & Communications Technology Promotion. The CAD tool was supported by the IDEC.

Conflicts of Interest: The authors declare no conflict of interest.

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