electronics

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Influence of Flexibility of the Interconnects on the Dynamic Bending Reliability of Flexible Hybrid Electronics

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Received: 28 December 2019; Accepted: 22 January 2020; Published: 1 February 2020

Abstract: The growing interest towards thinner and conformable electronic systems has attracted significant attention towards flexible hybrid electronics (FHE). Thin chip-foil packages fabricated by integrating ultra-thin monocrystalline silicon integrated circuits (ICs) on/in flexible foils have the potential to deliver high performance electrical functionalities at very low power requirements while being mechanically flexible. However, only very limited information is available regarding the fatigue or dynamic bending reliability of such chip-foil packages. This paper reports a series of experiments where the influence of the type of metal constituting the interconnects on the foil substrates on their dynamic bending reliability has been analyzed. The test results show that chip-foil packages with interconnects fabricated from a highly flexible metal like gold endure the repeated bending tests better than chip-foil packages with stiffer interconnects fabricated from copper or aluminum. We conclude that further analysis work in this field will lead to new technical concepts and designs for reliable foil based electronics.

Keywords: system-in-foil; flexible interposer; chip embedding; embedding in flex; fatigue reliability; flip-chip; ultra-thin silicon; chip-on-foil; thin metal film

1. Introduction

Recently developed process technologies for the integration of thin semiconductor components like state-of-the-art micro-controller ICs (integrated circuits) and sensor devices on or in flexible foil substrates have paved the way for extremely thin and even bendable electronic systems [1–3]. This so-called flexible hybrid electronics (FHE) enables a wide spectrum of new applications in consumer electronics, like for instance advanced wearable health monitoring devices such as smart watches and sensor plasters [4–9] and bendable as well as foldable mobile phones [10,11]. Besides, niche applications such as electronic skin for robotics as well as prosthetics [12–15] and ultra-thin IC packages [16–18] for miniaturized electronic packages could also benefit from FHE. Recent advances in FHE are very promising [19–25] and therefore, FHE is expected to play a vital role in further developments of these applications. Furthermore, low cost production of FHE components such as chip-foil packages for these applications could be achieved by implementing roll-to-roll (R2R) manufacturing processes [26]. A majority of the aforementioned applications require devices that are anticipated to bend repeatedly during the device usage, for, e.g., sensors and actuators placed in smart plasters and electronics skin. However, FHE is a relatively younger field of research that is still in its nascent stages of

development and hence, information available regarding the static [27–32] as well as dynamic bending reliability [33–36] of FHE components is rather very limited. Several studies have shown that the failure of chip-foil packages during repeated bending occur mainly because of the cracking of interconnects rather than the delamination of the chip from foil or chip fracture [34–36]. Hence, it is crucial to investigate various factors influencing the dynamic bending reliability of interconnects and to devise techniques to enhance the dynamic bending reliability of chip-foil packages. It is well known that the flexibility of metals increase with a decrease in their Young's modulus and increase in Poisson's ratio [37–40]. However, quantification of the influence of flexibility of the interconnect metal on the dynamic bending reliability would serve as a key information for fabricating reliable FHE systems. In line with this objective, we investigated the effect of flexibility of interconnects on the dynamic bending reliability of chip-foil packages by conducting repeated bending tests on chip-foil packages having interconnects fabricated from three metals with varying flexibility namely (i) copper, (ii) aluminum and (iii) gold.

This paper is organized as follows. The ensuing Section 2 explains the sample fabrication process. Then, the experimental setup used for the investigations is described in the subsequent Section 3. Next, the following Section 4 discusses the obtained test results. Finally, concluding remarks and our outlook for future works are included in Section 5.

2. Sample Fabrication Process

The chip-foil package samples required for investigating the dynamic bending reliability were fabricated by following various process steps that can be grouped as follows: 1. Interconnect fabrication on the foil substrate, 2. thinning of the silicon chips and 3. integration of the ultra-thin silicon chips on the foil substrates.

2.1. Fabrication of Interconnects on the Foil Substrate

We implemented semiconductor microfabrication processes such as sputter deposition, lithography and wet etching for patterning the interconnects on the foil substrate. Commercially available UPILEX® 50S polyimide (PI) with a thickness of 50 µm was used as the substrate foil for fabricating the interconnects. UPILEX® 50S was selected as the substrate due to its lower high-temperature shrinkage, higher maximum operating temperature, higher glass transition temperature (T_g), lower permeability to gas and water vapor, lower moisture uptake and lower coefficient of thermal expansion (CTE) [41–43]. The process was performed on the wafer level and therefore the first step in the process was to attach the PI foil on a 6'' carrier wafer. Next, the respective metals were sputter deposited on the PI foil using a Balzers LLS vertical sputter tool. The first step in the sputter deposition process was the activation of the substrate surface with argon plasma etching. Copper and gold exhibit poor adhesion to the polyimide foil. Therefore, a titanium tungsten (Ti10W90) adhesion layer having a thickness of 15 nm was sputter deposited prior to depositing copper and gold without breaking vacuum after deposition of the adhesion layer. After deposition of the metals, a positive photoresist (AZ®1514) was spin coated and then lithographically patterned to define the interconnects. Exposure was performed at a Süss mask aligner MA6 using soft contact. Then, wet etching of the metals was executed using commercially available etchants: K–KI based etchant for Au, $Na_2S_2O_8$ solution for Cu and PWS etchant for Al. Etch rates were adjusted by using the appropriate concentration and temperature to achieve etch rates in the range of 180–270 nm/min. The TiW layer was then etched separately using H_2O_2. Finally, the resist was stripped using suitable solvent-based media to pattern the interconnects. The layer thickness of the fabricated interconnects was about 300 nm.

2.2. Fabrication and Thinning of Silicon Chips

The ultra-thin silicon chips consisting of daisy chain test patterns were fabricated following the well-known dicing-by-thinning process that follows a subtractive approach [44]. In the first step, daisy chain tests patterns were fabricated on prime silicon wafers having a thickness of approximately

700 µm. Then, grooves were scribed on the front side of the sample wafer using a wafer saw along the predefined boundaries of the test chips. After sawing, the sample wafer was bonded to a rigid carrier wafer using a solvable glue. Next, the bonded stack was transferred to a wafer grinder where the sample wafer was thinned down by grinding from its rear side using rotating diamond wheels that remove material physically. Wafer grinding normally consists of a coarse and a fine grinding step depending on the size of the diamonds used to remove material. The rear side of the wafer is typically rough even after fine grinding having total thickness variation (TTV) in the range of 1–2 µm. After completion of the grinding step, chemical mechanical polishing involving fine removal of wafer (<1 µm/min) with abrasive medium was performed to improve the surface quality of the rear side of the wafer thereby enhancing the fracture strength of the wafer [45]. Finally, the thinned down test chips were released from the carrier wafer by dissolving the glue with an organic solvent. The thickness of the released chips was about 20 µm. Further information about the dicing-by-thinning process is available in [44].

2.3. Integration of Ultra-Thin Silicon Chips on Foil Substrates

The fabricated ultra-thin silicon chips were then bonded on to the interconnects of the foil substrates using flip-chip bonding with an anisotropic conductive adhesive (ACA). ACA is an epoxy consisting of suspended metal particles that establishes electrical interconnection between the chip pads and the corresponding foil interconnect upon application of pressure. The salient feature of ACA is that it is conductive in the *Z*-axis while remaining non-conductive in the *X* and *Y*-axes upon curing. We used Delo Monopox AC 245 that has nickel particles having a diameter of 5.3 µm to bond the chips in this work [46]. The flip-chip bonding process was performed in a programmable die bonding equipment, Panasonic FCB3 at a temperature of ~200 °C and a bonding force of 5 N. Figure 1 presents a scanning electron microscopy image of a typical example of the cross-section of single contact pad interconnection of a flip-chip bonded chip-foil package. The fabricated chip-foil packages with copper, aluminum and gold interconnects are shown in Figure 2.

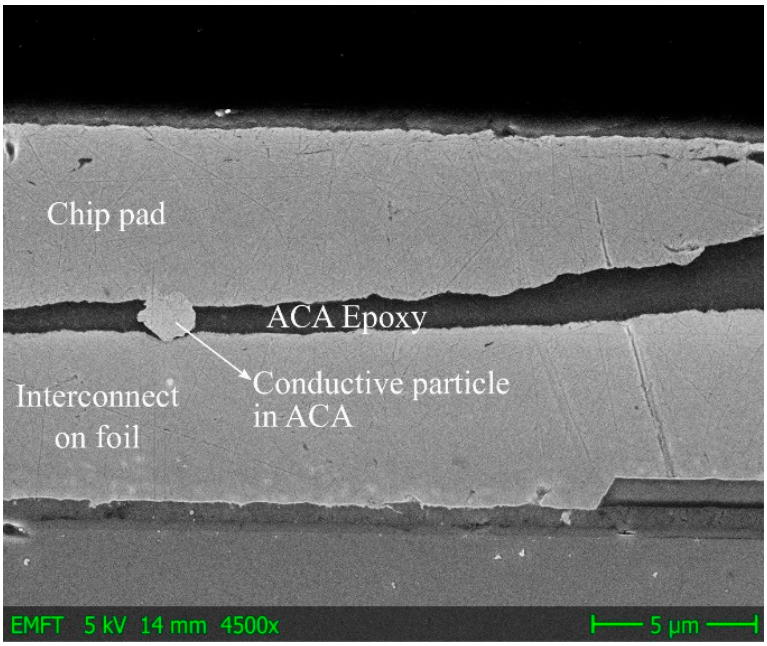


Figure 1. Scanning electron microscopy image of a typical example of the cross-section of a single contact pad interconnection of a flip-chip bonded chip-foil package.

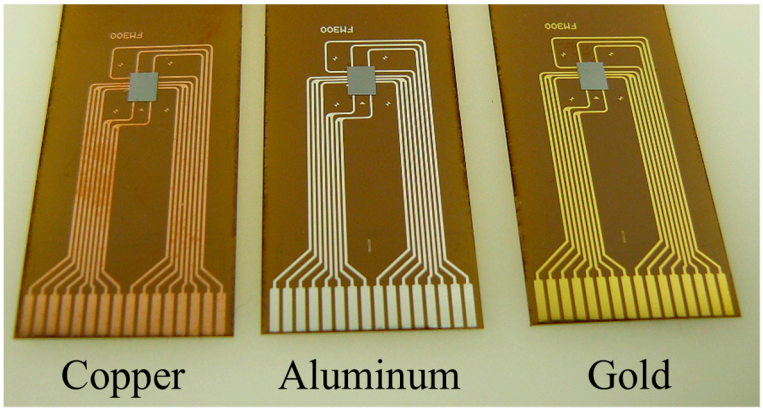


Figure 2. Chip-foil package test samples with copper, aluminum and gold interconnects.

3. Experimental Setup and Procedure

3.1. Test Equipment

The dynamic bending tests on the fabricated chip-foil packages were performed in custom-built test equipment (shown in Figure 3) that facilitates online measurement of the electrical characteristics of the test samples. The equipment primarily consists of two parts: 1. a fixed platform and 2. a movable arm. The samples were fixed to the test equipment with one end of the samples attached to the fixed platform and the other end to the movable arm. The chip-foil package sample was attached to the fixed platform through a zero-insertion force (ZIF) connector mounted on a Printed Circuit Board, PCB (Figure 4). The PCB connects the test samples with a parameter analyzer (Keysight 4156C) via a ribbon cable for measuring the electrical parameters of the samples. The resistance of daisy chain structures of the chip-foil package samples was measured during the tests in this work and a change in the daisy chain resistance was monitored to identify failure of the test samples. The movable arm was connected to a stepper motor from Festo AG & Co. KG (Esslingen, Germany) that controlled the bending cycles through a software interface. The number of bending cycles and the frequency of the bending cycles can be defined via the software interface. A polytetrafluoroethylene (PTFE) mandrel was attached to the fixed platform to define the bending radius and the samples were bent repeatedly back and forth around the mandrel during the tests.

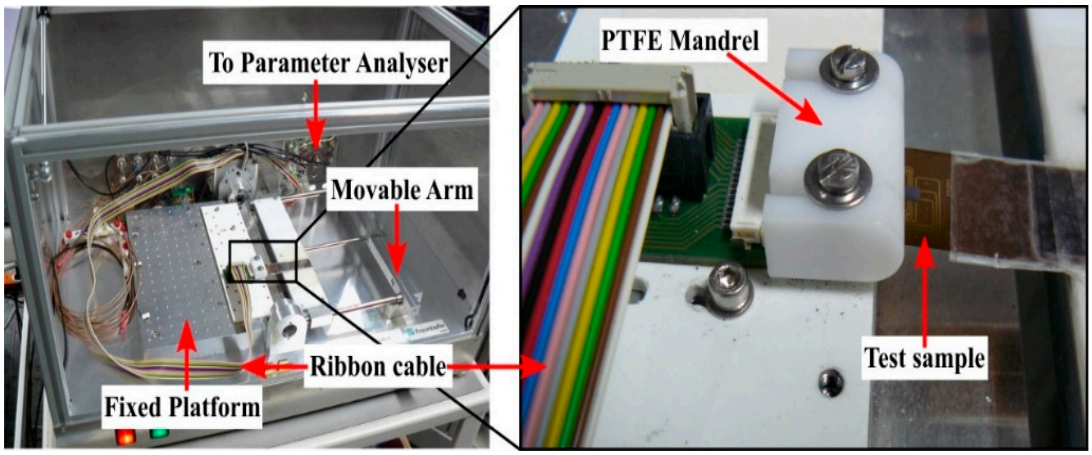


Figure 3. Custom-built test equipment used for performing the dynamic bending tests.

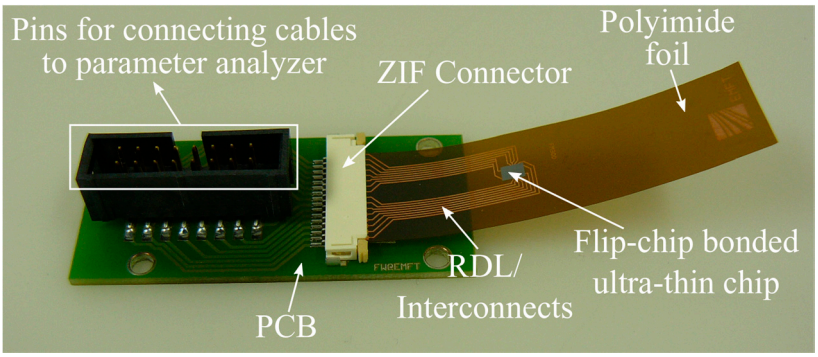
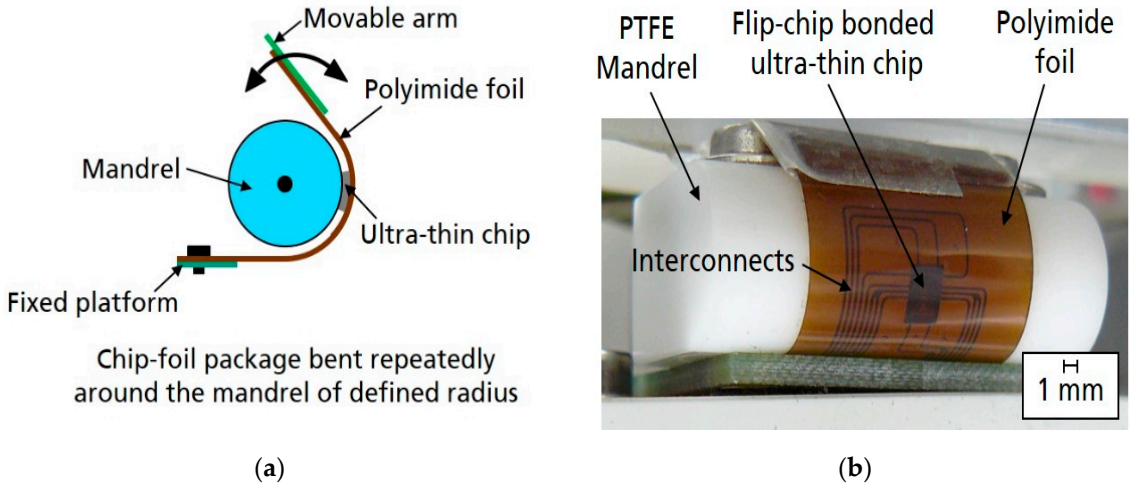


Figure 4. A chip-foil package test sample connected to the PCB via the zero-insertion force (ZIF) connector.

3.2. Experimental Procedure

In this work, repeated bending tests under compressive stress were performed on the samples at a bending radius of 5 mm. During the dynamic bending tests, the samples were placed on the equipment in such a way that one of the samples was attached to the fixed platform while their other end to the movable arm. The tests were performed under laboratory conditions at a temperature of 25 °C and a relative humidity of 38%. The back and forth movement of the movable arm around the PTFE mandrel from 0 to 180° enabled by the stepper motor facilitated the repeated bending of the test samples at a bending radius of 5 mm. Figure 5a,b shows the schematic of the test procedure and a chip-foil package sample bent to 180° around the PTFE mandrel respectively. Since the three investigated metals namely copper, gold and aluminum have different sheet resistance values (Table 1), a relative increase in the daisy chain resistance of the chip-foil package samples was compared up to 20,000 bending cycles (corresponds to 28 bending cycles per day for 2 years). The tests were conducted at a relatively slow bending speed of 13.3 bending cycles per minute and the time required for the completion of 20,000 bending cycles was about 25 h. A 100% relative increase in the daisy chain resistance during the bending tests was defined as the failure criterion.



(**a**) (**b**)

Figure 5. (**a**) Schematic of the test procedure and (**b**) a bent chip-foil package test sample during a test.

Table 1. Material properties of the metals used for fabricating interconnects [47–49].

Metal	Sheet Resistance (mΩ/sq)	Young's Modulus (GPa)	Poisson's Ratio
Copper	64–78	132	0.33
Aluminum	102–110	69	0.33
Gold	189–226	24.2–43.9	0.42

4. Results and Discussion

Dynamic bending tests were performed on a total of 15 chip-foil package samples with five samples per interconnect metal and it was found that none of the samples reached the predefined failure criteria of 100% relative increase in daisy chain resistance. Figure 6 summarizes the results of the tests where the mean values of relative change in daisy chain resistance were plotted after every 5,000 bending cycles for the three sample types. It could be noticed that chip-foil packages with gold interconnects showed the least increase in the resistance followed by aluminum and copper after 20,000 bending cycles. After 20,000 bending cycles, the mean relative increase in resistance for copper, aluminum and gold was 87.6%, 47.38% and 25.12% respectively. The least increase in relative resistance of chip-foil packages with gold interconnects could be directly attributed to the superior flexibility of gold compared to copper and aluminum resulting from the lower Young's Modulus and higher Poisson's ratio of gold.

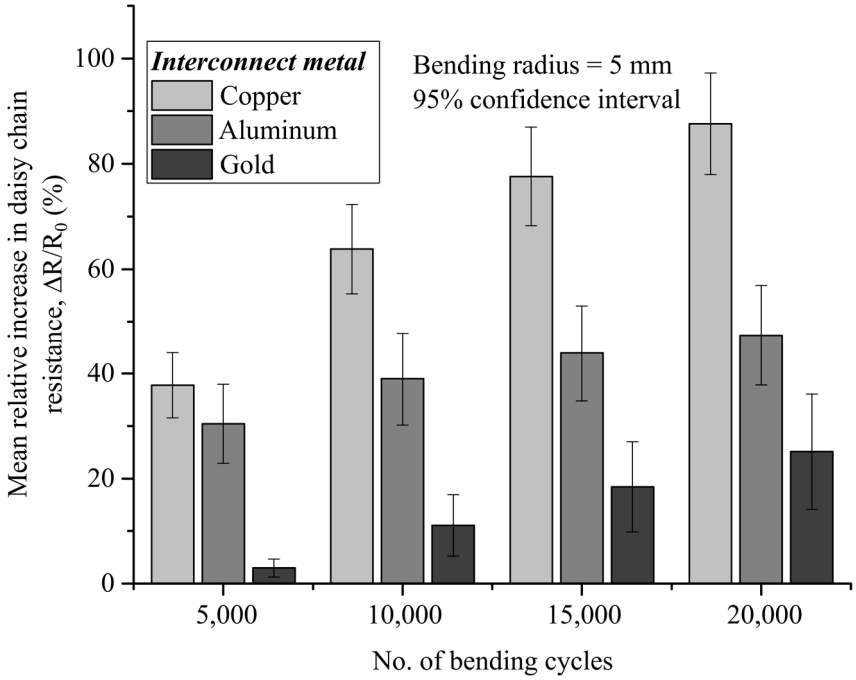


Figure 6. Mean relative change in daisy chain resistance of chip-foil packages with copper, aluminum and gold interconnects. Relative change in daisy chain resistance, $\frac{\Delta R}{R_0} = \frac{(R-R_0)}{R_0} \times 100\%$ where R is the daisy chain resistance at the corresponding bending cycle and R_0 is the initial daisy chain resistance at the start of the bending tests.

4.1. Optical Analysis

After the completion of 20,000 bending cycles, the chip-foil package test samples were inspected with optical as well as scanning electron microscopy. The analyses revealed that the bonded ultra-thin chips were devoid of any cracks or delamination and the increase in resistance during the tests was resulted from the formation of hillocks in the interconnects perpendicular to the direction of bending. Figure 7 shows the hillocks formed on the copper interconnects. Section analysis performed with atomic force microscopy (AFM) revealed that the hillocks had a height of about 150 nm (Figure 8). Similar hillocks were found also on aluminum and gold interconnects (Figures 9 and 10). Several studies indicate that hillocks are created on thin metal layers deposited on foil substrates under repeated bending due to uneven stress distribution arising from thermal and mechanical stresses [50–55]. Various mechanisms such as surface roughening and localized differential stress relaxation occurring in the thin metal layer when subjected to repeated mechanical stress have been reported to induce hillocks in thin metal layers [51–55].

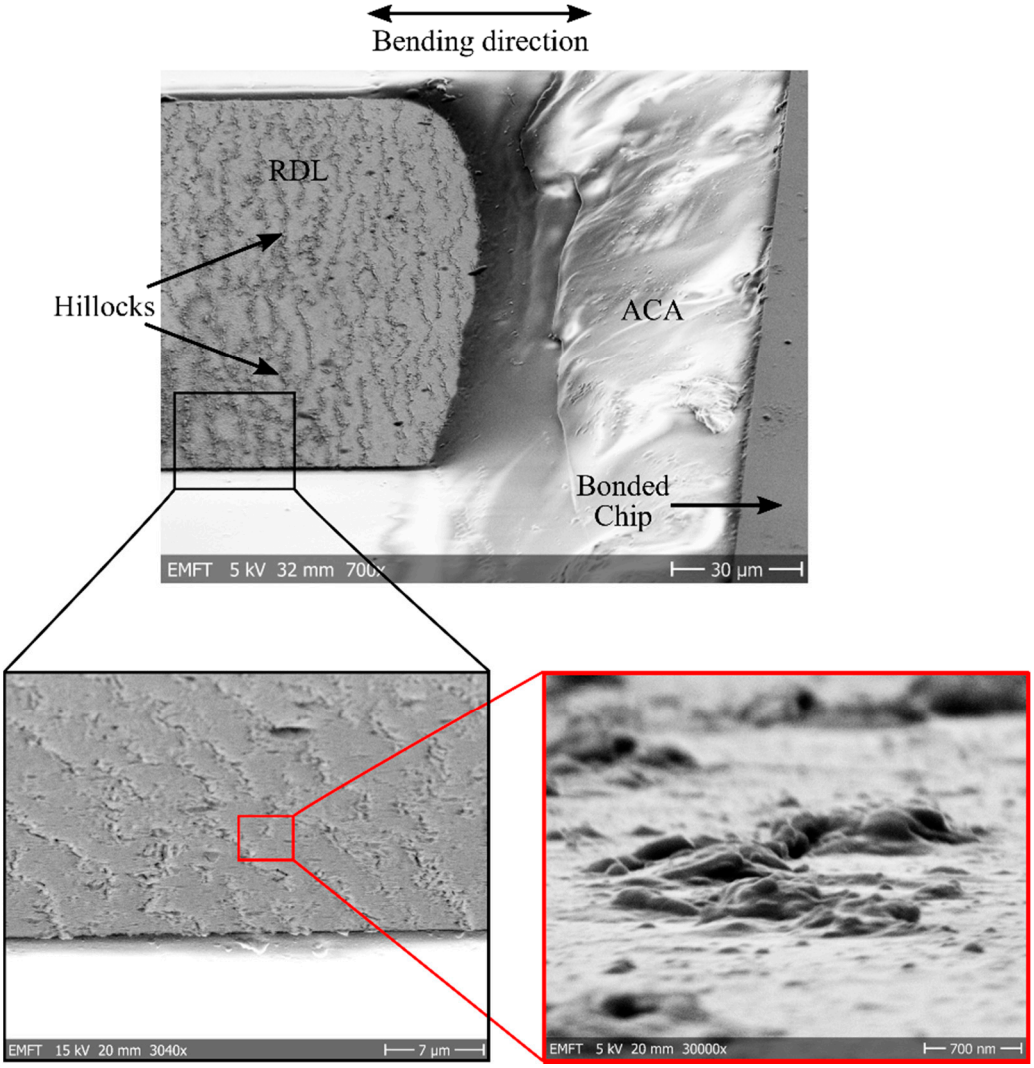


Figure 7. SEM image showing the hillocks created on the copper interconnect after 20,000 bending cycles.

The height of hillocks was found to be almost the same (approximately 150 nm) for all three metals (Figures 8 and 10). Therefore, the difference in the increase in daisy chain resistance could plausibly be attributed to the number of hillocks formed in the interconnects since the number of hillocks found on copper interconnects was comparatively higher than the number of hillocks on aluminum and gold interconnects (Figures 7 and 9). Lee et al. have observed that the formation of dislocations and vacancies in thin copper films during bending results in resistance increase [56]. Similar vacancies and dislocations plausibly formed underneath the hillocks could act as electron scattering centers thus increasing the daisy chain resistance. This hypothesis could conceivably be exemplified by correlating the daisy chain resistance increase and the number of hillocks formed in the interconnects. Copper interconnects with the relatively higher number of hillocks exhibited the highest increase in daisy chain resistance whereas gold interconnects with the relatively lower number of hillocks demonstrated the lowest increase in daisy chain resistance. Hence, it could arguably be concluded that the number of hillocks formed on the interconnects is directly proportional to the increase in daisy chain resistance. However, further in-depth investigations are necessary to support this hypothesis. Besides, extensive analysis to determine the exact mechanism behind the formation of hillocks observed in this work is required and this will be comprehensively analyzed in a separate study.

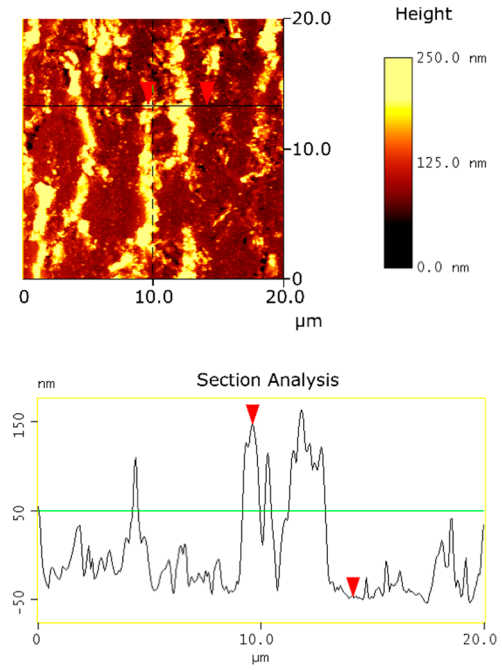
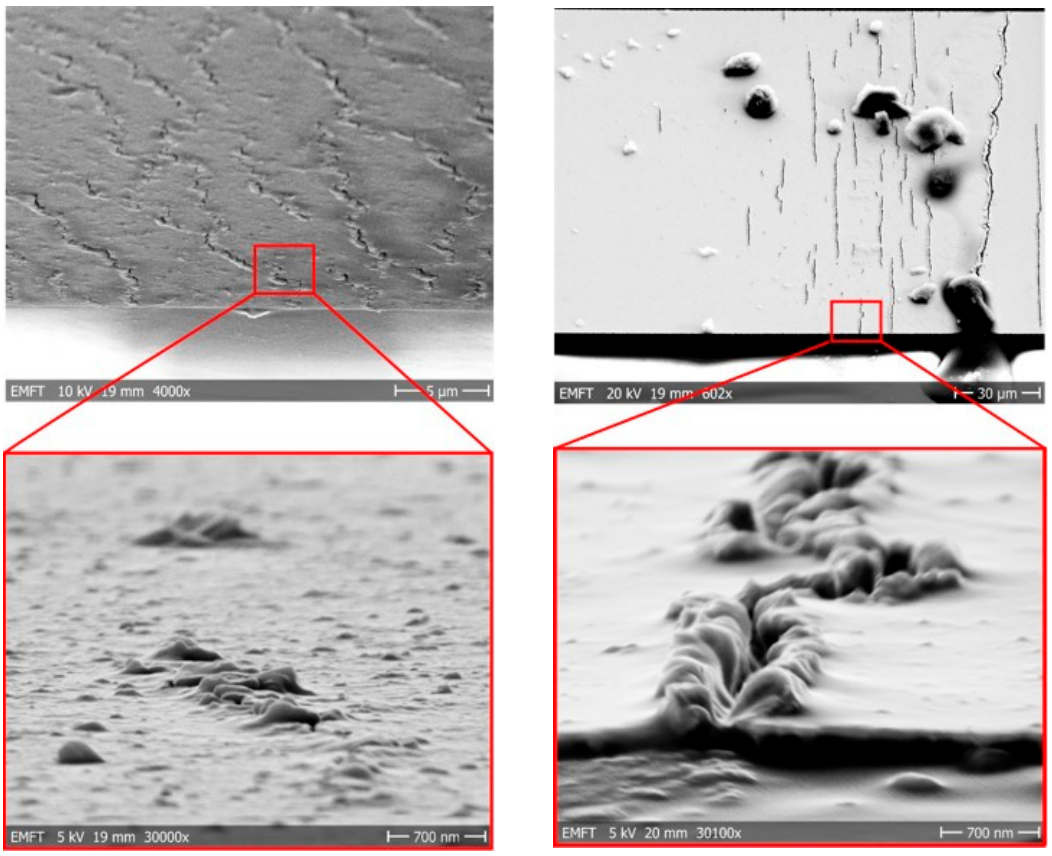


Figure 8. Atomic force microscopy (AFM) section analysis of copper interconnect revealing the height of the hillocks.



(**a**) (**b**)

Figure 9. SEM images presenting the hillocks formed on (**a**) aluminum and (**b**) gold interconnects after 20,000 bending cycles.

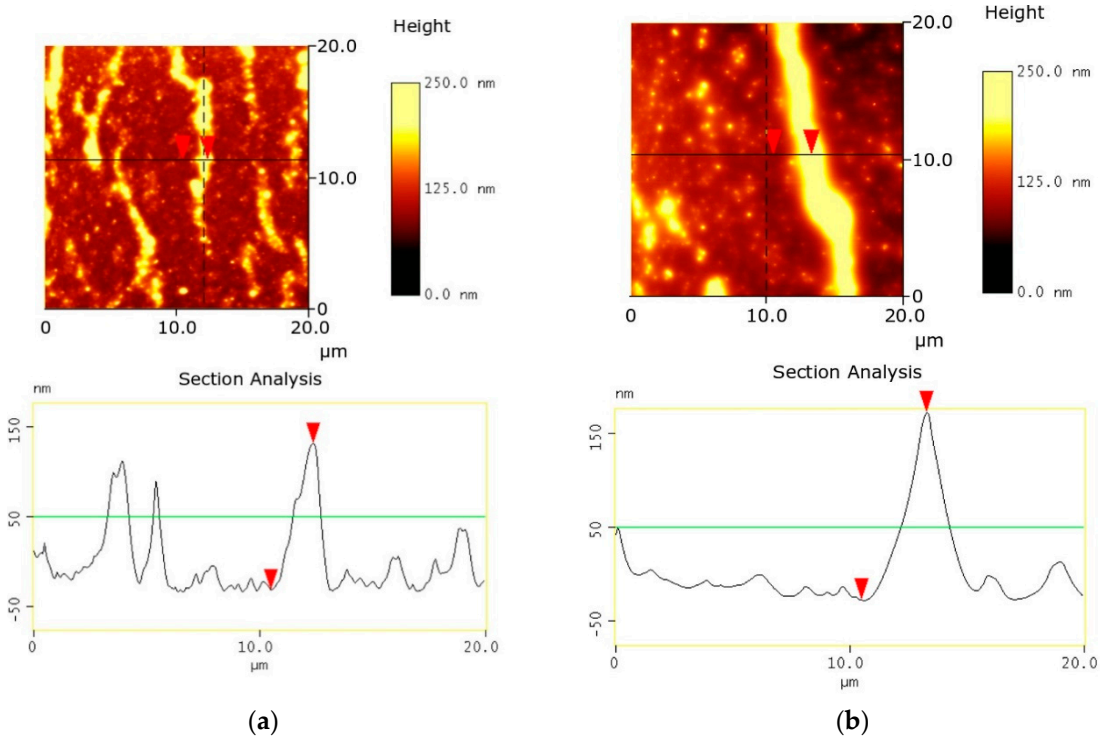


Figure 10. AFM section analysis of (**a**) aluminum and (**b**) gold interconnects after 20,000 bending cycles showing the height of the hillocks.

4.2. Choice of Metal for Fabrication of Interconnects

The results of the dynamic bending tests showed that chip-foil packages with gold interconnects are the most flexible followed by aluminum and copper implying that gold could be the favored metal for fabricating interconnects for FHE. However, the higher sheet resistance together with the higher cost of gold compared to copper and aluminum indicate that aluminum could be preferred over gold owing to the decent electrical conductivity as well as good dynamic bending reliability of aluminum.

5. Conclusions

Dynamic bending tests conducted on chip-foil packages revealed a strong influence of flexibility of the metals constituting the interconnects. Under repeated bending, the daisy chain resistance of the chip-foil packages as the bending cycles progressed. Optical analysis indicated that the increase in daisy chain resistance could plausibly be attributed to the formation and the number of hillocks formed in the interconnects. Test results showed that the chip-foil packages with gold interconnects endured the 20,000 repeated bending cycles at least three times more than the chip-foil packages with copper interconnects with a mean increase in resistance of 25.2% compared to 87.6% mean increase for copper interconnects and about 2 times more than the chip-foil package with aluminum interconnects (47.38% mean increase in resistance). However, the higher sheet resistance as well as higher cost of gold indicate that aluminum could instead be favored for fabricating the interconnects due to the decent electrical conductivity and good dynamic bending reliability apart from the relatively lower cost of aluminum.

In the next step, we intend to conduct an in-depth analysis to understand the exact mechanism behind the formation of hillocks. In particular, the influence of the adhesion layer and the foil substrate on the formation of hillocks will be investigated. Afterwards, measures to avoid the formation of hillocks must be devised to improve the dynamic bending reliability of chip-foil packages. Besides, the effect of repeated tensile stress on the dynamic bending reliability of chip-foil packages will also be studied in detail. Furthermore, the reliability of chip-foil packages under torsional bending.

Finally, environmental tests to examine the corrosion resistance of the chip-foil packages are pivotal for fabricating reliable FHE systems.

Author Contributions: Conceptualization, methodology and investigations, N.P.; sample preparation: W.H., A.D.; manuscript writing, N.P.; manuscript review and editing, C.L., C.K., K.B.; supervision, C.L., C.K., K.B.; funding, C.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research was executed within Fraunhofer internal projects and has not received external funding.

Acknowledgments: The authors would like to thank Robert Faul, Martin König, Dieter Bollmann, Sabine Scherbaum and Dennise Linke for their support in preparation of the samples that resulted in the fruition of this work.

Conflicts of Interest: The authors declare no conflict of interest.

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