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# Comparative Evaluation of Wide-Range Soft-Switching PWM Full-Bridge Modular Multilevel DC-DC Converters 

Jingwen Chen ${ }^{\text {( }, ~ X i a o f e i ~ L i, ~ H o n g s h e ~ D a n g ~ * ~ a n d ~ Y o n g ~ S h i ~}$<br>School of Electrical and Control Engineering, Shaanxi University of Science and Technology, Xi'an 710021, China; chenjw@sust.edu.cn (J.C.); lxiaofei1214@163.com (X.L); shiyong@sust.edu.cn (Y.S)<br>* Correspondence: danghs@sust.edu.cn

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#### Abstract

This paper discusses some wide-range soft-switching full-bridge (FB) modular multilevel dc-dc converters (MMDCs), and a comparative evaluation of these FB MMDCs is also presented. The discussed topologies have all merits belonging to conventional FB MMDCs, e.g., smaller voltage stress on the primary switches, no added primary clamping devices and modular primary structure. In addition, the primary switches in each converter can obtain zero-voltage switching (ZVS) or zero-current switching (ZCS) in a wide load range. Two presented topologies are selected as examples to discuss in detail. The proposed FB MMDCs are assessed and evaluated based on performance, components and topology structure indices, such as soft switching characteristics, current stress, power loss distribution, number of added devices, complexity of structure and added cost. Experimental results are also included to verify the feasibility and advantages of the new topologies.


Keywords: full bridge (FB); modular multilevel dc-dc converters (MMDCs); zero-voltage switching (ZVS); zero-current switching (ZCS)

## 1. Introduction

With the rapid development of smart grid systems, dc-based distributed power systems and micro grids attract more and more attention due to some clearly good features, e.g., high power transfer efficiency, low system cost, high system stability and easy system control [1,2]. Commonly, the input voltage of these dc interfaces is very high to obtain optimum system performance, which makes high input voltage and high frequency isolated dc-dc converters become hot and causes challenging issues in power electronics. In the high voltage applications, how to reduce the voltage stress on the primary switches is a key point, and several methods can be used to solve this problem. The first way is to connect the power switches in series directly, but this method is seldom used in the high frequency applications due to the serious static and dynamic voltage balance problems [3]. Second, three-level (TL) dc-dc converters (TLDCs) are suitable topologies for high voltage applications due to only half the input voltage stress on the primary switches [4]. The first diode-clamped TLDC was proposed in 1992 [4], and then, many other efforts have been made on this topic, e.g., novel topologies and corresponding control strategies [4-11], wide range soft switching solutions [12-16] and reduced filter size solutions [16-19]. Finally, modular multilevel dc-dc converters (MMDCs) can also be used in high voltage applications [20]. MMDCs are built of modular cells with input series and output series or parallel connected, and can be extended to higher voltage levels easily due to their modular structure. Many TLDCs, e.g., diode-clamped TLDCs, can also be extended to a higher voltage level. But, as mentioned in [20], the number of achievable voltage levels is limited due to not only the dynamic voltage unbalance problem but also the complexity of the primary circuit structure
and modulation strategy. Therefore, MMDCs may be a better choice for applications with super high input voltage, i.e., 1400 V or higher. A half bridge (HB) MMDC was proposed and discussed in [4], which is built of two-level HB modules. Several HB MMDCs for higher input voltage ratings have been proposed [21,22]. In [23], an FB MMDC was proposed, which is composed of two input series and output series connected two-level FB cells. Compared to HB MMDCs, FB MMDCs are more suitable for high input and large power industry applications due to the lower VA rating of the primary components, more modular structure and easy control. A number of new FB MMDCs were proposed and discussed in [20,23-26]. A new FB MMDC with auto-balance ability among series connected primary modules was proposed in [20]. Controlling strategies for output parallel-connected FB MMDCs were analyzed in [27-29]. However, improvements are still required. In the high voltage applications, soft switching performance of the primary switches is a key point to ensure higher efficiency due to the switching loss increases squared with the input voltage. Fortunately, the switching scheme of FB MMDCs is quite similar to that of the two-level phase shift (PS) FB dc-dc converter. Hence, common wide-range soft-switching solutions for conventional two-level PS FB dc-dc converters can be directly used in FB MMDCs. But, the system performance, structure complexity and added cost of different solutions for FB MMDCs are quite different because more primary cells are involved. Therefore, wide-range soft-switching FB MMDCs and a comparative evaluation of these solutions are still interesting subjects.

In this paper, some new wide-range soft-switching FB MMDCs are discussed and compared.
The main contributions of this paper are:
(1) Based on conventional FB MMDC, this paper proposes eight novel soft-switching solutions;
(2) Through comparative study of them, the two most promising switching solutions are found;
(3) Converter losses, efficiency and costs of the two solutions are analyzed and tested for verification.

This paper is organized as follows. In Section 2, the circuits of the presented converters are described. The operation principles and relevant analysis of an improved zero-voltage switching (IZVS) FB MMDC are provided in Section 3. The operation principles and relevant analysis of a zero-voltage and zero-current switching (ZVZCS) FB MMDC are discussed in Section 4. A comparative evaluation of the presented converters is provided in Section 5. In Section 6, experimental results are presented and analyzed. Finally, some brief conclusions are given.

## 2. Wide-Range Soft-Switching PWM FB MMDCs

Figure 1 illustrates a conventional FB MMDC, which is built of two two-level FB cells. The switches in each cell are switched in PS mode. Thus, eight switches in Figure 1 can also be divided into two groups, i.e., the leading and lagging switches. The lagging switches will face more difficulty to obtain ZVS because only the energy stored in the leakage inductances can be used.


Figure 1. Conventional full-bridge (FB) modular multilevel dc-dc converter (MMDC).

As the switching scheme of Figure 1 is quite similar to that of a two-level PS FB dc-dc converter, common wide-range soft-switching solutions for two-level PS FB dc-dc converters can also be used [30-37]. These solutions can be concluded into two types: IZVS and ZVZCS. IZVS converters extend the ZVS range of the lagging switches by increasing either the value of the primary equivalent inductance or the currents of the switches [30-34]. In the ZVZCS converters, the lagging switches can realize ZCS by resetting the primary current during the free-wheeling mode. According to the different reset voltage generated methods, the ZVZCS converters can be further divided into two kinds, which are primary reset and secondary reset ZVZCS converters [35-37]. Generally, ZVZCS solutions are more suitable for the converters with IGBTs because of the large tailing current during the switching commutation.

### 2.1. IZVS FB MMDCs

Figure 2 shows four IZVS FB MMDCs. In IZVS_CD, the upper FB primary cell is built of the switches S1 to S4, the primary coil T1p, Lr1, Dcl1, Dcl2 and the blocking capacitor CBL1; another primary cell is comprised of the switches S5 to S8, the primary coil T2p, Lr2, Dcl3, Dcl4 and the blocking capacitor CBL2. Lr1 and Lr2 are added to enlarge ZVS range of the lagging switches. Dcl1 to Dcl4 are used to eliminate the oscillation and clamp the secondary rectified voltage reflected to the primary side. The power transformer is built of two independent magnetic cores, two primary coils and two common secondary coils. Each primary coil is wired around an independent magnetic core; while the common secondary coils enclose both cores. Cin1 and Cin2 are the input capacitors with the same value, and these capacitors share the input voltage evenly during the operation stages, i.e., $V_{\mathrm{Cin} 1}=V_{\mathrm{Cin} 2}=V_{\mathrm{in}} / 2$. Llk1 and Llk2 are leakage inductances of T1p and T2p. Do1 and Do2 are the rectifier diodes, and the output filter is built of Lo and Co. Ro is the load resistor.


Figure 2. Improved zero-voltage switching (IZVS) FB MMDCs: (a) IZVS with clamped diode (IZVS_CD); (b) IZVS with commutation auxiliary circuit (IZVS_CAC); (c) IZVS with small magnetizing inductance (IZVS_SMI); (d) IZVS with secondary modulation method (IZVS_SMM).

In IZVS_CAC, two commutation auxiliary circuits (CACs) are added to enlarge the ZVS range of the lagging switches. The secondary rectifier of IZVS_CAC is identical to that of IZVS_CD. The configuration of IZVS_SMI is quite similar to that of Figure 1. However, the magnetic currents of the transformer in IZVS_SMI are increased to provide more resonant energy. The structure of
the power transformers in IZVS_CAC and IZVS_SMI is identical to that of IZVS_CD. IZVS_SMM shows a secondary modulated FB MMDC. The primary structure of IZVS_SMM is identical to that of IZVS_SMI, and the magnetizing currents are also increased to help the ZVS of the primary switches. The transformer in IZVS_SMM has two primary coils and two secondary coils. Do3 to Do6 are the rectifier diodes. Sse1 and Sse2 are two added secondary switches. The output filter is built of Lo and Co. Ro is the load resistor.

### 2.2. ZVZCS FB MMDCs

Figure 3 depicts four ZVZCS FB MMDCs. IZVZCS_DCF is a primary current reset ZVZCS converter with two cut-off diodes in each FB cell. CBL1 and CBL2 are designed to a specific value to reset the primary currents. D3, D4, D7 and D8 are used to block the reverse primary currents. The secondary circuit of IZVZCS_DCF equals that of IZVS_CD. IZVZCS_SAC\&CAC and IZVZCS_SRC\&CAC illustrate two secondary reset ZVZCS FB MMDCs. In IZVZCS_SAC\&CAC, Sse and Cse are added to conventional FB MMDC to reset the primary currents; while the secondary reset circuit in IZVZCS_SRC\&CAC has the same function, which is composed of Dse1, Dse2 and Cse. In IZVZCS_SI, CBL1 and CBL2 are designed to a specific value to reset the primary currents, and two saturable inductors, i.e., Lr1 and Lr2, are used to limit the reverse primary currents. The structure of the power transformers in Figure 3 is identical to that of IZVS_CD.


Figure 3. Improved zero-voltage and zero-current switching (IZVZCS) FB MMDCs: (a) IZVZCS with diode cutting-off (IZVZCS_DCF); (b) IZVZCS with secondary active clamping and commutation auxiliary circuit (IZVZCS_SAC\&CAC); (c) IZVZCS with secondary reactive clamping and commutation auxiliary circuit (IZVZCS_SRC\&CAC); (d) IZVZCS with saturable inductance (IZVZCS_SI).

## 3. IZVS FB MMDC with Secondary Modulated

In order to simplify the description, the operation principle and characteristics of IZVS_CD, IZVS_CAC and IZVS_SMI is not presented here, and corresponding information can be found in [30-33]. The IZVS_SMM is selected as an example to analyze in detail in this part.

### 3.1. Operation Principle

Key waveforms of IZVS_SMM are shown in Figure 4. There are six operation stages during the whole switching cycle, and the operation stages in the first half switching cycle are illustrated in Figure 5. Before the analysis, some assumptions are set to simplify the explanation: all the components in the topology are ideal; Cin1 and Cin2 are large enough to be considered as voltage sources valued $V_{\text {in }} / 2$, and the voltage ripple on them can be neglected; CBL1 and CBL2 are large enough, and the voltage ripple on them can be neglected; $L_{\mathrm{m} 1}=L_{\mathrm{m} 2}=L_{\mathrm{m}} ; L_{\mathrm{L} 1 \mathrm{~K} 1}=L_{\mathrm{L} 1 \mathrm{~K} 2}=L_{1 \mathrm{~K}} ; I \mathrm{~m}$ is the peak value of the magnetizing currents; output filter and load are replaced by a constant current source Io; $\mathrm{k}_{\mathrm{T} 1}$ and $\mathrm{k}_{\mathrm{T} 2}$ are the turn ratios $k_{\mathrm{T}}^{\prime}=\left(k_{\mathrm{T} 1} \times k_{\mathrm{T} 2}\right) /\left(k_{\mathrm{T} 1}+k_{\mathrm{T} 2}\right)$. The output capacitance of each switch is identical and represented as $\operatorname{Cos}$ in the following equations.


Figure 4. Key waveforms of IZVS_SMM.
Stage 1 [Figure 5a]: before $t 0$, the circuit is operated in steady condition. Input source powers the load. S1, S4, S5 and S8 are on; Do2 is conducted; Sse 2 is also on, and the current flowing through Sse2 is zero due to Do4 is off. $v_{\mathrm{BC}}=v_{\mathrm{DE}}=V_{\mathrm{in}} / 2 ; v_{\text {rect }}=V_{\mathrm{in}} / k_{\mathrm{T} 2} ; i_{1 \mathrm{p}}=i_{2 \mathrm{p}}=I_{\mathrm{o}} / k_{\mathrm{T} 2} ; i_{\mathrm{L} 1 \mathrm{k} 1}=i_{1 \mathrm{p}}+i_{\mathrm{m} 1}$; $i_{\mathrm{L} 1 \mathrm{k} 2}=i_{2 \mathrm{p}}+i_{\mathrm{m} 2} ; i \mathrm{~m} 1$ and $i \mathrm{~m} 2$ increase with time linearly, and the slope is

$$
\begin{equation*}
\frac{d i_{\mathrm{m} 1}}{d t}=\frac{d i_{\mathrm{m} 2}}{d t}=\frac{V_{\mathrm{in}}}{2 L_{\mathrm{m}}} \tag{1}
\end{equation*}
$$

Stage 2 [Figure $5 \mathrm{~b}, t 0-t 1$ ]: At $t 0, \mathrm{Sse} 2$ is turned off at zero-current. Primary side powers the load. $v_{\mathrm{BC}}=v_{\mathrm{DE}}=V_{\mathrm{in}} / 2 ; v_{\text {rect }}=V_{\mathrm{in}} / k_{\mathrm{T} 2} ; i_{1 \mathrm{p}}=i_{2 \mathrm{p}}=I_{\mathrm{o}} / k_{\mathrm{T} 2} ; i_{\mathrm{L} 1 \mathrm{k} 1}=i_{1 \mathrm{p}}+i_{\mathrm{m} 1} ; i_{\mathrm{L} 1 \mathrm{k} 2}=i_{2 \mathrm{p}}+i_{\mathrm{m} 2} ; i \mathrm{~m} 1$ and im2 keep increasing.

Stage 3 [Figure $5 \mathrm{c}, t 1-t 2$ ]: At $t 1$, Sse1 is turned on; Do1 is conducted and Do2 is off. Primary powers the load. $v_{\mathrm{BC}}=v_{\mathrm{DE}}=V_{\mathrm{in}} / 2 ; v_{\text {rect }}=V_{\mathrm{in}} / 2 k_{\mathrm{T}}^{\prime} ; i_{1 \mathrm{p}}=i_{2 \mathrm{p}}=I_{\mathrm{o}} / k_{\mathrm{T}}{ }^{\prime} ; i_{\mathrm{L} 1 \mathrm{k} 1}=i_{1 \mathrm{p}}+i_{\mathrm{m} 1} ; i_{\mathrm{L} 1 \mathrm{k} 2}=i_{2 \mathrm{p}}+i_{\mathrm{m} 2} ;$ im1 and im2 increase with time linearly.


Figure 5. Operation stages of IZVS_SMM: (a) stage 1; (b) stage 2; (c) stage 3; (d) stage 4; (e) stage 5; (f) stage 6 .

Stage 4 [Figure $5 \mathrm{~d}, \mathrm{t2}-\mathrm{t} 4$ ]: At $t 2, \mathrm{~S} 1, \mathrm{~S} 4, \mathrm{~S} 5$ and S 8 are simultaneously turned off at zero-voltage due to the existence of $\mathrm{C} 1, \mathrm{C} 4, \mathrm{C} 5$ and $\mathrm{C} 8 ; i \mathrm{Llk} 1$ charges C 1 and C 4 , and discharges C 2 and C 3 linearly with time; $i \mathrm{Llk} 2$ charges C 5 and C8, and discharges C6 and C7 linearly with time. During this interval, $i m 1$ and $i m 2$ reach their peak value Im and keep constant. Before $v_{\text {rect }}>0$, the energy stored in the output inductor can still be used to charge or discharge the output capacitance of each primary switch. When vrect is zero, one half of the final voltage on each primary switch has been charged or discharged [34]. Thus, less resonant energy is required to obtain ZVS for the primary switches, and this is the advantage of IZVS_SMM. After $t 3$, the circuit will be operated into the free-wheeling mode. iLlk1 charges C1 and C4, and discharges C2 and C3 linearly with time; iLlk2 charges C5 and C8, and discharges C 6 and C 7 linearly with time. This stage ends until $v_{\mathrm{C} 1}=v_{\mathrm{C} 4}=v_{\mathrm{C} 5}=v_{\mathrm{C} 8}=V_{\text {in }} / 2$ and $v_{\mathrm{C} 2}=v_{\mathrm{C} 3}=v_{\mathrm{C} 6}=v_{\mathrm{C} 7}=0$.

Stage 5 [Figure 5e, t4-t5]: At $t 4, \mathrm{D} 2, \mathrm{D} 3, \mathrm{D} 6$ and D7 conduct naturally. The circuit operates in the free-wheeling mode; $i \mathrm{Llk} 1$ and $i \mathrm{Llk} 2$ decrease due to negative voltage applied to the terminals of Llk1 and Llk2; during this stage, S2, S3, S6 and S7 must be turned on to achieve ZVS. According to Figure 4, S2, S3, S6 and S7 are turned on at $t 5$.

Stage 6 [Figure 5f, t5-t6]: At $t 5, \mathrm{~S} 2, \mathrm{~S} 3, \mathrm{~S} 6$ and S7 are switched on; $i 1 \mathrm{p}$ and $i 2 \mathrm{p}$ increase in the inverse direction. When these currents reach $-I_{\mathrm{o}} / k_{\mathrm{T} 2}$, the free-wheeling mode is over. Primary powers load. After $t 6, v_{\mathrm{BC}}=v_{\mathrm{DE}}=-V_{\text {in }} / 2 ; v_{\text {rect }}=-V_{\mathrm{in}} / k_{\mathrm{T} 2} ; i_{1 \mathrm{p}}=i_{2 \mathrm{p}}=-I_{\mathrm{o}} / k_{\mathrm{T} 2} ; i \mathrm{Llk} 1$ equals the sum of $i 1 \mathrm{p}$ and $i \mathrm{~m} 1 ; i \operatorname{Llk} 2$ equals the sum of $i 2 \mathrm{p}$ and $i \mathrm{~m} 2 ; i \mathrm{~m} 1$ and $i \mathrm{~m} 2$ decrease with time linearly, and the slope is determined by (1). The current flowing through Sse1 is zero due to Do1 is off. After stage 6, the circuit will be operated in the second half switching cycle.

### 3.2. Soft Start

During the soft-start operation, the IZVS_SMM can be treated as a conventional FB MMDC in Figure 1. Two secondary switches are off, and four primary switches in each FB module are switched in PS mode. The output voltage can be regulated down to zero by increasing the phase angle among the primary switches. Detailed operation principle about this procedure can be found in $[23,24]$.

### 3.3. ZVS Condition of The Primary Switches

With proper design of $i 1 \mathrm{~m}$ and $i 2 \mathrm{~m}$, all primary switches can obtain ZVS down to 0 load currents. S2 and S3 in the upper module are selected to describe as an example. Figure 5d shows the equivalent circuit of this procedure. Before vrect decays to zero, the load current can still be used to charge or discharge corresponding capacitors. As discussed above, $50 \%$ of the final voltage across C 1 to C 4 has been discharged or charged before vrect decays to zero. Thus, following equation should be fitted to obtain ZVS.

$$
\begin{equation*}
\frac{1}{2} L_{\mathrm{lk}} I_{\mathrm{m}}^{2} \geq 2 \times C_{\mathrm{os}}\left(\frac{V_{\mathrm{in}}}{4}\right)^{2} \tag{2}
\end{equation*}
$$

The required Im is

$$
\begin{equation*}
I_{\mathrm{m}} \geq \frac{V_{\mathrm{in}}}{2} \sqrt{\frac{\mathrm{C}_{\mathrm{os}}}{L_{\mathrm{lk}}}} \tag{3}
\end{equation*}
$$

The peak to peak value of $i m$ is

$$
\begin{equation*}
\Delta i_{\mathrm{m}}=\frac{V_{\mathrm{in}} T_{\mathrm{s}}}{2 L_{\mathrm{m}}}=2 I_{\mathrm{m}} \tag{4}
\end{equation*}
$$

Thus, Im is

$$
\begin{equation*}
I_{\mathrm{m}}=\frac{V_{\mathrm{in}} T_{\mathrm{s}}}{4 L_{\mathrm{m}}} \tag{5}
\end{equation*}
$$

Substituting (5) into (3) yields

$$
\begin{equation*}
L_{\mathrm{m}} \leq \frac{T_{\mathrm{s}}}{2} \sqrt{\frac{L_{\mathrm{lk}}}{\mathrm{C}_{\mathrm{os}}}} \tag{6}
\end{equation*}
$$

Therefore, S2 and S3 can obtain ZVS down to zero load current with a specific value of Lm decided by (6).

### 3.4. ZCS Condition of The Secondary Switches

As proved in Figures 4 and 5, all secondary switches can obtain ZCS independent of the load current. Sse2 is selected to describe as an example. As shown in Figure 5a, Sse2 is on in this stage. But, the current flowing through Sse 2 is zero due to the reverse voltage applied to Do4. As shown in Figure 5b, Sse2 is switched off at zero current. Therefore, the switching loss of the secondary switches can be minimized.

### 3.5. Turn Ratios

The output is regulated by the phase angle among the primary and secondary switches. The turn ratios of IZVS_SMM should be designed according to the input voltage range. At maximum input voltage, the phase angle between S1 and Sse1 is zero; primary powers the load through Ts2. With decreasing of the input voltage, the phase angle between S 1 and Sse 1 is increased, and primary powers the load through both Ts 1 and Ts 2 . Hence, $k \mathrm{~T} 2$ is

$$
\begin{equation*}
k_{\mathrm{T} 2} \leq \frac{V_{\mathrm{inmax}}}{V_{\mathrm{o}}} \tag{7}
\end{equation*}
$$

And $k \mathrm{~T} 1$ can be computed by

$$
\begin{equation*}
\frac{k_{\mathrm{T} 1} k_{\mathrm{T} 2}}{k_{\mathrm{T} 1}+k_{\mathrm{T} 2}}=\frac{V_{\mathrm{inmin}}}{V_{\mathrm{o}}} \tag{8}
\end{equation*}
$$

As for a converter with 100 to 300 V input and 50 V output (used in the prototype), $k \mathrm{~T} 2$ can be decided by (7) and the value is 16 ; according to $(8), k_{\mathrm{T} 1}=48$.

### 3.6. Duty Ratio Loss

The time between $t 5$ and $t 6$ is defined as duty ratio loss time, and corresponding states are plotted in Figures 5e and 5f. The primary side currents are

$$
\begin{equation*}
i_{\mathrm{kp}}=\frac{I_{\mathrm{o}}}{k_{\mathrm{T}}^{\prime}}-\frac{V_{\mathrm{in}}}{2 L_{\mathrm{lk}}} \Delta t_{56}, k=1,2 \tag{9}
\end{equation*}
$$

when $i_{\mathrm{kp}}=-I_{\mathrm{o}} / k_{\mathrm{T} 2}, k=1,2$, the free-wheeling mode is finished. The time of this interval is

$$
\begin{equation*}
\Delta t_{56}=\frac{2 I_{\mathrm{o}} L_{\mathrm{lk}}}{V_{\mathrm{in}}}\left(\frac{k_{\mathrm{T}}^{\prime}+k_{\mathrm{T} 2}}{k_{\mathrm{T}}^{\prime} k_{\mathrm{T} 2}}\right) \tag{10}
\end{equation*}
$$

The duty ratio loss is

$$
\begin{equation*}
\Delta D=\frac{\Delta t_{56}}{T_{\mathrm{s}} / 2}=\frac{4 I_{\mathrm{o}} L_{\mathrm{lk}} f_{\mathrm{s}}}{V_{\mathrm{in}}}\left(\frac{k_{\mathrm{T}}^{\prime}+k_{\mathrm{T} 2}}{k_{\mathrm{T}}^{\prime} k_{\mathrm{T} 2}}\right) \tag{11}
\end{equation*}
$$

### 3.7. Reduced Filter Size

The reduction of the output inductance with TL secondary rectified voltage waveform has been discussed in [16-19]. According to these references, the required output inductance of the converters with TL secondary rectified voltage waveform is about one-third of that of conventional two-level converters. Therefore, the volume of the output filter in the IZVS_SMM can be significantly reduced.

## 4. ZVZCS FB MMDC with Secondary Active Reset

The IZVZCS_SAC\&CAC. is selected as an example to analyze in detail in this part. In order to simplify the description, the operation principle and characteristics of IZVZCS_DCF, IZVZCS_SRC\&CAC and IZVZCS_SI are not presented here, and detailed information can be found in $[35,36$ ] and [37].

### 4.1. Operation Principle

Key waveforms of IZVZCS_SAC\&CAC are provided in Figure 6.
There are 12 operation stages in each switching cycle, and eight switching stages in the first half switching cycle are provided in Figure 7. Before the analysis, some assumptions are set to simplify the explanation: all the components in the topology are ideal; the voltage ripple on Cin1 and Cin2 can be neglected; $L_{\mathrm{L} 1 \mathrm{~K} 1}=L_{\mathrm{L} 1 \mathrm{~K} 2}=L_{1 \mathrm{~K}} ; k \mathrm{~T}$ is the turn ratio; the output filter and load are replaced by a constant current source Io. The output capacitance of each primary switch is identical and represented as Cos in the following equations.

Stage 1 [Figure 7a, $t 0-t 1$ ]: At $t 0$, primary powers the load. $\mathrm{S} 1, \mathrm{~S} 4, \mathrm{~S} 5$ and S 8 are on; Do1 is conducted while Do2 is off. The secondary rectified voltage is clamped by Cse through the anti-parallel diode of Sse. iLlk1 and $i \mathrm{Llk} 2$ are

$$
\begin{equation*}
i_{\mathrm{L} 1 \mathrm{k} 1}=i_{\mathrm{L} 1 \mathrm{k} 2}=\frac{1}{L_{\mathrm{lk}}}\left(\frac{V_{\mathrm{in}}}{2}-k_{\mathrm{T}} v_{\mathrm{Cse}}\right) t \tag{12}
\end{equation*}
$$

The current of the clamping capacitor Cse is

$$
\begin{equation*}
i_{\mathrm{Cse}}=k_{\mathrm{T}} i_{\mathrm{L} 1 \mathrm{k} 1}-I_{\mathrm{o}} \tag{13}
\end{equation*}
$$

This stage ends until $i_{\text {Cse }}$ is 0 .

Stage 2 [Figure $7 \mathrm{~b}, t 1-t 2$ ]: At $t 1$, the anti-parallel diode of Sse is turned off; primary powers the load. S1, S4, S5 and S8 are on; Do1 is conducted while Do2 is off. $i_{\mathrm{L} 1 \mathrm{k} 1}=i_{\mathrm{L} 1 \mathrm{k} 2}=I_{\mathrm{o}} / k_{\mathrm{T}} ; v_{\text {rect }}=V_{\mathrm{in}} / k_{\mathrm{T}}$.

Stage 3 [Figure 7c, $t 2-t 3$ ]: At $t 2, \mathrm{~S} 1$ and S 5 are turned off at zero-voltage due to the existence of D1 and D5. iLlk1 charges C1 and discharges C2 linearly with time, and iLlk2 charges C5 and discharges C6 linearly with time, the voltage of $B$ is

$$
\begin{equation*}
v_{\mathrm{B}}(t)=V_{\mathrm{in}}-\frac{I_{\mathrm{o}}}{k_{\mathrm{T}}} \frac{t}{2 C_{\mathrm{os}}} \tag{14}
\end{equation*}
$$

And the voltage of $D$ is

$$
\begin{equation*}
v_{\mathrm{D}}(t)=\frac{V_{\mathrm{in}}}{2}-\frac{I_{\mathrm{o}}}{k_{\mathrm{T}}} \frac{t}{2 C_{\mathrm{os}}} \tag{15}
\end{equation*}
$$

The time of this stage is

$$
\begin{equation*}
T_{32}=\frac{V_{\mathrm{in}} C_{\mathrm{os}} k_{\mathrm{T}}}{I_{\mathrm{o}}} \tag{16}
\end{equation*}
$$

After $t 3$, D2 and D6 are turned on. Then, S2 and S6 should be gated to achieve ZVS, and according to Fig.6, S2 and S6 are switched at $t 3$.

Stage 4 [Figure 7d, t3-t4]: At t3, S2 and S6 are turned on at zero-voltage. Sse is also turned on at this time. vrect is forced to $V C$ se, and this voltage is applied to the primary leakage inductances. Hence, $i \mathrm{Llk} 1$ and $i \mathrm{Llk} 2$ decrease, and the slope is

$$
\begin{equation*}
\frac{d i_{\mathrm{L} 1 \mathrm{k} 1}}{d t}=\frac{d i_{\mathrm{L} 1 \mathrm{k} 2}}{d t}=-\frac{k_{\mathrm{T} v_{\mathrm{Cse}}}}{L_{\mathrm{lk}}} \tag{17}
\end{equation*}
$$



Figure 6. Key waveforms of IZVZCS_SAC\&CAC.


Figure 7. Operation principle of IZVZCS_SAC\&CAC: (a) stage 1; (b) stage 2; (c) stage 3; (d) stage 4; (e) stage 5 ; (f) stage 6 ; (g) stage 7 ; (h) stage 8 .

Stage 5 [Figure 7e, $t 4-t 5$ ]: At $t 4, i$ Llk1 and $i$ Llk2 are 0 , all rectifier diodes are off. Io is free-wheeled through Sse and Cse.

Stage 6 [Figure 7f, t5-t6]: At $t 5$, Sse is off, and all rectified diodes are conducted. $i \mathrm{Llk} 1$ and $i \mathrm{Llk} 2$ keep zero.

Stage 7 [Figure $7 \mathrm{~g}, \mathrm{t6}-\mathrm{t} 7$ ]: At $t 6, \mathrm{~S} 4$ and S 8 are turned off at zero current.
Stage 8 [Figure $7 \mathrm{~h}, t 7-t 8$ ]: At $t 7, \mathrm{~S} 3$ and S 7 are turned on at zero current due to the existence of Llk1 and Llk2. iLlk1 and $i \operatorname{Llk} 2$ decrease due to negative value applied to Llk1 and Llk2. When these currents reach -Io/kT, the free-wheeling mode is over. After stage 8 , the circuit is operated in the second half period.

### 4.2. Duty Ratio Loss

The time between $t 7$ and $t 8$ is defined as the duty loss caused by the leakage inductances, and corresponding state is plotted in Figure 7 h . The primary side currents are

$$
\begin{equation*}
i_{\mathrm{L} 1 \mathrm{ki}}=0-\frac{V_{\mathrm{in}}}{L_{\mathrm{lk}}} \Delta t_{78}, i=1,2 \tag{18}
\end{equation*}
$$

when $i_{\mathrm{L} 1 \mathrm{ki}}=-I_{\mathrm{O}} / k_{\mathrm{T}}$, the free-wheeling mode is accomplished, and the time of this interval is

$$
\begin{gather*}
\Delta t_{78}=\frac{2 I_{0} L_{1 \mathrm{k}}}{V_{\mathrm{in}}}  \tag{19}\\
D_{\mathrm{L}_{-} \text {loss }}=\frac{\Delta t_{78}}{T_{\mathrm{s}} / 2}=\frac{4 I_{\mathrm{o}} L_{\mathrm{lk}} f_{\mathrm{s}}}{k_{\mathrm{T}} V_{\mathrm{in}}} \tag{20}
\end{gather*}
$$

where $D_{\mathrm{L}_{-} \text {loss }}$ is the duty ratio loss caused by the leakage inductances.
As shown in Figure 6, the primary currents are reset to zero during the interval of [ $t 4, t 5$ ]. In order to ensure safe ZCS of the lagging switches, the maximum primary duty ratio should be limited as

$$
\begin{equation*}
D_{p_{-} \max }=1-D_{\text {reset }} \tag{21}
\end{equation*}
$$

where $D_{p_{-} \max }$ is the maximum primary duty ratio of IZVZCS_SAC\&CAC.
However, as depicted in Figure 6, the primary reset time can be well compensated by the boost effect of secondary clamping, which is defined as $D_{\text {Boost }}$ in Figure 6. $D_{\text {Boost }}$ is identical to $D_{\text {reset }}$, thus, total duty ratio loss of IZVZCS_SAC\&CAC is

$$
\begin{equation*}
D_{\text {loss }}=D_{\mathrm{L} \_ \text {loss }}+D_{\text {reset }}-D_{\text {Boost }}=\frac{4 I_{\mathrm{o}} L_{\mathrm{lk}} f_{\mathrm{s}}}{k_{\mathrm{T}} V_{\mathrm{in}}} \tag{22}
\end{equation*}
$$

where $D_{\text {loss }}$ is total duty ratio loss of IZVZCS_SAC\&CAC.

### 4.3. ZVS Condition of the Leading Switches

S 2 is chosen as an example, the switching instant is provided in Figure 7c. ZVS criteria for S 2 is

$$
\begin{equation*}
\frac{1}{2} L_{\mathrm{p}}\left(\frac{I_{\mathrm{o}}}{k_{\mathrm{T}}}\right)^{2} \geq 2 C_{\mathrm{os}}\left(\frac{V_{\mathrm{in}}}{2}\right)^{2} \tag{23}
\end{equation*}
$$

where $L_{\mathrm{p}}$ is equal to $L_{1 \mathrm{k} 1}+k_{\mathrm{T} 2} L_{\mathrm{o}}$.
The minimum load current to keep safe ZVS is

$$
\begin{equation*}
I_{\mathrm{o} \_\min }=k_{\mathrm{T} 1} V_{\mathrm{in}} \sqrt{\frac{C_{\mathrm{os}}}{L_{1 \mathrm{k} 1}+k_{\mathrm{T} 1}^{2} L_{\mathrm{o}}}} \tag{24}
\end{equation*}
$$

The stored energy in the output inductance is large enough to conduct D2, so S2 can obtain ZVS in wide load range.

### 4.4. ZCS Condition of the Lagging Switches

As illustrated in Figure 6, the lagging switches should be turned off after iLlk1 and iLlk2 decay to zero. The reset time is T43, and its value is

$$
\begin{equation*}
T_{43}=\frac{I_{\mathrm{o}} L_{\mathrm{lk}}}{k_{\mathrm{T}}^{2} V_{\mathrm{Cse}}} \tag{25}
\end{equation*}
$$

When IGBTs are used as the lagging switches, the minority carriers in the component can be combined in a specific time, and this interval is determined by the component itself and defined as TCOM. Therefore, the following equation should be confirmed to ensure ZCS operation:

$$
\begin{equation*}
T_{43}+T_{\text {com }} \leq T_{\text {reset }} \tag{26}
\end{equation*}
$$

## 5. Comparative Evaluation

In this section, a comparative evaluation of the proposed converters with regard to soft-switching characteristics, duty ratio loss, the current rating of the primary components, power loss distribution, number of added components and added cost is provided to highlight the advantages and disadvantages of each converter and to help the selection of a candidate for a given application.

### 5.1. Specifications

The presented converters are compared based on the specifications listed as follows. The input voltage is varied from 100 to 300 V . The rated output voltage is 50 V , and the output current is 20 A . The switching frequency is $20 \mathrm{kHz} .1000 \mathrm{~V} / 60 \mathrm{~A}$ IGBTs are used as the primary switches, and the output capacitance of IGBTs is estimated as 1 nF . The equivalent leakage inductances of the transformer in each converter are set to be $10 \mu \mathrm{H}$. The ideal value of $k \mathrm{~T} 1$ in IZVS_SMM is 48 regardless of the effect of the leakage inductances, while $k_{\mathrm{T} 2}=16$. The ideal value of kT in other converters is 12 . The peak value of the magnetic currents of IZVS_CD and IZVS_SMM are set as 0.6 times of the primary rate current, and the magnetic currents of other converters can be omitted.

### 5.2. Duty Ratio Loss

The duty ratio loss caused by the leakage inductances is a disadvantage of PS-controlled dc-dc converters. Large duty ratio loss requires the transformer turn ratio to comprise, which degrades the performance of the converter. Table 1 shows the duty ratio loss comparison. As an additional inductor is series-connected with each primary coil, the duty ratio loss of IZVS_CD is highest among all the converters. The primary currents of IZVS_SMM are TL waveforms, thus, the duty ratio loss of IZVS_SMM is smallest among all IZVS converters. The primary currents in ZVZCS converters are reset to zero during freewheeling stages, and the duty ratio loss caused by leakage inductances of ZVZCS converters is smaller than that of IZVS converters. However, as a specific time for primary current resetting is required, thus, the duty ratio loss of IZVZCS_DCF, IZVZCS_SRC\&CAC and IZVZCS_SI is a little higher. As proved in Figure 6, the primary reset time of IZVZCS_SAC\&CAC can be compensated by the duty ratio boost effect, thus, the duty ratio loss of this converter is smallest. Figure 8 shows the duty ratio loss at rated load current. As shown in Figure 8, when $I_{0}=20 \mathrm{~A}$, the duty ratio loss of IZVS_CD is about 0.089. Considering the duty ratio loss, the turn ratios of the proposed converters should be revised, and detailed information is listed in Table 2.

Table 1. Duty ratio loss comparison [30-37].



Figure 8. Duty ratio loss at rated output current.
Table 2. Turn ratios after considering the duty ratio loss.

| Item | IZVS_CD | IZVS_CAC and IZVS_SMI | IZVS_SMM |
| :---: | :---: | :---: | :---: |
| Turn ratios | $k_{\mathrm{T}}=10.9$ | $k_{\mathrm{T}}=11.4$ | $k_{\mathrm{T} 1}=41.4, k_{\mathrm{T} 2}=16$ |
| Item | IZVZCS_DCF, IZVZCS_SRC\&CAC and | IZVZCS_SI |  |
| Turn ratios | IZVZCS_SAC\&CAC | $k_{\mathrm{T}}=11.7$ |  |

### 5.3. Soft Switching Load Range

The soft switching load range is defined as

$$
\begin{equation*}
\eta_{\mathrm{LR}}=\frac{I_{\mathrm{O} \_ \text {rate }}-I_{\mathrm{O} \_\min }}{I_{\mathrm{O} \_ \text {rate }}} \tag{27}
\end{equation*}
$$

where $I_{\mathrm{O}_{-} \text {rate }}$ represents the rated output current, and its value is 20 A in this paper; $I_{\mathrm{o}_{-} \min }$ is the minimum load current to ensure ZVS of the switches.
(1) Leading switches:

As the energy stored in the output inductance can be used, all leading switches can obtain ZVS in wide load range. As proved in [31], the minimum load of the leading switches in IZVS_CD is

$$
\begin{equation*}
I_{\mathrm{o}_{-} \min }=k_{\mathrm{T}} V_{\mathrm{in}} \sqrt{\frac{C_{\mathrm{os}}}{L_{\mathrm{r}}+L_{1 \mathrm{k}}+k_{\mathrm{T}}^{2} L_{\mathrm{o}}}} \tag{28}
\end{equation*}
$$

As proved in [32] and [35-37], the minimum load of the leading switches in IZVS_CAC and Figure 3 is

$$
\begin{equation*}
I_{\mathrm{o} \_\min }=k_{\mathrm{T}} V_{\mathrm{in}} \sqrt{\frac{C_{\mathrm{os}}}{L_{1 \mathrm{k}}+k_{\mathrm{T}}^{2} L_{\mathrm{o}}}} \tag{29}
\end{equation*}
$$

As the magnetizing current of the leading switches is increased in IZVS_SMI and IZVS_SMM, the leading switches in IZVS_SMI and IZVS_SMM can obtain ZVS down to 0 load current. Thus, the $\eta_{\text {LR }}$ of the leading switches is concluded in Table 3.

Table 3. $\eta_{\text {LR }}$ (leading-switches, 300 V ).

| Item | IZVS_CD | IZVS_CAC | IZVS_SMI | IZVS_SMM |
| :---: | :---: | :---: | :---: | :---: |
| $\eta_{\text {LR }}$ | 0.967 | 0.996 | 1 | 1 |
| Item | IZVZCS_DCF | IZVZCS_SRC\&CAC | IZVZCS_SAC\&CAC | IZVZCS_SI |
| $\eta_{\text {LR }}$ | 0.996 | 0.996 | 0.996 | 0.996 |

(2) Lagging switches:

A resonate inductance is added to enlarge the ZVS load range of the lagging switches in IZVS_CD, and, as shown in [31], the minimum load of the lagging switches in IZVS_CD is

$$
\begin{equation*}
I_{\mathrm{O}_{-} \min }=k_{\mathrm{T}} V_{\mathrm{in}} \sqrt{\frac{\mathrm{C}_{\mathrm{os}}}{L_{\mathrm{r}}+L_{1 \mathrm{k}}}} \tag{30}
\end{equation*}
$$

With proper design, the lagging switches of IZVS_CAC, IZVS_SMI and IZVS_SMM can obtain ZVS down to zero loads. The lagging switches in Figure 3 are operated in ZCS mode, and the ZCS operation can be ensured under $D_{\mathrm{p}_{-} \max }$ at rated load current. Thus, the $\eta_{\mathrm{LR}}$ of the lagging switches is listed in Table 4.

Table 4. $\eta_{\text {LR }}$ (lagging-switches, 300 V ).

| Item | IZVS_CD | IZVS_CAC | IZVS_SMI | IZVS_SMM |
| :---: | :---: | :---: | :---: | :---: |
| $\eta_{\text {LR }}$ | 0.76 | 1 | 1 | 1 |
| Item | IZVZCS_DCF | IZVZCS_SRC\&CAC | IZVZCS_SAC\&CAC | IZVZCS_SI |
| $\eta_{\text {LR }}$ | 1 | 1 | 1 | 1 |

### 5.4. Relative Current Rating of the Primary Components

The rate primary current is defined as

$$
\begin{equation*}
I_{\text {P_rate }}=I_{\text {o_rate }} / k_{\text {T_ideal }}=20 / 12=1.667(\mathrm{~A}) \tag{31}
\end{equation*}
$$

where $I_{\mathrm{p}_{-} \text {rate }}$ is the primary rate current; $k_{\mathrm{T}_{-} \text {ideal }}$ is 12 .
The primary relative average absolute current rating is

$$
\begin{equation*}
\tau_{\mathrm{C}_{-} \mathrm{AV}}=\frac{I_{\mathrm{p} \_\mathrm{AV}}}{I_{\mathrm{p} \_ \text {rate }}} \tag{32}
\end{equation*}
$$

where $I_{\mathrm{p}_{-} \mathrm{AV}}$ is the primary average absolute current.
The primary relative RMS current rating is

$$
\begin{equation*}
\tau_{\mathrm{C} \_ \text {RMS }}=\frac{I_{\mathrm{p} \_\mathrm{RMS}}}{I_{\text {p_rate }}} \tag{33}
\end{equation*}
$$

where $I_{\mathrm{p}_{-} \mathrm{RMS}}$ is the primary RMS current.
Table 5 illustrates $\tau_{\mathrm{C}_{-} A V}$ and $\tau_{\mathrm{C}_{-} R M S}$ of the primary components. The magnetizing currents of IZVS_SMI are increased to help ZVS of the lagging switches, and these currents keep their peak value during the whole free-wheeling time. Thus, $\tau_{\text {C_AV }}$ and $\tau_{\text {C_RMS }}$ of IZVS_SMI is highest, which results highest primary side conduction loss. The magnetizing currents of IZVS_SMM are also enlarged, but, the average value in the half switching cycle of these currents is zero, and these currents are not in phase with the load current. Hence, $\tau_{\mathrm{C}_{-} A V}$ and $\tau_{\mathrm{C}_{-} R M S}$ of IZVS_SMM are much smaller than that of IZVS_SMI. The IZVZCS_SAC\&CAC has the smallest $\tau_{\mathrm{C} \_A V}$ and $\tau_{\mathrm{C}_{-} R M S}$.

Table 5. $\tau_{C_{-} A V}$ and $\tau_{C_{-} R M S}$ of the primary components.

| Item | $\tau_{\text {C_AV }}$ |  | $\tau_{\text {C_RMS }}$ |  |
| :---: | :---: | :---: | :---: | :---: |
|  | Switches | Added diodes | Transformer | Added inductor |
| IZVS_CD | 1.1 | 0.55 | 1.1 | 1.1 |
| IZVS_CAC | 1.05 | None | 1.05 | 0.21 |
| IZVS_SMI | 1.89 | None | 1.3 | None |
| IZVS_SMM | 1.04 | None | 1.09 | None |
| IZVZCS_DCF | 1.08 | 0.54 | 1.08 | None |
| IZVZCS_SAC\&CAC | 1.02 | None | 1.02 | None |
| IZVZCS_SRC\&CAC | 1.08 | None | 1.08 | None |
| IZVZCS_SI | 1.08 | None | 1.08 | 1.08 |

### 5.5. Power Loss Distribution

The losses of soft-switching FB converters mainly include switching losses, transformer losses, output rectifier diode losses, resonance inductance losses, and other losses. The switching loss model mainly covers light-load and heavy-load senarios. The losses of a MOSFET can be calculated by (34), where $P_{\text {Driver }}$ is the driving loss, $P_{\text {SW }}$ is the switching loss of the MOSFET, $P_{\text {MOS_Lead }}$ is the conduction loss of the leading MOSFET, $P_{\text {MOS_Lag }}$ is the conduction loss of the lagging MOSFET.

$$
\left\{\begin{array}{c}
P_{\mathrm{MOSFET}}=P_{\text {Drive }}+P_{\mathrm{SW}}  \tag{34}\\
P_{\mathrm{MOSFET}}=P_{\mathrm{MOS} \text { _Lead }}+P_{\text {MOS_Lag }}
\end{array}\right.
$$

Transformer loss mainly includes copper loss $\left(P_{\text {Winding }}\right)$ and iron loss, which includes eddy-current $\operatorname{loss}\left(P_{\mathrm{e}}\right)$ and hysteresis $\operatorname{loss}\left(P_{\mathrm{h}}\right)$. Then, the total transformer loss, defined as $P_{\mathrm{T}}$, is

$$
\begin{equation*}
P_{\mathrm{T}}=P_{\text {Winding }}+P_{\mathrm{h}}+P_{\mathrm{e}} \tag{35}
\end{equation*}
$$

The output rectifier diode loss includes three parts: turn-off $\operatorname{loss}\left(P_{\mathrm{D}_{-} \text {off }}\right)$, turn-on $\operatorname{loss}\left(P_{\mathrm{D} \_ \text {on }}\right)$, and on-state $\operatorname{loss}\left(P_{\text {Con }}\right)$. The total loss of a diode, defined as $P_{\mathrm{D}_{-} \text {loss, }}$, is

$$
\begin{equation*}
P_{\mathrm{D} \_ \text {loss }}=P_{\mathrm{D} \_ \text {off }}+P_{D_{-} \text {on }}+P_{\mathrm{Con}} \tag{36}
\end{equation*}
$$

Inductor losses mainly include copper loss, $P_{\mathrm{Cu}_{-} l o}$ and iron loss $P_{\mathrm{Fe} \_l}$. Then the total inductor loss of $L_{o}$ and $L_{r}$ are

$$
\begin{align*}
P_{\mathrm{Lo} \_ \text {loss }} & =P_{\mathrm{Fe} \_ \text {lo }}+P_{\mathrm{Cu} \_ \text {lo }}  \tag{37}\\
P_{\mathrm{Lr} \_ \text {loss }} & =P_{\mathrm{Fe} \_ \text {lr }}+P_{\mathrm{Cu} \_ \text {lr }} \tag{38}
\end{align*}
$$

Relative switching loss is

$$
\begin{equation*}
\delta_{\mathrm{S}_{-} \text {loss }}=\frac{\sum_{\mathrm{n}} P_{\mathrm{S}_{\mathrm{L}} \mathrm{Loss}}}{P_{\mathrm{o}}} \tag{39}
\end{equation*}
$$

where $P_{\mathrm{o}}$ is the output power and $\delta_{\mathrm{S}_{-} \text {loss }}$ is the corresponding switching loss.
Relative conduction loss is

$$
\begin{equation*}
\delta_{\mathrm{C}_{-} \text {loss }}=\frac{\sum_{\mathrm{n}} P_{\mathrm{C}_{\text {_Loss }}}}{P_{\mathrm{o}}} \tag{40}
\end{equation*}
$$

where $P_{\mathrm{o}}$ is the output power and $P_{\mathrm{C}_{-} \text {Loss }}$ is corresponding conduction loss.
The power loss distribution of the proposed converters is estimated in Table 6. The magnetizing currents of IZVS_SMM are enlarged to help the ZVS of the primary switches and the peak value of these currents can provide more resonant energy with increasing of the input voltage, thus, the switching loss of the primary switches of IZVS_SMM is smallest among all IZVS converters. When $V_{\text {in }}=300 \mathrm{~V}$, the phase angle between the primary switches and secondary switches is zero, and the primary currents of IZVS_SMM are much smaller than that of other IZVS converters. Therefore, the primary
conduction loss of IZVS_SMM is also smallest among all IZVS converters. As depicted in Table 6, some secondary conduction loss and switching loss is added to the converter in IZVS_SMM because two secondary switches are required. However, the efficiency of IZVS_SMM is still highest among all IZVS MMDCs. As shown in Table 6, the IZVZCS_SAC\&CAC has the smallest conduction loss among all ZVZCS MMDCs due to smaller duty ratio loss. In addition, the turn-off loss of the leading switches of IZVZCS_SAC\&CAC is also smaller, which results in smaller switching loss of the primary switches. Hence, the efficiency of IZVZCS_SAC\&CAC is highest among all ZVZCS converter.

Table 6. $\delta$ S_loss and $\delta C_{-}$loss $\left(V_{\text {in }}=300 \mathrm{~V}\right)$.

| Item | $\delta_{\text {S_loss }} \times 10^{-3}$ |  |  |  | $\delta_{\text {C_loss }} \times 10^{-3}$ |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Primary |  | Secondary |  | Primary |  | Secondary |  |
|  | $I_{0}=5 \mathrm{~A}$ | $I_{0}=20 \mathrm{~A}$ | $I_{0}=5 \mathrm{~A}$ | $I_{0}=20 \mathrm{~A}$ | $I_{0}=5 \mathrm{~A}$ | $I_{0}=20 \mathrm{~A}$ | $I_{0}=5 \mathrm{~A}$ | $I_{0}=20 \mathrm{~A}$ |
| IZVS_CD | 73.5 | 49.3 | 23.3 | 15.5 | 18.1 | 20.1 | 17.8 | 19.8 |
| IZVS_CAC | 57.6 | 38.6 | 23.3 | 15.5 | 14.5 | 16.1 | 17.8 | 19.8 |
| IZVS_SMI | 79.1 | 53.1 | 23.3 | 15.5 | 21.2 | 23.6 | 17.8 | 19.8 |
| IZVS_SMM | 40.4 | 28 | 24.6 | 16.5 | 9.6 | 10.7 | 19.6 | 21.8 |
| IZVZCS_DCF | 71.1 | 47.4 | 23.3 | 15.5 | 13.9 | 15.4 | 17.8 | 19.8 |
| IZVZCS_SAC\&CAC | 47.3 | 36.4 | 24.6 | 16.5 | 9.6 | 10.7 | 18.1 | 20.1 |
| IZVZCS_SRC\&CAC | 67.5 | 45 | 23.3 | 15.5 | 10.4 | 11.6 | 18.5 | 20.5 |
| IZVZCS_SI | 74.3 | 49.5 | 23.3 | 15.5 | 13.0 | 14.4 | 17.8 | 19.8 |

### 5.6. Structure and Cost Comparison

Table 7 shows a comparison of added components of the proposed converters. The IZVS_SMI, IZVS_SMM, IZVZCS_SAC\&CAC and IZVZCS_SRC\&CAC have no added primary components, which means the primary circuits of these converters are simpler and more compact compared to that of other converters. A smaller number of primary components means not only cheaper BOM cost but also simpler and more compact primary structure. In addition, less area in the primary side of these converters is required to ensure safe electrical clearance due to the smaller number of primary components and simpler connection between these components. Therefore, the primary circuit volume of the IZVS_SMI, IZVS_SMM, IZVZCS_SAC\&CAC and IZVZCS_SI is smaller and more compact, which are attractive features for high input voltage industry applications. As depicted in Table 7, the IZVS_CD, IZVS_CAC, IZVS_SMI, IZVZCS_DCF and IZVZCS_SI require no added secondary components. In some industrial applications, the input voltage may be 1400 V or higher. Due to the modular structure, the proposed converters can be extended to higher voltage levels easily. As shown in Table 7, the added primary components of the extension topologies of the IZVS_CD, IZVS_CAC, IZVZCS_DCF and IZVZCS_SI increase linearly with the number of the primary modules. However, as depicted in Table 7, the added secondary components of the extension topologies of the IZVS_SMI, IZVS_SMM and IZVZCS_SRC\&CAC are not increased with primary cells. Thus, the IZVS_SMI, IZVS_SMM, IZVZCS_SAC\&CAC and IZVZCS_SI are more suitable for super-high-voltage applications due to smaller added components and a simpler primary structure. The added cost of the proposed converters is listed in Table 8.

From above analyses, some brief conclusions can be drawn as follows. The IZVS_SMM and IZVZCS_SRC\&CAC show some clear advantages compared to other solutions, e.g., smaller duty ratio loss, wide range soft switching operation, less conduction loss, simpler and more compact primary circuit, and lower added cost. Thus, these two converters are more suitable for high input voltage applications with more primary modules. The current stress of Sse and Cse in IZVZCS_SRC\&CAC increases with the output current, which may arise several implementation problems. Hence, the IZVS_SMM is a better choice for large output current applications. The IZVS_SMM has some special characteristics. The secondary rectified voltage is a TL waveform, which results lower input
and output filter requirements. The IZVS_SMM is the only topology, which can be used in the high input applications with controllable multi-output ports.

Table 7. Added component comparison. ( N is series-connected primary modules number).

| Converter | Added primary components | Added secondary components |
| :---: | :---: | :---: |
| IZVS_CD | $\mathrm{N} \times$ inductors and $2 \mathrm{~N} \times$ diodes | None |
| IZVS_CAC | $\mathrm{N} \times$ inductors and $\mathrm{N} \times$ capacitors | None |
| IZVS_SMI | None | None |
| IZVS_SMM | None | $2 \times$ MOSFETs and $2 \times$ diodes |
| IZVZCS_DCF | $2 \mathrm{~N} \times$ diodes | None |
| IZVZCS_SAC\&CAC | None | $1 \times$ MOSFET and $1 \times$ capacitors |
| IZVZCS_SRC\&CAC | None | $2 \times$ diodes and $1 \times$ capacitors |
| IZVZCS_SI | $\mathrm{N} \times$ inductors | None |

Table 8. Added cost comparison. (Two series-connected primary modules).

| Converter | Added components | Added cost | Ratio of the total cost |
| :---: | :---: | :---: | :---: |
| IZVS_CD | $2 \times$ inductors and $4 \times$ diodes | $\$ 150$ | $8.8 \%$ |
| IZVS_CAC | $2 \times$ inductors and $2 \times$ capacitors | $\$ 60$ | $3.3 \%$ |
| IZVS_SMI | $2 \times$ MOSFETs, $2 \times$ diodes and | None | None |
| IZVS_SMM | corresponding drive circuits <br> $4 \times$ diodes | $\$ 80$ | $4.4 \%$ |
| IZVZCS_DCF | $\$ \times$ MOSFETs, $1 \times$ diodes and | $\$ 120$ | $6.7 \%$ |
| IZVZCS_SAC\&CAC | corresponding drive circuits | $\$ 50$ | $2.8 \%$ |
| IZVZCS_SRC\&CAC | $2 \times$ diodes and $1 \times$ capacitors | $\$ 45$ | $2.6 \%$ |
| IZVZCS_SI | $2 \times$ inductors | $\$ 30$ | $1.7 \%$ |

## 6. Experimental Results

The IZVS_SMM and IZVZCS_SAC\&CAC are selected as examples to test in this section, and the conventional FB MMDC in Figure 1 is also tested in the efficiency comparison. The main parameters of the prototype are listed in Table 9. The waveforms of IZVS_SMM and IZVZCS_SAC\&CAC are provided in Figure 9.

Table 9. Main parameters of the prototypes.

| Item | Parameters |
| :---: | :---: |
| Input | $100-300 \mathrm{~V}$ |
| Output | $50 \mathrm{~V} / 20 \mathrm{~A}$ |
| Switching frequency | 20 kHz |
| I GBT | G 60 N 100 |
| C BL1 $_{\text {and CBL2 }}$ | $100 \mu \mathrm{~F}$ |
| $k_{\mathrm{T} 1}$ and $k_{\mathrm{T} 2}$ (IZVS_SMM) | $k_{\mathrm{T} 1}=41, k_{\mathrm{T} 2}=16$ |
| $k_{\mathrm{T}}$ (IZVZCS_SAC\&CAC) | 11.7 |
| $k_{\mathrm{T}}$ (Figure 1) | 11.4 |
| $\mathrm{~S}_{\text {se1 }}$ and S S Se2 (IZVS_SMM)) | IPB180N04S4 $\times 4$ |
| $\mathrm{~S}_{\text {se }}$ (IZVZCS_SAC\&CAC) | IPB180N04S4 $\times 1$ |
| $\mathrm{C}_{\text {se }}$ (IZVZCS_SAC\&CAC) | $3 \mu \mathrm{~F} / 200 \mathrm{~A}$ |
| Rectifier diodes | MBR 30100 |
| $\mathrm{~L}_{\mathrm{o}}$ | $7 \mu \mathrm{H}$ |
| $\mathrm{C}_{\mathrm{o}}$ | $1000 \mu \mathrm{~F}$ |



Figure 9. Experimental waveforms: (a) $v \mathrm{CE}(\mathrm{S} 1)$ and $v \mathrm{CE}(\mathrm{S} 5)$ of IZVS_SMM; (b) $v \mathrm{cin} 1$, $v \mathrm{in} 2$ and io of IZVS_SMM; (c) vBC and iLlk1 of IZVS_SMM; (d) iLo and vrect of IZVS_SMM; (e) iLlk2 of IZVS_SMM; (f) vBC and iLlk1 of IZVS_SMM (soft start); (g) vGE(S1) and vCE(S1) of IZVS_SMM (turn-on); (h) vGE(S1) and $v \mathrm{CE}(\mathrm{S} 1)$ of IZVS_SMM (turn-off); (i) $v \mathrm{DS}$ (Sse1) and $i \mathrm{DS}(\mathrm{Sse} 1)$ of IZVS_SMM; (j) $v \mathrm{BC}$, iLlk1and iLo of IZVZCS_SAC\&CAC; (k) vBC and ise of IZVZCS_SAC\&CAC; (1) vGE(Sse) and $i \operatorname{Llk} 1$ of IZVZCS_SAC\&CAC; (m) $v \mathrm{GE}(\mathrm{S} 1)$ and $v \mathrm{CE}(\mathrm{S} 1)$ of IZVZCS_SAC\&CAC; (n) $v \mathrm{CE}(\mathrm{S} 1)$ and $v C E(S 5)$ of IZVZCS_SAC\&CAC.

A conventional circuit of a phase-shifted full-bridge includes IZVS and ZVZCS operation modes. IZVS implement ZVS on both the leading switches and the lagging switches. Due to the existence of the transformer leakage inductance and the output inductance, the current does not change suddenly when the leading switches are turned off, and only ZVS. IZVS mode has good switching characteristics and high on-state loss. For the ZVZCS mode, it achieves ZVS of the leading switches and ZCS on the lagging switches. ZVZCS mode has low on-state loss and current overshoot. Some of the proposed FB-MMDCs discussed in this paper have clear advantages compared with conventional FB MMDC. For example, IZVZCS-SAC\&CAC (see Figure 3b) has less voltage stress on the primary switch no additional primary clamping device and modular primary structure. In addition, the primary switch in all converters can achieve ZVS or ZCS over a wide load range.

As shown in Figure 9a, the off-state voltage of the primary switches in IZVS_SMM is even during normal operation stages, and the midpoint voltage of the input capacitors is stable and equals Vin/2. $v \mathrm{in}, v \mathrm{Cin} 2$ and Io are depicted in Figure 9b, and the mid-point voltage of the input capacitors is balanced even during the output dynamic instant. As proved in Figure 9c, $\mathrm{iLlk1}$ is not a constant value because $i 1 \mathrm{~m}$ is enlarged to help the ZVS of the primary switches. As $i 1 \mathrm{~m}$ is not in phase with the load current, the added primary RMS current is smaller. Thus, added conduction loss is also smaller. As depicted in Figure 9 c, vBC does not have free-wheeling time. Therefore, the input current ripple is smaller. As proved in Figure 9d, the secondary rectified voltage is a TL waveform, which can significantly reduce the volume of output filter. The $i \operatorname{Llk} 2$ is provided in Figure 9e, and $v \mathrm{BC}$ and $i \mathrm{Llk} 1$ during the soft-start operation are shown in Figure 9f. The voltage waveforms of the gate-emitter and the collector-emitter of S1 are depicted in Figure 9 g and 9h. In Figure 9g, the gate-emitter voltage of S1 is much lower than gate-emitter threshold voltage when the collector-emitter voltage of S1 decreases to zero, thus, S1 can obtain ZVS. According to Figure 9i, Sse1 can obtain ZCS.

The waveforms of IZVZCS_SAC\&CAC are depicted in Figure 9j to 9n. As proved in Figure 9j, $i \mathrm{Llk} 1$ is reset by the secondary clamping capacitor and keeps zero during the whole free-wheeling stage. Thus, the lagging switches can obtain ZCS. In addition, the primary circling energy is zero. ise is provided in Figure 9k. The gate signal of Sse and the primary current is depicted in Figure 91, the secondary switches are turned on at the beginning of the free-wheeling stages to reset the primary currents. In Figure 9m, the gate-emitter voltage of S1 is much lower than the gate-emitter threshold voltage when the collector-emitter voltage of S1 decreases to zero; thus, S 1 can obtain ZVS. As shown in Figure 9n, the off-state voltage of the primary switches in IZVZCS_SAC\&CAC is even during normal operation stages, and the mid-point voltage of the input capacitors is stable and equals Vin/2.

Figure 10 shows the efficiency comparison between the converters in the conventional FB MMDC (Figure 1), the IZVS with secondary modulation method (IZVS_SMM, Figure 2d) and the IZVZCS with secondary active clamping and commutation auxiliary circuit (IZVZCS_SAC\&CAC, Figure 3b). During the efficiency test, the auxiliary power of the controller and driver are taken into account, and the power of the force air cooling fan is also included. As depicted in Figure 10a, the efficiency of IZVS_SMM and IZVZCS_SAC\&CAC is higher than that of Figure 2 because of wide-range soft-switching for all primary switches. As illustrated in Figure 10a, the light-load efficiency of IZVZCS_SAC\&CAC is a bit lower than that of IZVS_SMM because the switching loss of the leading switches is a little higher, and the high load efficiency of IZVZCS_SAC\&CAC is a bit higher than that of IZVS_SMM due to the smaller turned off loss of the lagging switches and lower conduction loss. Figure 10b shows the efficiency curves with larger output capacitance of the primary switches. Turn-off loss of the switches decreases with the increasing of the output capacitance, but, turn-on loss may increase due to narrow ZVS load range. As all primary switches in IZVS_SMM can still obtain ZVS turned-on in wide load range with less added conduction loss, the efficiency of IZVS_SMM is higher than others. Hence, the converter in IZVS_SMM can gain optimum efficiency performance by more flexible selecting of the trade-off among turn-on loss, turn-off loss and conduction loss. Figures 10c and 10d show the efficiency comparison with variable input voltage. The efficiency curves decrease with the increasing of the input voltage. As the magnetizing inductances can provide more resonant energy, the converter in IZVS_SMM has higher efficiency under high input voltage condition.


Figure 10. Efficiency comparison: (a) variable output current (Vin $=300 \mathrm{~V}$, $\mathrm{Cos}=1 \mathrm{nF}$ ); (b) variable output current (Vin = $300 \mathrm{~V}, \mathrm{Cos}=10 \mathrm{nF}$ ); (c) variable input voltage ( $\mathrm{Io}=20 \mathrm{~A}, \mathrm{Cos}=1 \mathrm{nF}$ ); (d) variable input voltage ( $\mathrm{Io}=20 \mathrm{~A}, \mathrm{Cos}=10 \mathrm{nF}$ ).

## 7. Conclusions

Eight wide-range soft-switching FB MMDCs are proposed and discussed. Two of the most promising converters are found and explained in detail, and a comparative evaluation among the proposed converters is also provided. The experimental results agree with the theoretical prediction. The IZVS_SMM and IZVZCS_SAC\&CAC show clear advantages compared to other solutions, e.g., smaller duty ratio loss, wide-range soft switching, less conduction loss, a simpler and more compact primary circuit and lower added cost. Thus, these two converters are more suitable for high input voltage applications with more primary modules. Furthermore, the IZVS_SMM has some special characteristics. its secondary rectified voltage is a TL waveform, which results in lower input and output filter requirements. The IZVS_SMM is the only topology which can be used in the high input voltage applications with controllable multi-output ports.

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