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An Area-Efficient 10-Bit Buffer-Reused DAC for AMOLED Column Driver ICs

Ming Xia [1,2], Zunkai Huang [1,*], Li Tian [1], Ning Wang [1], Yongxin Zhu [1], Hui Wang [1,*] and Songlin Feng [1]

[1] Shanghai Advanced Research Institute, Chinese Academy of Sciences, Shanghai 201210, China; xiam@sari.ac.cn (M.X.); tianl@sari.ac.cn (L.T.); wangning@sari.ac.cn (N.W.); zhuyongxin@sari.ac.cn (Y.Z.); fengsl@sari.ac.cn (S.F.)

[2] University of Chinese Academy of Sciences, Beijing 100049, China

* Correspondence: huangzk@sari.ac.cn (Z.H.); wanghui@sari.ac.cn (H.W.)

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Abstract: In this paper, we proposed an area-efficient 10-bit digital-to-analog converter (DAC) with buffer-reusing method to dramatically relief the severe area exploding issue in high-definition active-matrix organic light-emitting diode (AMOLED) driver integrated circuits (ICs). In our design, we implement the functionalities of a large number of switches and capacitors in conventional DAC by a compact internal buffer. Furthermore, we minimize the buffer capacity requirement by elaborately reusing the indispensable output buffer in the typical column driver. In this way, we can cut down nearly a half of the decoder-switches and simultaneously reduce the capacitor size from 8 *C* to 3 *C* without designing an intricate and power-consuming amplifier separately. A prototype 6-channel column driver employing the proposed buffer-reused DAC was fabricated by 0.35 μm 2P3M BCD (Bipolar, CMOS, DMOS) process and its effective layout area per channel is 0.0429 mm^2, which is 42.8% smaller than that of the conventional 10-bit R-C DAC. Besides, the measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.514 LSB/0.631 LSB, respectively and the maximum value of inter-channel deviation voltage output (DVO) is 3.25 mV. The settling time within 5.6 μs is readily achieved under 1.5 kΩ-resistance and 100 pF-capacitance load. Measurement results indicate that the proposed buffer-reused DAC can successfully minimize the die area while maintaining other required performances.

Keywords: AMOLED displays; digital-to-analog converter (DAC); output buffer; column driver

1. Introduction

Active-matrix organic light-emitting diode (AMOLED) display has recently emerged as the most promising candidate for the next-generation mainstream display technology. It natively presents superior characteristics over other display technologies, such as thinness, lightweight, wide viewing angle, bright color, fast response and low power consumption [1–4]. In AMOLED display panel, data driver IC(integrated circuit) is usually considered as one of the most critical components, which receives the instructions and digital frame data from the video processor and provides the analog data signal to the pixel array. The ever-increasing demand of ultra-high-resolution panels leads to a growing community of researches on driver IC, including driving strategy design, circuit optimization, et al. Among various driving schemes, the voltage-driving method, which features fast writing time and a reduction in power consumption, has been widely adopted in commercial applications [5]. Generally, an AMOLED driver IC is composed of a column driver, a timing controller, a row driver and a reference generator. The column driver is especially crucial in achieving high-speed driving, high resolution and low-power dissipation. Figure 1 illustrates the block diagram of a quintessential column

driver. Basically, a column driver consists of shift registers, sample latches, data latches, level shifters, digital-to-analog converters (DACs) and output buffers. Its operating principle can be concluded as follows—The graphic data are firstly paralleled by the shift registers and the input registers and then subsequently stored in the data latches. Next, the signal amplitude of graphic data is lifted by the level shifters. After that, the DACs reconstruct the graphic data from the digital domain to the analog domain. Finally, the output buffers drive the data line of the pixel array to the corresponding voltage values within one horizontal scanning time. DACs play a key role in data voltage generation in the column driver and they usually occupy a large part of the chip area in the driver IC. For example, in a 6-bit driver IC, the DACs occupies more than 30% of the die area [6]. Consequently, area compactness becomes one of the most stringent requirements for DACs [7]. Furthermore, as the number of columns in the AMOLED panel increases rapidly, it becomes more important to reduce the chip area of DACs as much as possible while maintaining their accuracy and uniformity [8].

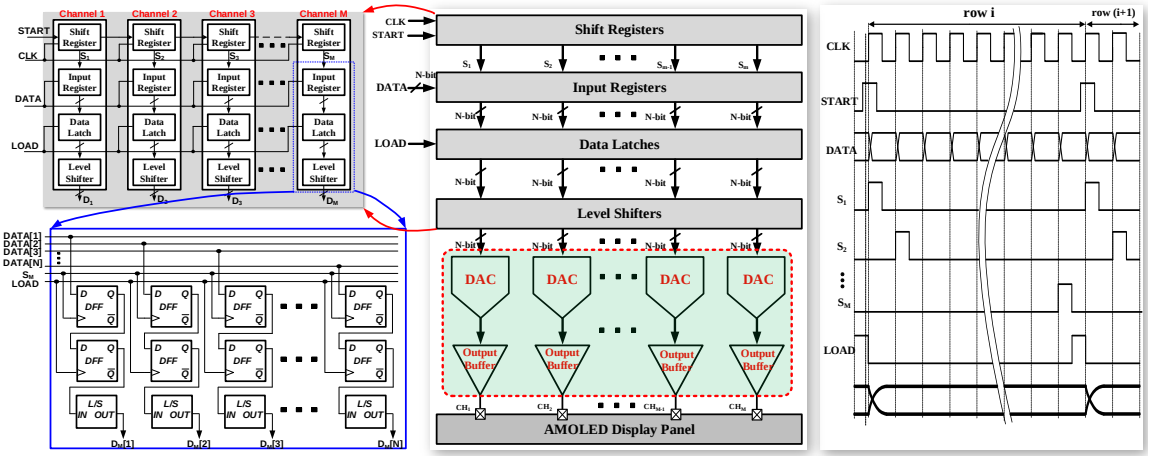


Figure 1. The architecture of active-matrix organic light-emitting diode (AMOLED) column driver.

Currently, resistor DAC (R-DAC) is widely utilized in AMOLED column drivers due to its distinguished uniformity, which stems from the commonly shared resistor-string for all channels [9,10]. However, the area of R-DAC generally increases exponentially along with the improvement of conversion resolution [11]. This makes the conventional R-DAC impractical for use in column driver ICs for more vivid colors with higher resolution. To overcome the afore-mentioned issues, several area-efficient two-stage DACs have been proposed, including resistor-to-resistor DACs (R-R DACs) [11,12], resistor-to-capacitor DACs (R-C DACs) [13,14] and embedded DACs [15,16], respectively. In these two-stage DACs, the 1st stage DAC selects two adjacent voltages according to the *M* MSBs and sends these two voltages to the second stage and the 2nd stage DAC conducts fine conversion according to the (*N*-*M*) LSBs by means of resistive subdivision or charge-redistribution. In this way, the die area of two-stage DACs can be effectually shrunken. However, there still remains several unsolved problems with the conventional two-stage DACs. In R-R DAC, it is difficult to maintain uniformity among all channels due to the ineludible offset errors introduced by the independent unity-gain buffers in the 2nd stage DAC. Besides, the isolating buffers also inevitably consume extra power consumption. In the case of the embedded DAC, it also suffers greatly from channel matching challenges. The R-C DAC outperforms other DACs in terms of uniformity but it has limited capacity for channel area reduction. More critically, the aforementioned two-stage DACs, as well as other state of the art two-stage DACs, generally contain a redundant two-voltage selector. The die area required for an *i*-bit two-voltage selector is doubled compared with an *i*-bit one-voltage selector. Hence, the conventional two-stage DACs are far from thoroughly optimized in terms of area occupancy.

In this paper, we make the following contributions to alleviate the area redundancy issue of conventional two-stage DACs—(1) We propose a novel two-stage 10-bit DAC design with an internal buffer to replace the functionalities of large number of switches and capacitors in conventional DAC

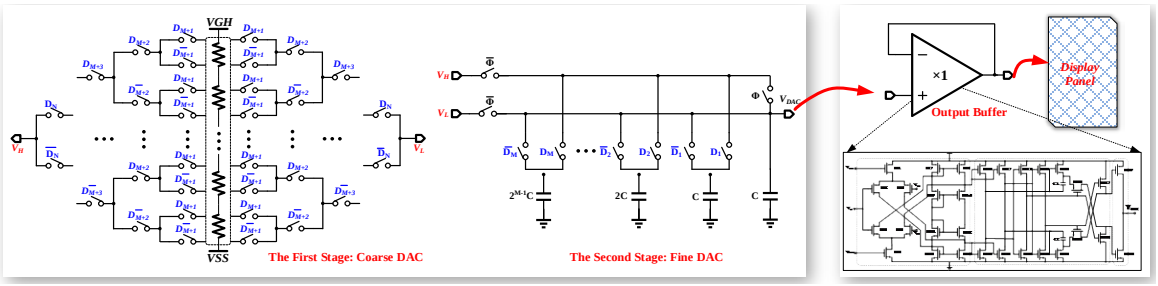
design; (2) We propose a buffer-reusing method to minimize the buffer capacity requirement; (3) We verify our design by taping-out a 6-channal column driver IC containing the proposed buffer-reused DAC module.

This paper is organized as follows—Section 2 first introduces the basic structure of conventional R-C DAC and then explains the principle of our proposed buffer-reused DAC. Section 3 describes the class-B buffer adopted in the proposed DAC. Section 4 demonstrates the experimental results and the conclusions are presented in Section 5.

2. DAC Architecture

2.1. Principle of the Conventional Two-Stage R-C DAC

For the convenience of comparison, we prefer to first explain the architecture and principle of the conventional two-stage R-C DAC briefly. A representative *N*-bit R-C DACs for the AMOLED column driver is illustrated in Figure 2. As previously mentioned, the 1st stage DAC predominantly consists of a global resistor string and a two-voltage selector and it selects two adjacent voltages according to the (*N*-*M*)-bit MSBs (D_N~D_{M+1}). Additionally, the 2nd stage DAC is typically comprised of a switched-capacitor circuit and it mainly conducts the fine conversion according to the *M*-bit LSBs (D_M~D_1) by means of charge-redistribution. In comparison with the traditional R-R DACs, the two-stage R-C DAC shown in Figure 2 holds advantages of high uniformity and low static power consumption, so it has been considered as a good choice in the high-definition AMOLED display application. However, the conventional two-stage R-C DAC owns limited capacity for channel area reduction because of its redundant two-voltage selector. For instance, in a 10-bit (7-bit MSBs and 3-bit LSBs) two-stage R-C DAC, there are totally 508 switches in the first stage DAC and the die area required for these 508 switches is twice times larger than that of a 7-bit one-voltage selector. Hence, the conventional two-stage DACs are far from optimal in terms of area occupancy.



(**a**) (*N*-*M*)-bit coarse DAC (**b**) *M*-bit fine section DAC

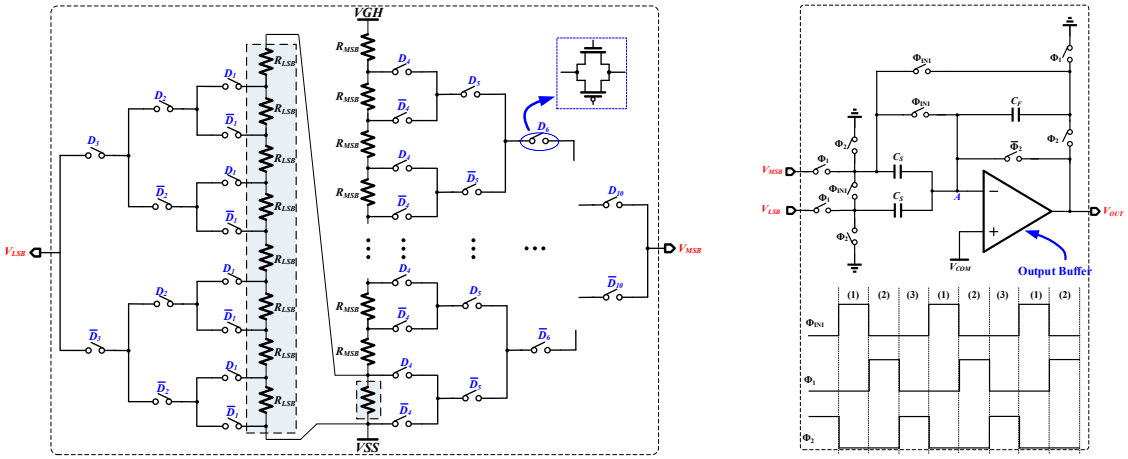
Figure 2. The schematic diagram of a typical *N*-bit two-stage resistor-to-capacitor digital-to-analog converter (R-C DAC) consisting of (**a**) (*N*-*M*)-bit coarse DAC and (**b**) *M*-bit fine section DAC.

2.2. Our Proposed Area-Efficient 10-Bit DAC with the Buffer-Reusing Method

As discussed before, the conventional two-stage R-C DAC generally contains a complicated two-voltage selector in its 1st stage, which inevitably results in chip an increased dimension since the die area required for an *i*-bit two-voltage selector doubles that of an *i*-bit one-voltage selector. To overcome these issues, we propose a novel two-stage 10-bit DAC design with an internal buffer to replace the functionalities of a large number of switches and capacitors in conventional DAC design and adopt a buffer-reusing method to minimize the buffer capacity requirement. The principle of our proposed buffer-reused DAC is described below.

The schematic and timing diagrams of our proposed area-efficient 10-bit DAC is shown in Figure 3. The proposed 10-bit DAC is divided into the 1st stage 7-bit coarse conversion sub-DAC and the 2nd

stage 3-bit fine conversion sub-DAC, respectively. Compared with the conventional two-stage R-C DAC, it merely consists of a compact 7-bit one-voltage selector and a tiny 3-bit one-voltage selector in its 1st stage sub-DAC, rather than a complicated 7-bit two-voltage selector. Accordingly, the switch number, as well as the relevant routing wires in the proposed DAC, can be significantly decreased. Specifically, the 1st stage sub-DAC of our proposed circuit purely contains 268 switches, while the conventional two-stage R-C DAC shown in Figure 2 needs more than 508 switches.



(**a**) The 1st stage sub-DAC (**b**) The 2nd stage sub-DAC

Figure 3. The schematic diagram of our proposed area-efficient 10-bit DAC with buffer-reusing method: (**a**) the 1st stage sub-DAC and (**b**) the 2nd stage sub-DAC.

As shown in Figure 3a, in the 1st stage sub-DAC, the 7-bit one-voltage selector and the 3-bit one-voltage selector select two voltages, namely V_{MSB} and V_{LSB}, from the global resistor-string according to D_{10}–D_4 and D_3–D_1, respectively and then feed them to the 2nd stage sub-DAC. The global resister string is constructed by 127 large resistors with the value of R_{MSB} and 8 small resistors with the value of R_{LSB} and is connected between the high reference voltage V_{GH} and ground V_{SS}. The resistance of R_{MSB} and R_{LSB} satisfies the following condition:

$$R_{MSB} = 8R_{LSB}. \tag{1}$$

Besides, the magnitude of V_{MSB} and V_{LSB} in the 1st stage sub-DAC can be figured out by Equations (2) and (3) according to the voltage division principle of the resistor string:

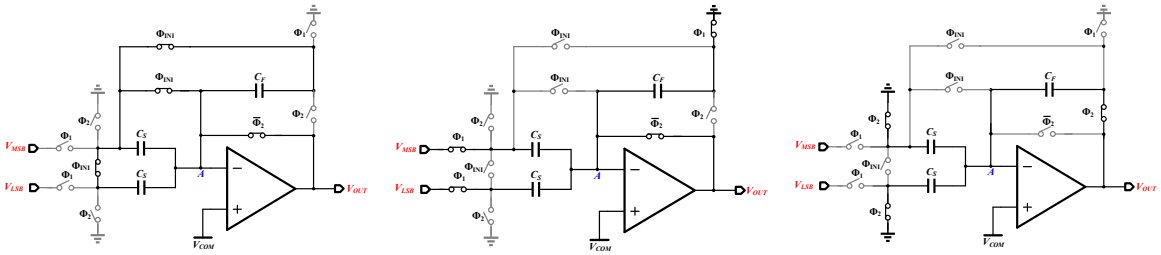
$$V_{MSB} = \frac{VGH \times R_{MSB}}{127R_{MSB} + 8R_{LSB}} \sum_{i=0}^{i=6} 2^i D_{i+3} = \frac{VGH}{2^7} \sum_{i=0}^{i=6} 2^i D_{i+3} \tag{2}$$

$$V_{LSB} = \frac{VGH}{2^7 \times 2^3} \sum_{i=0}^{i=2} 2^i D_i = \frac{VGH}{2^{10}} \sum_{i=0}^{i=2} 2^i D_i. \tag{3}$$

The schematic diagram of the 2nd stage sub-DAC is illustrated in Figure 3b. It can be principally counted as a sample-and-hold circuit, which is implemented by two sampling-capacitors C_S, a feedback-capacitor C_F, 10 MOS (Metal-Oxide-Semiconductor) switches and an operational amplifier. The capacitance values of the sampling-capacitor C_S and the feedback-capacitor C_F are equal. The switches are controlled by the three clock signals, namely Φ_{INI}, Φ_1 and Φ_2. We elaborately reused the existing output buffer, whose primary assignment is to drive the data line with a high capacitive load in the column driver, to fabricate the sample-and-hold circuit. This means we can expediently obtain the 2nd stage sub-DAC without designing an intricate and power-consuming dedicated amplifier. Furthermore, the capacitor size in our proposed DAC is declined from 8 C to 3 C

as well compared with the conventional 10-bit R-C DAC as depicted in Figure 2. By employing the proposed buffer-reusing method, we can effectively minimize the buffer capacity requirement and thus the area dimension of the column driver will be further narrowed.

Overall, the operation principle of our proposed area-efficient buffer-reused DAC can be divided into three phases, namely reset phase ($\Phi_{INI} = 1$, $\Phi_1 = 0$, $\Phi_2 = 0$), sampling phase ($\Phi_{INI} = 0$, $\Phi_1 = 1$, $\Phi_2 = 0$) and evaluation phase ($\Phi_{INI} = 0$, $\Phi_1 = 0$, $\Phi_2 = 1$). The operation state of the proposed DAC is depicted in Figure 4. As shown in Figure 4a, during the reset phase, "Φ_{INI}" is set to "1," while Φ_1 and Φ_2 are set to "0." Both top and bottom plates of the sampling-capacitors C_S and the feedback-capacitor C_F are reduced through the switches controlled by Φ_{INI}. Meanwhile, the inverting input node of the operational amplifier is connected to the output node V_{OUT}. As a consequence, the residual charge stored in C_S and C_F inherited from the previous evaluation phase can be thoroughly swept away.



(**a**) reset phase (**b**) sampling phase (**c**) evaluating phase

Figure 4. Operation states of our proposed buffer-reused two-stage DAC according to the operation phases: (**a**) the reset phase, (**b**) the sampling phase and (**c**) the evaluation phase.

The operation state of the sampling phase is described in Figure 4b. During this phase, "Φ_{INI}" dips to "0" and "Φ_1" rises to "1." The top plates of the sampling-capacitors C_S are connected to the inverting input node of the operational amplifier and the bottom plates of the two sampling-capacitors C_S are respectively connected to the selected voltages V_{MSB} and V_{LSB}, which are calculated and fed by the 1st stage sub-DAC. Since "Φ_2" remains "0," the inverting input node and the output node of the operational amplifier keep short. At the end of this phase, the total charge stored at node A, Q_{AS} can be expressed as:

$$Q_{AS} = (V_{COM} - V_{MSB})C_S + (V_{COM} - V_{MSB})C_S + V_{COM}C_F = (2V_{COM} - V_{MSB} - V_{LSB})C_S + V_{COM}C_F, \quad (4)$$

where V_{COM} represents the common-mode voltage of the operational amplifier.

As illustrated in Figure 4c, during the evaluation phase, "Φ_1" dips to "0" and "Φ_2" rises to "1." The bottom plates of the two sampling-capacitor C_S are connected no longer to the selected voltages V_{MSB} and V_{LSB} but to the ground V_{SS}. Additionally, the bottom and top plates of the feedback-capacitor C_F are respectively connected to the output node and the inverting input node of the operational amplifier. Thus, charge redistribution occurs between the sampling and feedback-capacitors. Eventually, the updated charge amount stored at node A, Q_{AE} can be calculated as:

$$Q_{AE} = 2V_{COM}C_S + (V_{COM} - V_{OUT})C_F. \quad (5)$$

Since the inverting input node of the operational amplifier, A, has been in the floating state during the sampling phase and evaluation phase, the charge stored at node A will remain consistent. As a result, the following equation can be established.

$$Q_{AS} = Q_{AE} \quad (6)$$

$$V_{OUT} = (V_{MSB} + V_{LSB})\frac{C_S}{C_F}. \quad (7)$$

As mentioned before, the sampling-capacitor C_S and feedback-capacitor C_F are equal to each other. Hence, the output voltage of the proposed DAC can be successfully obtained by substituting Equations (2) and (3) into Equation (7):

$$V_{OUT} = \frac{VGH}{2^7}\sum_{i=0}^{i=6} 2^i D_{i+3} + \frac{VGH}{2^{10}}\sum_{i=0}^{i=2} 2^i D_i = \frac{VGH}{2^{10}}\sum_{i=0}^{i=9} 2^i D_i. \quad (8)$$

Apparently, Equation (8) indicates that the output voltage of the proposed buffer-reused 10-bit two-stage DAC exactly coincides with that of the standard 10-bit DAC. In other words, the proposed buffer-reused DAC is capable of effectually fulfilling the 10-bit digital-to-analog converting operation and its feasibility is thus demonstrated.

Compared with the conventional two-stage R-C DAC discussed in Section 2.1, our proposed buffer-reused 10-bit DAC exhibits evident superiority in area-efficiency. The competitive advantage primarily stems from the following aspects. On one hand, since part of the functionalities of the large number of switches and capacitors is implemented by a compact internal buffer, the proposed 10-bit DAC merely consists of a compact 7-bit one-voltage selector and a tiny 3-bit one-voltage selector in its 1st stage sub-DAC, rather than a complicated 7-bit two-voltage selector. Hence, the switch number, as well as the relevant routing wires, can be significantly decreased. Moreover, the capacitor size in our proposed DAC is also declined from 8 *C* to 3 *C*. On the other hand, by elaborately reusing the indispensable output buffer in the column driver, we can expediently obtain the 2nd stage sub-DAC without designing an intricate and power-consuming dedicated amplifier. So, the buffer capacity requirement can be successfully minimized. Consequently, the area dimension of the proposed buffer-reused DAC can be effectively narrowed. In addition, if we use metal-insulator-metal (MIM) capacitors in layout design, the die area can be further reduced by placing the capacitors over the voltage selectors in the 1st stage sub-DAC.

3. Output Buffer

In the AMOLED column driver, the DACs are responsible for converting the input graphic data from the digital domain to the analog domain and the output buffers drive the data line of the pixel array to the voltage levels produced by the DACs within one horizontal scanning time. The output buffers determine the performance of the entire column driver in terms of speed, resolution, voltage swing and power dissipation [17]. Recently, high resolution is required and the number of data lines on the display panel has increased. The output buffer must meet much more strict requirements to accommodate high-resolution display, such as short setting time, large voltage swing, low power dissipation, et al. Moreover, the output buffer is reused in our proposed DAC to fabricate the sample-and-hold circuit, so its area should also be minimized. Based upon the above analysis, we adopt the rail-to-rail class B amplifier, which features large transient driving capability, little static current and small die area, as the output buffer circuit in the proposed column driver [18].

The schematic diagram of the class-B output buffer designed in this work is depicted in Figure 5. It can be roughly divided into four parts, namely bias (*MB1–MB4*), rail-to-rail input stage (*M1–M14*), comparators (*M15–M18*) and the class-B output stage (*M19–M20*). The bias circuit provides appropriate reference voltages for the output buffer. The input stage realizes a rail-to-rail input voltage swing by using complementary transistors. The comparators and the class-B output stage are used to improve the slew rate. The system phase compensation is effectively performed by the zero introduced by the load capacitor C_L and the series compensation resistor R_C.

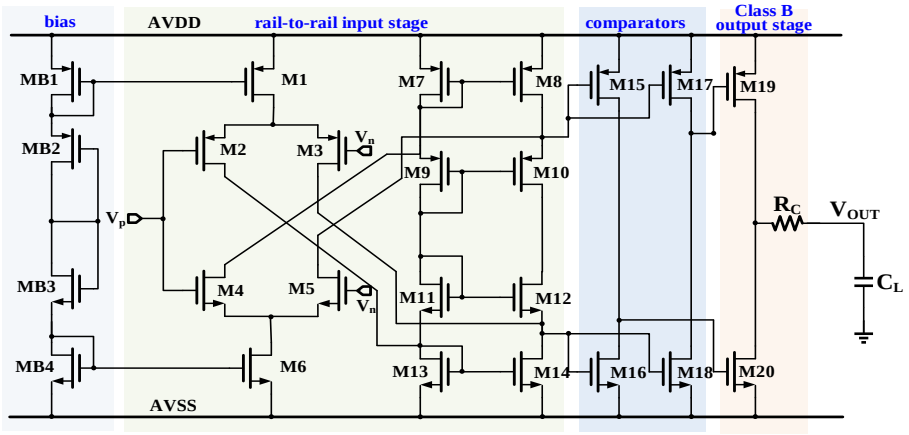


Figure 5. Schematic diagram of the rail-to-rail class-B output buffer.

In the rail-to-rail input stage, the aspect ratios of *M7*, *M9*, *M11 and M13* are designed to be equal to those of *M8*, *M10*, *M12* and *M14*, respectively. In this way, both branches of the complementary differential input stage will draw an equal amount of current during the static state. In order to make the two comparators work properly, the following design conditions should be fulfilled:

$$(W/L)_{15} < (W/L)_8 < (W/L)_{17}\ (W/L)_{18} < (W/L)_{14} < (W/L)_{16}. \quad (9)$$

The operating principle of the output buffer can be explained as follows—In the static state, the current flowing through the two branches of the folded-cascade current mirror is equal. In this case, the gate voltages of *M15* and *M16* are equal to that of *M8* and *M14*, respectively. Hence, the drain current of *M8* and *M14* are mirrored to *M15* and *M16*. More specifically, as $(W/L)_{15}$ is smaller than $(W/L)_8$ and $(W/L)_{16}$ is larger than $(W/L)_{14}$, M_{16} will operate in the triode region while *M15* remains in the saturated region. In addition, the gate voltage *M18* will dip almost to V_{SS}, thus *M18* will be cut off. Similarly, *M19* will be switched off as well. As a result, the output stage will not consume any static power in the static stage. When a negative-going step is applied to the input node, the drain currents of *M8* and *M14* will grow larger and smaller than those of *M7* and *M13*, respectively, so the drain voltages of *M8* and *M14* will drop concomitantly. *M15* will enter into the triode region and *M16* will go into the saturation region. Accordingly, *M19* and *M20* will be respectively switched off and on to discharge the output node with large current. Likewise, if a positive-going step is applied to the input node, *M20* will be cut off and *M19* will be switched on to charge the output node. Consequently, it could be concluded that this buffer draws little current during the static state but possesses an improved driving capability during transient operation.

Generally speaking, Equation (9) is a design rule we should follow to make the current comparators in the class-B output buffer work properly. It is merely determined by the operating principle of the buffer shown and is compatible with any technologies adopted. When implementing the output buffer with more advanced technology, we just need to simultaneously narrow the length and width of the involved transistors and keep the aspect ratio of them satisfying Equation (9). In this way, the presented output buffer can also work correctly with the advanced technology. Hence, technology scaling will not influence the behavior of our design.

4. Experimental Results and Discussion

The prototype column driver IC employing the proposed buffer-reused DAC was fabricated by 0.35 μm two-poly-three-metal (2P3M) BCD (Bipolar, CMOS, DMOS) process technology. The chip contains 6 channels totally and the digital/analog power supply is 3.3 V/5.5 V. Figure 6 illustrates the micrograph of the fabricated chip and the chip test environment. The effective area of each channel is $1100 \times 39\ \mu m^2$.

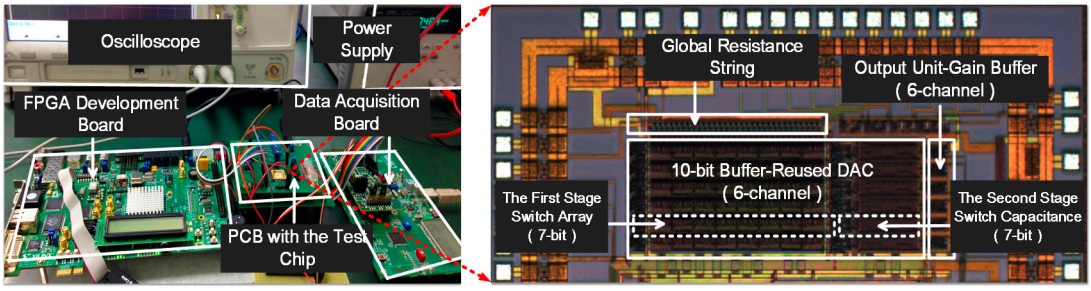


Figure 6. The micrograph of the fabricated chip and the chip test environment.

Specifically, the adequate comparisons of the layout dimensions for (a) the proposed buffer-reused 10-bit DAC, (b) the conventional 10-bit R-C DAC, as well as (c) the widely used 8-bit R-DAC, are depicted in Figure 7. The column driver with our proposed buffer-reused 10-bit DAC gives 42.8% shrinkage of the chip area occupation compared with the column driver with the conventional 10-bit R-C DAC. Even compared with the traditional 8-bit R-DAC with lower conversion accuracy, the proposed buffer-reused 10-bit DAC can still achieve approximately 35.2% shrinkage of the chip area. Hence, Figure 9 demonstrates that our proposed buffer-reused 10-bit DAC is area-efficient.

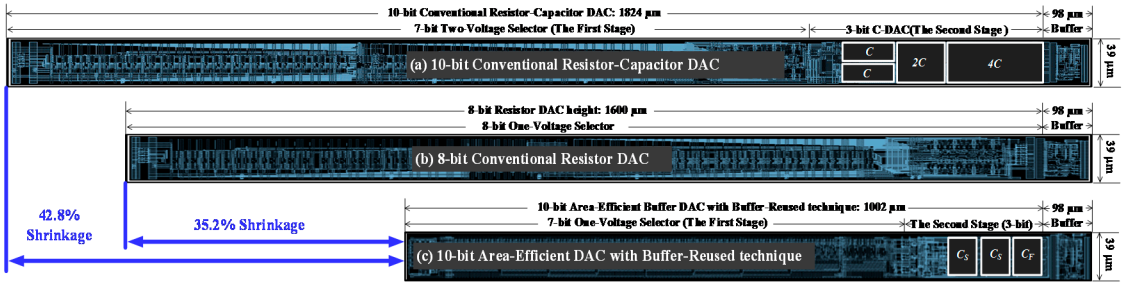


Figure 7. Comparisons of the layout dimensions for (**a**) the proposed buffer-reused 10-bit DAC, (**b**) the conventional 10-bit R-C DAC, as well as (**c**) the widely used 8-bit R-DAC.

In order to verify the functionality, the proposed buffer-reused 10-bit DAC was firstly simulated. Figure 8 shows the simulated transient response when changing the input digital signals from $(000)_{16}$ to $(3FF)_{16}$ with 1.5 kΩ-resistance and 100 pF-capacitance load. In Figure 8, t_{INI}, t_S and t_A represent the time required for the reset phase, the sampling phase and the evaluation phase, respectively. It can be easily figured out that the output voltage of our proposed DAC, namely V_{OUT}, faultlessly retrieves the input signal in the analog domain. Hence, the functionality of the proposed DAC is undisputed.

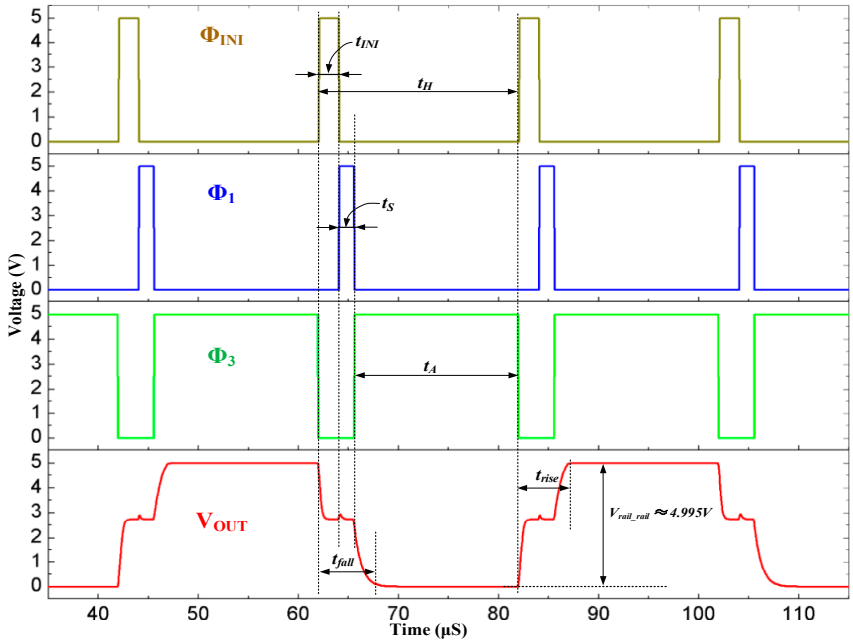


Figure 8. The simulated transient response of our proposed buffer-reused 10-bit DAC.

Furthermore, the fabricated 10-bit column driver employing our proposed buffer-reused DAC was also measured. Figure 9 shows the measured output waveform when changing the input digital signals from $(000)_{16}$ to $(3FF)_{16}$ with 1.5 kΩ-resistance and 100 pF-capacitance load. It can be seen that the output voltage swing of the proposed buffer-reused DAC equals about 4.995 V. Besides, the settling time with 0.1% of the target voltage for a full swing (0–4.995 V) is approximately 5.6 μs. In the case of the 1080-channel column driver IC employing the proposed buffer-reused DAC, the effective horizontal scanning time to drive the full-HD panel at 60 Hz/frame is about 15.43 μs. Hence, the proposed buffer-reused 10-bit DAC can fully meet the driving requirements for full-HD AMOLED applications.

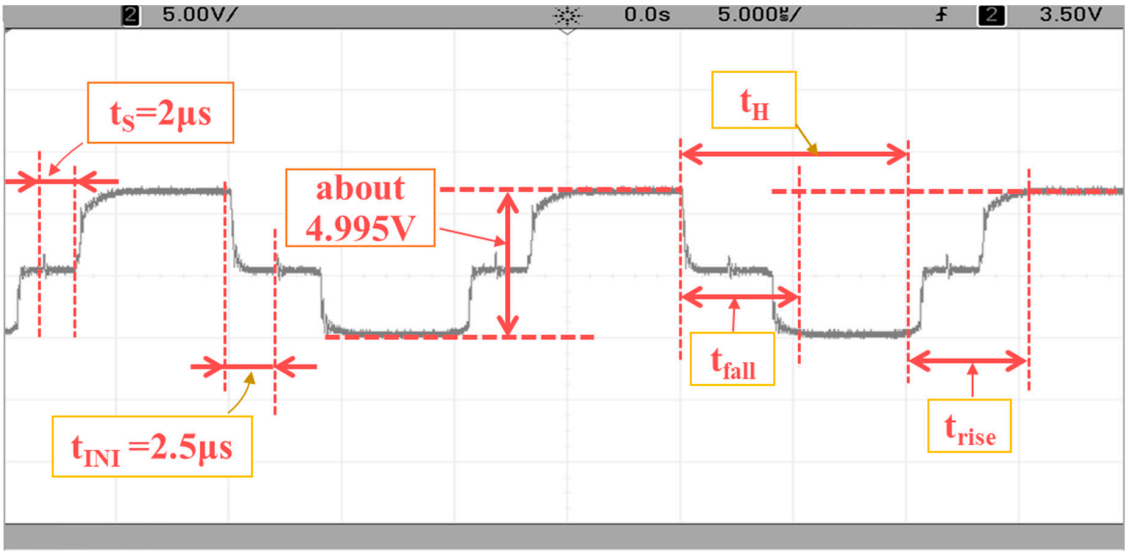
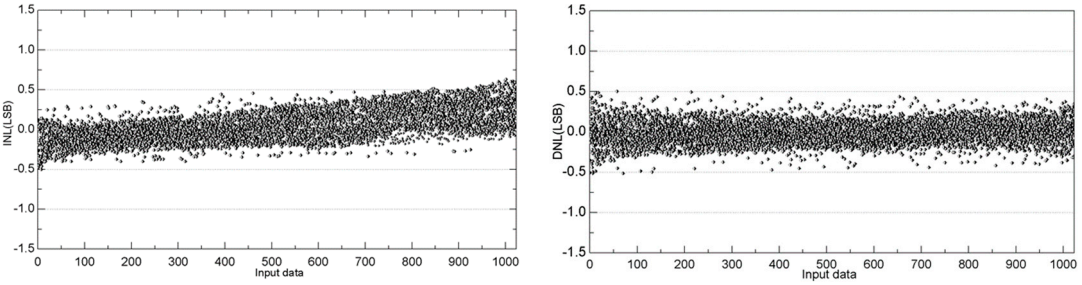


Figure 9. The measured output waveform of the fabricated 10-bit column driver.

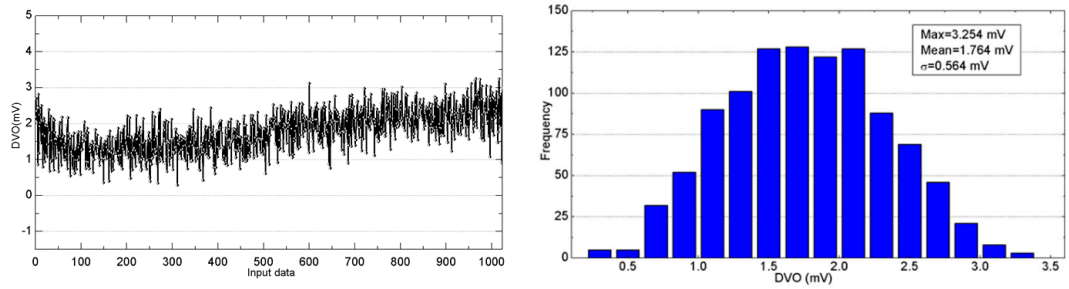
Figure 10 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the fabricated 10-bit column driver. The worst DNL and INL are measured as 0.514 LSB and 0.631 LSB, respectively. Since the AMOLED display driver contains thousands of channels, the uniformity between the channels is also important for the overall image quality. The inter-channel deviation

voltage output (DVO) is the key performance of the column driver which heavily affects the display quality. As shown in Figure 11a, the measured maximum DVO among 6 channels of the fabricated prototype is less than 3.254 mV, which is mainly caused by the offset of the output buffer. Figure 11b presents the statistics of the measured inter-channel DVO. The mean value of DVO is 1.764 mV.



(**a**) (**b**)

Figure 10. The measurement results of our proposed buffer-reused DAC: (**a**) integral nonlinearity (INL) and (**b**) differential nonlinearity (DNL).



(**a**) (**b**)

Figure 11. The measurement results of the buffer-reused DAC: (**a**) deviation voltage output (DVO) (**b**) the statistics of DVOs.

As discussed before, the output buffer is used for driving the highly capacitive column lines of the display panel. So, it should equip with a large slew rate to provide a small settling time. Figure 12 shows measured slow rates and setting time of the fabricated class-B output buffer with different load capacitances. As shown in Figure 12, with the increment of load capacitance, the settling time of the output buffer increases almost linearly. Even if the load capacitance reaches 1000 pF, the output buffer can still provide a sufficient slew rate of about 2.5 V/μs.

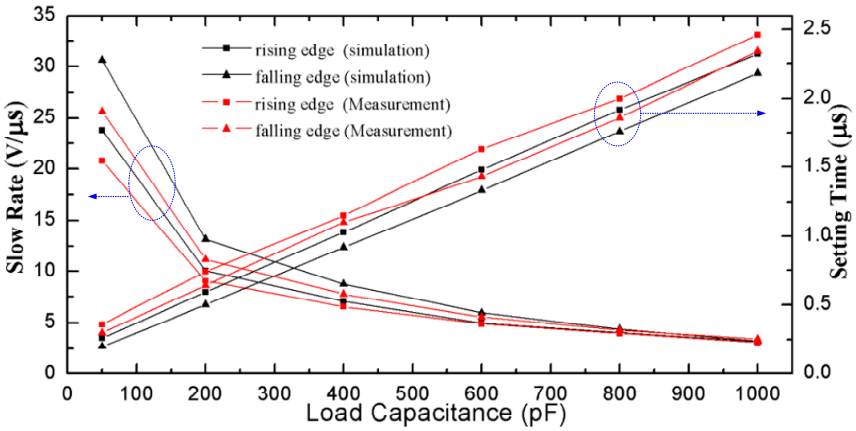


Figure 12. The measured slow rates and setting time for different load capacitances under a voltage swing of 5 V.

Table 1 summarizes the measured performance of the prototype DAC and compares it with the previous state-of-the-art DACs. The measured average area per channel of the column driver IC employing the proposed buffer-reused DAC is 0.0429 mm^2. For ease of comparison, Reference [19] introduced the notation of the normalized size, which represents the consumed channel size for each resolution. Comparing with other DACs, the proposed buffer-reused DAC shows the best performance in normalized size.

Table 1. Performance summary and comparisons.

Parameter	[20]	[21]	[22]	[23]	[24]	This Work
Technology	0.35 μm (N/A)	0.35 μm (2P4M)	0.18 μm (1P4M)	0.18 μm (1P4M)	0.25 μm (N/A)	0.35 μm (2P3M)
Power supply	5 V	3.3 V/5 V	3.5 V	1.8 V/9 V/18 V	5 V	3.3 V/5 V
Gray Scale	10-bit	8-bit	8-bit	10-bit	8-bit	10-bit
INL	2.13 LSB	0.68 LSB	0.75 LSB	N/A	1.31 LSB	0.631 LSB
DNL	1.30 LSB	0.44 LSB	0.56 LSB	N/A	0.21 LSB	0.514 LSB
Max DVO	4.9mV	≥40mV	N/A	16 mv	7.3 mv	3.25 mv
Setting Time R_L/C_L	≤2 μs (Only DAC)	6.8 μs 100 kΩ/10.5 pF	N/A	5.6 μs 5 kΩ/300 pF	2.26 μs 100 kΩ/10.5 pF	5.6 μs 1.5 kΩ/100 pF
Size of One Channel *	0.0526 mm^2	0.0332 mm^2	0.0194 mm^2	0.0212 mm^2	0.0322 mm^2	0.0429 mm^2
Normalized Size **	51.37	129.69	75.78	20.72	125.78	41.89

* Channel width × (DAC height + Output Buffer height). ** ((Size of channel)/($2^{(resolutions)}$)) × 10^6.

Taking Reference [22] as an example, the comparisons between our proposed circuit and other circuits fabricated with different technologies are analyzed as follows:

The power supply is determined by technology. The specified analog power supply in 0.18 μm and 0.35 μm is 3.3 V and 5 V, respectively. Grayscale is merely a design parameter, so it will not be changed with different technologies. INL and DNL are important parameters of DAC because they can evaluate the error and no-linearity of DAC. With the development of CMOS (Complementary Metal Oxide Semiconductor) technology, the process performances such as manufacture accuracy, die uniformity and device matching rate are greatly enhanced. As INL/DNL are strongly influenced by the chip non-uniformity and device mismatching, the circuits fabricated with 0.18 μm technology should show better INL/DNL than that implemented with 0.35 μm technology. Compared with [22], our proposed DAC has comparable INL/DNL even with 0.35 μm technology. This mainly because we employ a switched-capacitor circuit other than resistor-string to fulfill part of the data conversion task and the mismatching rate of capacitors is lower than that of resistors. As for circuit area, it seems like our proposed circuit occupies a larger area than Reference [22] but it can be explained for two reasons. Firstly, our proposed DAC has higher precision than Reference [22]. Since the DAC's area roughly doubles as its precision increases 1bit, directly comparing the area of DACs with different precisions is unfair. Secondly, our proposed DAC was fabricated with less advanced technology. In advanced technologies, the device size is smaller and the required minimum width and spacing of metal and ploy are narrower. Intuitively, the area of the circuits implemented with 0.18 μm technology should be much more compact than that of the same circuits implemented with 0.35 μm technology. Nevertheless, our proposed DAC shows smaller normalized size compared with Reference [22] even it is fabricated with 0.35 μm technology. It should be noted that the size of one channel can be made smaller using the advanced technologies. This can strengthen the fact that our proposed buffer-reused method is effective.

Moreover, although the proposed buffer-reused DAC needs extra phases to sweep out the residual charge and sample the selected voltages, the increase of its driving period is negligible because the reset and sampling phase are both short. The measured maximum settling time for the output to settle to within with 0.1% of the target voltage for a full swing (0–4.995 V) is approximately 5.6 μs, which is competitive. Furthermore, the measured DNL, INL and DVO of the proposed buffer-reused DAC are comparable or superior to other proposals. These results demonstrate that our proposed buffer-reused DAC can successfully minimize the die area while maintaining other required performances.

5. Conclusions

In this paper, a novel area-efficient 10-bit buffer-reused DAC has been thoroughly described, designed, implemented and evaluated. The proposed DAC implements the functionalities of large number of switches and capacitors by a compact internal buffer and minimize the buffer capacity requirement by reusing the indispensable output buffer in the typical column driver. In this way, it can cut down a large number of decoder-switches and capacitors without a dedicated amplifier. Accordingly, the die area of the proposed DAC can be significantly reduced. A prototype 6-channel column driver employing the proposed buffer-reused DAC was implemented in 0.35 µm 2P3M BCD process and its average die size per channel is 0.0429 mm^2, which is 42.8% smaller than that of the conventional R-C DAC. The measured worst DNL/INL are 0.514 LSB/0.631 LSB, respectively. The maximum value of inter-channel DVO is 3.25 mV and the settling time within 5.6 µs is achieved under 1.5 kΩ-resistance and 100 pF-capacitance load. The measurement results indicate that the proposed buffer-reused DAC is suitable for a compact-sized AMOLED display driver with high grayscale and high resolution.

Author Contributions: The design was conceived by Z.H., M.X. and Z.H. performed the experiments, analyzed the data and wrote the manuscript under the supervision of Y.Z., H.W. and S.F. L.T. and N.W. provided technical support for chip implementation. All authors have read and agreed to the published version of the manuscript.

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