

Article

Analysis of Symmetric Dual Switch Converter under High Switching Frequency Conditions

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Abstract: Electric vehicle batteries have the problem of low output voltage, so the application of a high-gain converter is a research hotspot. The symmetrical dual-switch high gain converter has the merits of simple structure, low voltage and current stress, and low EMI. Due to the deterioration of circuit performance caused by circuit parasitic parameters under high frequency operating conditions, the former analysis under low frequency condition cannot satisfy the requirements for performance evaluation. To clarify whether the symmetrical dual-switch high-gain converter can maintain its operating characteristics under high-frequency operating conditions, this paper establishes the converter model considering parasitic parameters, and deduces the sneak circuit modes at high frequency. The effects of parasitic parameters at high frequency on voltage gain, switch stress, and symmetrical operating are analyzed, which is beneficial for the selection and optimization of power devices. This paper believes that considering parasitic parameters may reduce the output gain of the symmetrical double-switch high-gain converter considering parasitic parameters under high frequency conditions, increase the switching stress, and affect the symmetry of the circuit operation when the parasitic parameter values are different. Finally, an experimental platform rated on 200 W with 200 kHz switching frequency is established, and experimental verification is given to verify the analysis.

Keywords: symmetrical dual-switch converter; parasitic parameters; high-frequency; characteristic analysis

1. Introduction

With the increasingly serious problems of environmental pollution and energy crisis, the new energy vehicle battery has gradually become a research hotspot in the field of new energy vehicles [1]. The new energy vehicle battery refers to a kind of power source that provides driving power source for electric vehicles, electric trains, electric bicycles, and other transportation tools. Compared with battery usage scenarios such as the energy supply of electronic and electrical equipment and the energy storage of energy storage power stations, the new energy vehicle battery has to adapt to the harsh usage scenarios of various vehicles. This requires that the battery should have the characteristics of high energy density, high charge and discharge power, high safety, long life, and low cost. Currently, there are many different types of battery technology systems that can provide power for vehicles, including lead–acid batteries, nickel–metal hydride batteries, lithium-ion batteries, supercapacitors, metal–air batteries, etc.

The new energy vehicle battery is the core component of the power system of electric vehicles, and its comprehensive performance directly affects the performance of electric vehicles. Electric vehicle

power battery packs provide traction for electric vehicles and supply energy to vehicle equipment—such as vehicle air conditioners, lighting equipment, etc. Due to the slow dynamic response of the new energy vehicle battery and the large voltage variation range, high gain DC/DC converter is necessary to achieve the high DC (direct current) bus voltage. Compared to isolated converter, the non-isolated high gain converter has the merits such as low cost, high efficiency, convenient to control, and so on [2]. Most of the non-isolated high-gain converters are derived from Boost converter. Commonly used voltage lifting method includes cascading, switched capacitor, and coupled inductors [3–5]. The above-mentioned boost converter has problems such as insufficient gain range, excessive switching stress of the device, and EMI (electromagnetic interference) problems. Compared to the high gain converters, the dual switch converter has the advantages of simple structure, high efficiency, low voltage, and current stress [6], while the asymmetric structure induces the unbalance across the power switches. A symmetric dual switch converter is derived to overcome the above disadvantage, it has the advantages of symmetrical circuit structure, internal voltage clamping, small EMI, etc. The symmetric dual switch converter can realize steady-state and dynamic voltage equalization of switches [7].

The symmetric dual switch converter circuit can reflect the working condition of the circuit based on ideal analysis model at low switching frequency [8]. In order to further improve the power density, a higher switching frequency is required. However, high switching frequency is inflicted with higher switching loss that can considerably reduce the power efficiency of power electronic systems [9]. Therefore, the former analysis under low frequency condition cannot satisfy the requirements for performance evaluation. As a result, many researchers considered parasitic components in their analytical models. Investigations into the effect of parasitic components under high frequency conditions can be summarized as the switching performances of MOSFET (metal-oxide-semiconductor field-effect transistor), switching loss, electromagnetic interference problems, the line current total harmonic distortion of Boost PFC (power factor correction) converter, and the voltage gain of the converter [10–14]. In early research, Gutschmann measured the effects of parasitic components in the power electronic systems by circuit simulations [15]. In Reference [16], the parasitic components were researched individually, the effect of parasitic inductance on MOSFET switching characteristics is studied through experiment. Xiong and Murthy-Bellur have analyzed the impacts of parasitic components and also provided solutions [17]. In Reference [18], the sneak circuit modal analysis method is used to analyze the changes in the operating characteristics of the DCM (discontinuous conduction mode) boost converter after considering the parasitic parameters. After analyzing the effect on gain and stress, the feasibility of the sneak circuit analysis method is proved.

Refer to the analysis content and analysis ideas of the above documents, this paper analyzes the sneak circuit and operating characteristics of the symmetrical dual-switch high gain converter considering parasitic parameters at high frequencies. This paper establishes the converter model considering parasitic parameters, and deduces the sneak circuit modes at high frequency. The effects of parasitic parameters at high frequency on voltage gain, switch stress, and symmetrical operating are analyzed, which is beneficial for the selection and optimization of power devices.

The arrangement of this paper is as follows: in Section 2, the converter model considering devices parasitic parameters at high frequency is established. The sneak modes considering the non-ideal device models are established. In Section 3, the influence of parasitic parameters under high-frequency conditions on the voltage gain, switching stress, and symmetrical operating of the converter is analyzed. The influence of parasitic parameters on the symmetrical performance of the circuit is analyzed. In Section 4, experiments are given to verify the theoretical analysis. Section 5 summarizes the full text of this article.

2. Analysis of Sneak Circuit of Dual-Switch Converter with Parasitic Parameters

The circuit topology of the symmetric dual switch high-gain converter is shown in Figure 1. The converter performs parallel charge and series discharge of L_1 , L_2 by controlling the switch to obtain high voltage gain. Since the voltage of the capacitor is constant in steady-state, the voltage of S_2 is

clamped by C_{o1} and C_{i2} , and the voltage of S_1 is clamped by C_{o2} and C_{i1} . Due to the symmetry of the structure, the converter can achieve the voltage balance of both switches either in steady-state or dynamic-state.

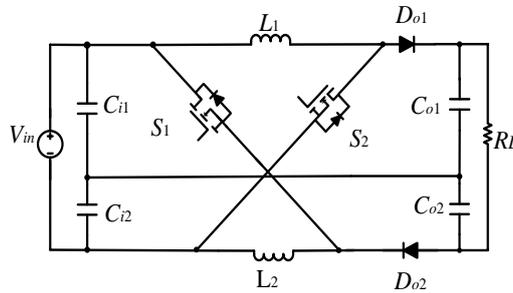


Figure 1. Dual switch step-up DC/DC converter.

For devices in the converter circuit: the inductors L_1, L_2 consider its parasitic resistances R_{L1}, R_{L2} ; diodes D_1, D_2 consider their parasitic capacitors C_{D01}, C_{D02} ; for MOSFET: C_{ds1}, C_{ds2} are the parasitic capacitors between the drain-source, L_{d_in}, L_{s_in} are the parasitic inductor of the drain and the source. R_s, R_d are the external equivalent parasitic resistor of the switch. L_{d_ex}, L_{s_ex} are the external equivalent parasitic inductors of the switch. For the convenience of calculations, let $L_d = L_{d_in} + L_{d_ex}, L_s = L_{s_in} + L_{s_ex}$. The converter model after considering parasitic parameters is given in Figure 2.

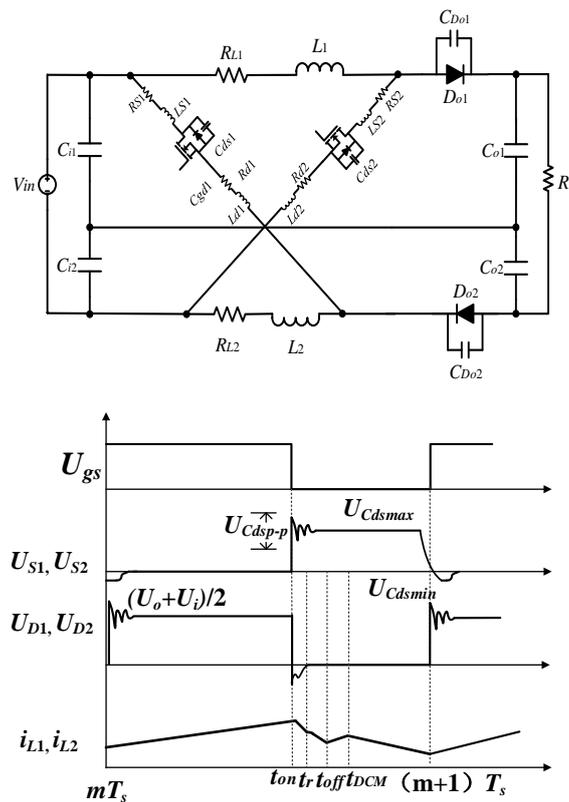


Figure 2. Dual switch step-up DC/DC converter considering parasitic parameters.

Use the mesh combination analysis method to analyze the sneak circuit caused by the parasitic parameters at high frequency. First, establish its undirected graph model as shown in Figure 3 below.

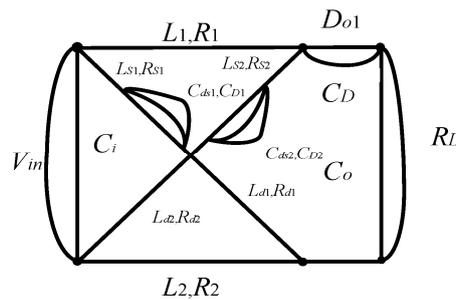


Figure 3. Undirected graph of dual-switch boost converter considering parasitic parameters.

According to the mesh combination analysis method, the maximum number of sub-circuits of the dual-switch converter can be obtained as 236. After removing duplicate sub-circuits, 106 actual sub-circuits are obtained. According to the working principle of the converter, the five effective working modes of the converter are obtained. Comparing these five working modes with the ideal working mode, the three normal modes and two sneak circuit modes caused by parasitic parameters under high-frequency conditions are obtained as follows:

For the convenience of reference, the parameters used in this article are defined as follows: U_{R_s} is the terminal voltage of R_s ; U_{R_d} is the terminal voltage of R_d ; U_{L_s} is the terminal voltage of L_s ; U_{L_d} is the terminal voltage of L_d ; $U_{C_{ds}}$ is the terminal voltage of C_{ds} , $U_{C_{ds,max}}$ is the maximum value of $U_{C_{ds}}$, $U_{C_{ds,min}}$ is the minimum value of $U_{C_{ds}}$, $U_{C_{dsp-p}}$ is the peak-to-peak voltage; I_R is the current of R_s ; I_{R_d} is the current of R_d ; I_{L_s} is the current of L_s ; I_{L_d} is the current of L_d ; $I_{C_{ds}}$ is the current of C_{ds} .

2.1. Analysis of Normal Modes

Mode 1, $t \in [mT_s, t_{on}]$: When the gate drive voltage reaches U_G , the switches are turned on. During this period, the switches S_1, S_2 remain on, and the diodes D_1, D_2 remain off. The power supply V_{in} charges the inductors L_1, L_2 , and the inductor current i_L increases linearly. The load side is powered by C_{o1}, C_{o2} . Its equivalent circuit is shown in Figure 4.

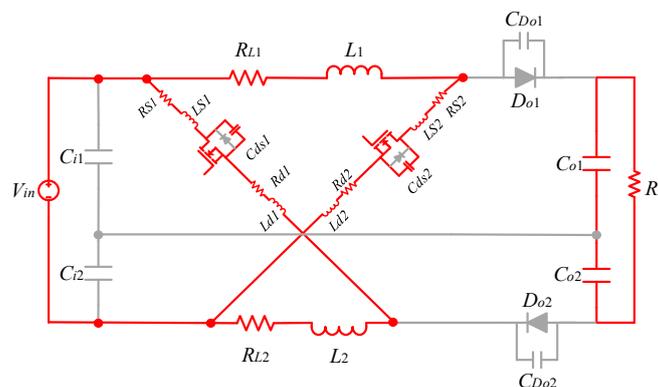


Figure 4. Equivalent circuit of Mode 1.

Mode 2, $t \in [t_r, t_{off}]$: At the time t_r , the diodes D_1, D_2 are still in the conducting state, the energy storage in the power supply and the inductors L_1, L_2 continues to be transferred to the load, and the inductor current i_L decreases linearly. At the same time, all the energy stored in the parasitic inductors L_d, L_s of the MOSFET is released. The equivalent circuit is given in Figure 5.

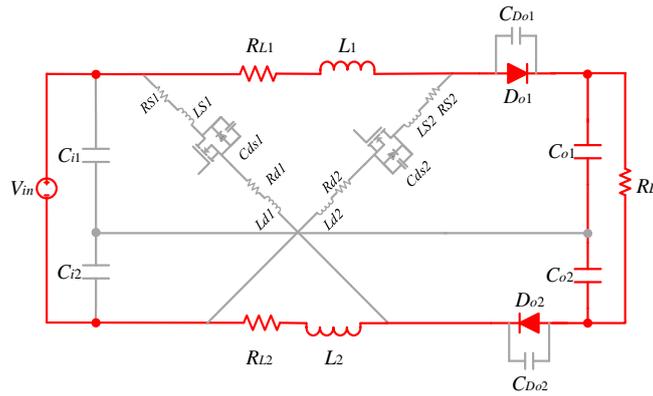


Figure 5. Equivalent circuit of Mode 2.

Mode 3, $t \in [t_{DCM}, (m + 1)T_s]$: Due to the energy consumption of the resistances in the circuit and the parasitic parameters, the inductor current i_L will attenuate to zero at time t_{DCM} . At this time, the inductor current can be regarded as zero, and the output capacitors C_{o1}, C_{o2} continue to provide energy to the load, and their equivalent circuits are shown in Figure 6.

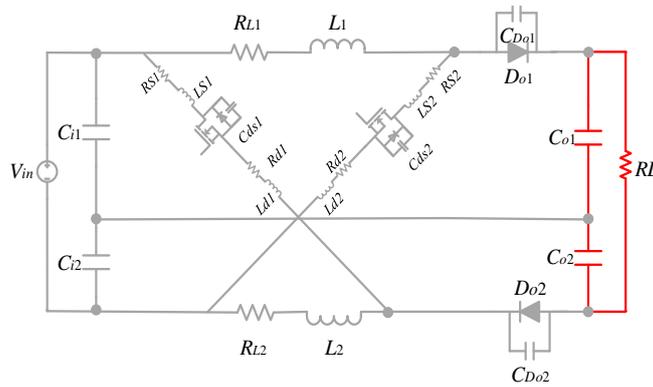


Figure 6. Equivalent circuit of Mode 3.

2.2. Analysis of Sneak Modes

Sneak Mode 1, $t \in [t_{on}, t_r]$: The switches S_1, S_2 are turned off at the time t_{on} , and the inductor current i_L is transferred from the switches S_1, S_2 to the diodes D_1, D_2 , and the energy is transferred to the load end. At the t_{on} moment, the voltage across C_{D01} increases from U_{CDmin} to U_{Cdsmax} , the voltages across C_{ds1}, C_{ds2} increase from U_{Cdsmin} to U_{Cdsmax} . The inductors and the parasitic capacitors in the circuit resonate. The equivalent circuit is shown in Figure 7, and the equations of Sneak Mode 1 can be obtained as

$$\left\{ \begin{aligned} i_{L1\Pi} &= I_{L1}(t_{on})e^{-\frac{R_{L1}+R_{L2}+R_{e2}}{L_1}(t-t_{on})} + \frac{U_i-U_o-U_{CDmax}}{R_{L1}+R_{L2}+R_{e2}} \left[1 - e^{-\frac{R_{L1}+R_{L2}+R_{e2}}{L_1}(t-t_{on})} \right] \\ i_{L2\Pi} &= I_{L2}(t_{on})e^{-\frac{R_{L1}+R_{L2}+R_{e1}}{L_2}(t-t_{on})} + \frac{U_i-U_o-U_{CDmax}}{R_{L1}+R_{L2}+R_{e1}} \left[1 - e^{-\frac{R_{L1}+R_{L2}+R_{e1}}{L_2}(t-t_{on})} \right] \\ U_{C_{dsp-p1}} &= 2 \frac{U_{C_{ds1max}}+U_{CDmax}-U_o}{\omega_1^2 L_{e1} C_{e1}} \\ U_{C_{dsp-p2}} &= 2 \frac{U_{C_{ds2max}}+U_{CDmax}-U_o}{\omega_2^2 L_{e2} C_{e2}} \\ U_{C_{dsmax}} &= \frac{U_o+U_i+U_{CDmax}}{2} - i_{L\Pi} R_s - L \frac{di_{L\Pi}}{dt} \\ U_{C_{dsmin}} &= \frac{U_o+U_i+U_{CDmin}}{2} - i_{L\Pi} R_s - L \frac{di_{L\Pi}}{dt} \end{aligned} \right. \tag{1}$$

$$\begin{cases} C_{e1} = C_{ds1} + \frac{C_{gs1}C_{gd1}}{C_{gs1}+C_{gd1}}, C_{e2} = C_{ds2} + \frac{C_{gs2}C_{gd2}}{C_{gs2}+C_{gd2}} \\ \omega_1 = 2\sqrt{1/L_{e1}} \frac{C_{e1}C_o}{C_{e1}+C_o}, \omega_2 = 2\sqrt{1/L_{e2}} \frac{C_{e2}C_o}{C_{e2}+C_o} \end{cases} \quad (2)$$

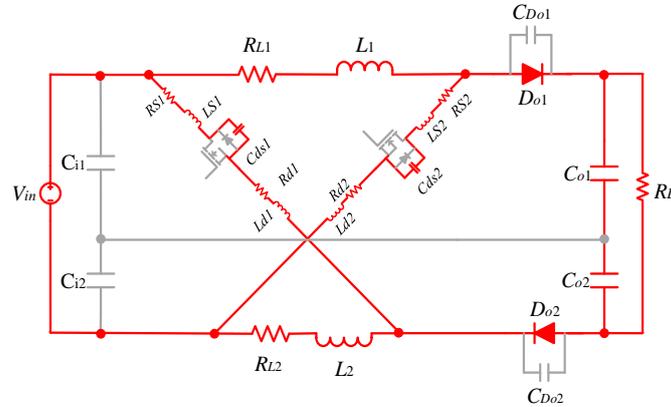


Figure 7. Equivalent circuit of Sneak Mode 1.

It can be seen from the formulas that $U_{C_{ds\ p-p}}$ is very small compared with $U_{C_{ds\ max}}$. If $U_{C_{ds\ p-p}}$ is small enough at time $t > t_{on}$, it can be considered that the operation process of the converter circuit at high frequency will cross the Sneak Mode. Set the boundary value equation as $U_{C_{dsp\ p}}/U_{C_{ds\ max}} = \zeta$. When $U_{C_{dsp\ p}}/U_{C_{ds\ max}} = \zeta$, the converter can skip Sneak Mode 1 operation.

Sneak Mode 2, $t \in [t_{off}, t_{DCM}]$: When the t_{off} time is reached, the inductor current decreases and then increases in the reverse direction, the parasitic capacitor and the inductor resonate, the voltage across the diode’s parasitic capacitor C_D discharges from $U_{C_D\ max}$ to $U_{C_D\ min}$, and the voltage of the switch parasitic capacitor C_{ds} discharges from $U_{C_{ds\ max}}$ to $U_{C_{ds\ min}}$. When the discharge voltage reaches the turn-on voltage of diodes, the diodes are turned on, and the converter then enters the reverse recovery process. The equivalent circuit is shown in Figure 8. Similarly, the equations of Sneak Mode 2 can be obtained as

$$\begin{cases} i_{L1IV} = \frac{U_i - U_o - U_{C_D\ max}}{\omega_1(L_1 + L_2 + L_{e2} + L_{q1})} e^{-\rho_1(t - t_{off})} \sin \omega_1(t - t_{off}) \\ i_{L2IV} = \frac{U_i - U_o - U_{C_D\ max}}{\omega_2(L_1 + L_2 + L_{e1} + L_{q2})} e^{-\rho_2(t - t_{off})} \sin \omega_2(t - t_{off}) \\ U_{C_{D01}} = U_i - U_o - (U_i - U_o - U_{C_D\ max}) e^{-\rho_1(t - t_{off})} [\cos \omega_1(t - t_{off}) + \frac{\rho_1}{\omega_1} \sin \omega_1(t - t_{off})] \end{cases} \quad (3)$$

$$\begin{cases} \rho_1 = \frac{2R_{l1} + R_{e1}}{2L_1}, \rho_2 = \frac{2R_{l2} + R_{e2}}{2L_2} \\ \omega_1 = \sqrt{\frac{1}{L_1(C_D + C_{e1})} - \rho_1^2}, \omega_2 = \sqrt{\frac{1}{L_2(C_D + C_{e2})} - \rho_2^2} \\ C_{r1} = C_D + C_{e1}, C_{r2} = C_D + C_{e2} \\ L_{q1} = \frac{L_{e1}C_{e1}C_D - R_0^2[C_D^2(C_{e1} + C_o) + C_0^2C_{r1}]}{(C_{r1} - \omega_1^2L_{e1}C_{e1}C_D)^2 + \omega_1^2R_0^2(C_{e1}C_D + C_oC_{r1} - \omega_1^2L_{e1}C_{e1}C_D)^2} \\ L_{q2} = \frac{L_{e2}C_{e2}C_D - R_0^2[C_D^2(C_{e2} + C_o) + C_0^2C_{r2}]}{(C_{r2} - \omega_2^2L_{e2}C_{e2}C_D)^2 + \omega_2^2R_0^2(C_{e2}C_D + C_oC_{r2} - \omega_2^2L_{e2}C_{e2}C_D)^2} \end{cases} \quad (4)$$

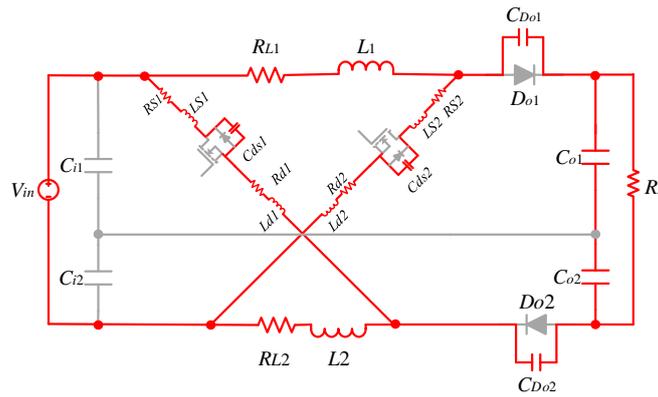


Figure 8. Equivalent circuit of Sneak Mode 2.

The analysis shows that the inductor current i_L in Sneak Mode 2 is a sinusoidal wave with resonant angular frequency ω . Substituting the voltage of C_D into the previous equation, the voltage expression of U_{CD} can be obtained as

$$\begin{cases} U_{CDmin1} = U_i - U_o + (U_i - U_o - U_{CDmax})e^{-\rho_1 \frac{\pi}{\omega_1}} \\ U_{CDmin2} = U_i - U_o + (U_i - U_o - U_{CDmax})e^{-\rho_2 \frac{\pi}{\omega_2}} \\ U_{CDmax1} = (U_i - U_o)(1 + e^{-\rho_1 \frac{\pi}{\omega_1}}) + \frac{2U_o C_{e1}}{C_{e1} + C_D} \\ U_{CDmax2} = (U_i - U_o)(1 + e^{-\rho_2 \frac{\pi}{\omega_2}}) + \frac{2U_o C_{e2}}{C_{e2} + C_D} \end{cases} \quad (5)$$

From the above analysis of the sneak circuit, considering the parasitic parameters of the devices under high-frequency conditions will cause the converter to resonate due to the parasitic junction capacitors and the inductors in the circuit, which will affect the output characteristic of the converter.

In the DCM mode, the circuit modes operation sequences are Mode 1, Sneak Mode 1, Mode 2, Sneak Mode 2, Mode 3. In the CCM (continuous conduction mode) mode, the circuit modes operation sequences are Mode 1, Sneak Mode 1, Mode 2, Sneak Mode 2. The operation process of the circuit in the CCM mode and the DCM mode is shown in the Figure 9 below.

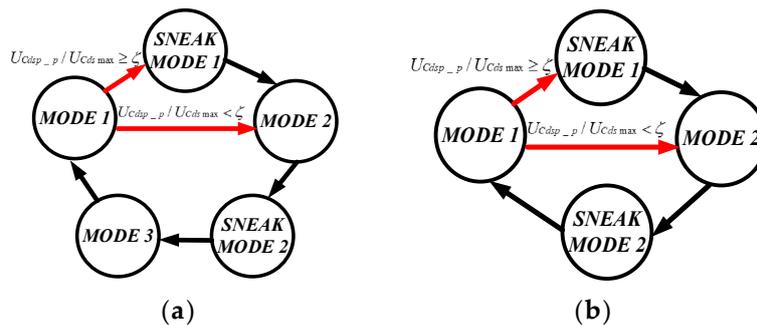


Figure 9. Operation mode conversion diagrams of the converter under two operating modes. (a) The modes of the converter in DCM (discontinuous conduction mode) mode. (b) The modes of the converter in CCM (continuous conduction mode) mode.

3. Considering the Influences of Parasitic Parameters on Converter Characteristic

According to the law of conservation of energy, write the following equation for the column

$$\begin{cases} U_i \int_{mT_s}^{(m+1)T_s} i_L dt = \frac{U_o^2}{R_L} T_s + \int_{mT_s}^{(m+1)T_s} (U_{RL1} + U_{RL2}) i_L dt \\ U_o \int_{mT_s}^{(m+1)T_s} i_0 dt = \frac{U_o^2}{R_L} T_s \end{cases} \quad (6)$$

During $t \in [t_{on}, t_{off}]$ the inductor current satisfies the equation as

$$\int_{t_{on}}^{t_{off}} i_L dt = \frac{1}{2}DT_s I_L(t_{on}) = \frac{U_o}{R_L}T_s - 2C_D(U_{C_D\max} - U_{C_D\min}) \tag{7}$$

Among them, $DT_s = t_{off} - t_{on}$.

3.1. Effects of Parasitic Parameters on Voltage Gain

1. In the Ideal Case

According to the volt-second equilibrium principle and the relationship between i_L and i_D in ideal mode, the voltage gain of an ideal dual-switch step-up converter can be obtained as

$$M = \frac{U_o}{U_i} = \frac{1 + D}{1 - D} \tag{8}$$

2. Considering Parasitic Parameters

According to the volt-second equilibrium principle and the law of energy conservation, the voltage gain of the dual-switch converter with parasitic parameters can be obtained as follows:

Switch on period:

$$U_{L1} = U_{L2} = U_i - U_{R1} - U_{R_e2} \tag{9}$$

Switch off period:

$$U_{L1} = U_{L2} = \frac{1}{2}(U_i - U_o - U_{R_{L1}} - U_{R_{L2}}) \tag{10}$$

Simultaneous equations are obtained:

$$M' = \frac{1 + D - \left[\frac{(R_s + R_d + R_L)}{R_o + f_s C_D (U_{C_D\min} - U_{C_D\max})} + f_s L_e \right] \frac{1 - e^{-2\rho D / f_s}}{R_s + R_d + R_L}}{1 - D} \tag{11}$$

From the above equations, the relationship between input voltage and output voltage is a constant value when the circuit parameters and operating period of the converter are determined in the ideal working state. When the converter considering parasitic parameters, the relationship is an exponentially decreasing expression.

Set the rated parasitic parameters values as follows: $C_{ds} = 232$ pF, $C_D = 60$ pF, $R_s = 0.05$ Ω , $L_e = 147$ nH. In the case where the ideal circuit parameter values are unchanged, the influences of the changes in the values of each parasitic parameter on the output gain characteristics of the converter are shown in Figure 10.

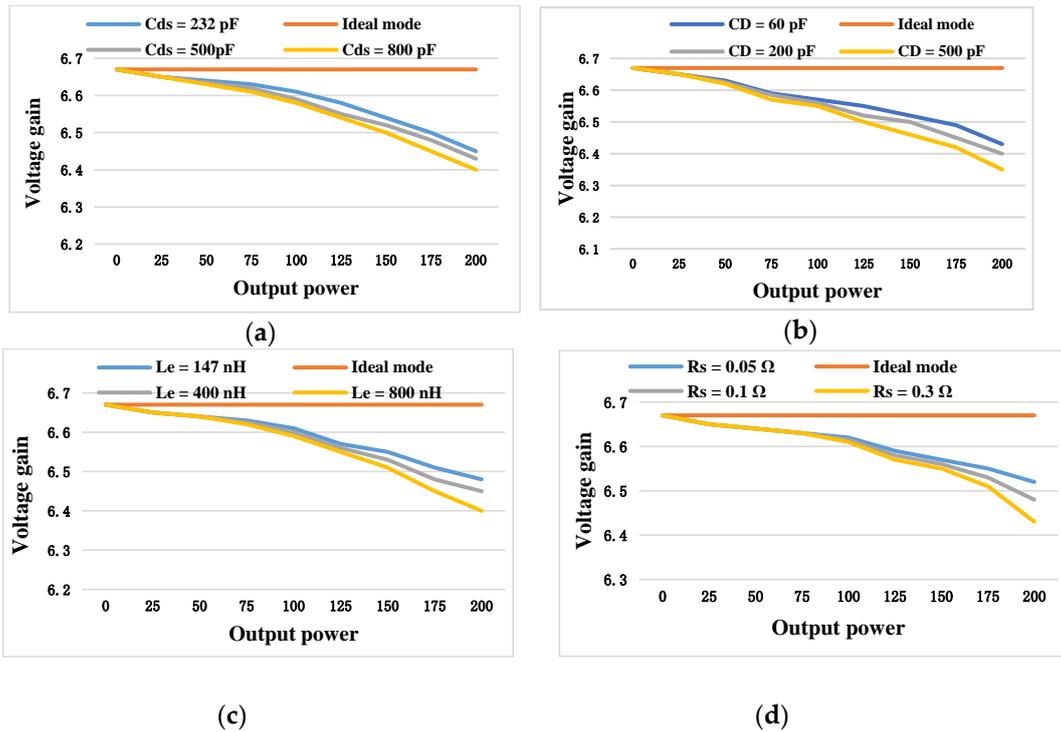


Figure 10. Comparisons of the influence of various parasitic parameters on the output gain. (a) Influences of numerical value of C_{ds} . (b) Influences of numerical value of C_D . (c) Influences of numerical value of C_{ds} . (d) Influences of numerical value of C_{ds} .

The above figures show the results that those four parasitic parameters share the common characteristic: the larger the values of the parasitic parameter, the more obvious the effects of reducing the output gain.

3.2. Effects of Parasitic Parameters on Switch Stress

List the voltage and current stress of the switching devices in the ideal model and the model considering parasitic parameters as follows:

1. Ideal conditions

$$\begin{cases} \bar{I}_S = \frac{U_i}{L_1+L_2}DT_s \\ U_S = \frac{MU_i}{2} \\ \bar{I}_D = \frac{U_i}{L_1+L_2}DT_s \\ U_D = -MU_i \end{cases} \tag{12}$$

2. Conditions considering parasitic parameters

$$\begin{cases} \bar{I}_{S1} = \frac{U_i - U_{C_{ds1min}}}{R_{S1} + R_{L1} + R_{d1}} \left(1 - e^{-\frac{R_{S1} + R_{L1} + R_{d1}}{L_1} t} \right) \\ \bar{I}_{S2} = \frac{U_i - U_{C_{ds2min}}}{R_{S2} + R_{L2} + R_{d2}} \left(1 - e^{-\frac{R_{S2} + R_{L2} + R_{d2}}{L_2} t} \right) \\ U_{S1} = \frac{U_o + U_i + U_{C_Dmax}}{2} - i_{L_{II}} R_s - L \frac{di_{L_{II}}}{dt} + \frac{U_{C_{ds1max}} + U_{C_Dmax} - U_o}{\omega_1^2 L_{e1} C_{e1}} \\ U_{S2} = \frac{U_o + U_i + U_{C_Dmax}}{2} - i_{L_{II}} R_s - L \frac{di_{L_{II}}}{dt} + \frac{U_{C_{ds2max}} + U_{C_Dmax} - U_o}{\omega_2^2 L_{e2} C_{e2}} \\ \bar{I}_D = \frac{U_i - U_{C_{dsmin}}}{R_{S1} + R_{L1} + R_{d1}} \left(1 - e^{-\frac{R_{S1} + R_{L1} + R_{d1}}{L_1} t} \right) \\ U_D = U_{C_{Dmin}} \end{cases} \tag{13}$$

Set the rated parasitic parameter values as follows: $C_{ds} = 232 \text{ pF}$, $C_D = 60 \text{ pF}$, $R_s = 0.05 \text{ } \Omega$, $L_e = 147 \text{ nH}$. The voltage stress of the ideal model and the model considering the parasitic parameter are shown in Figure 11 below.

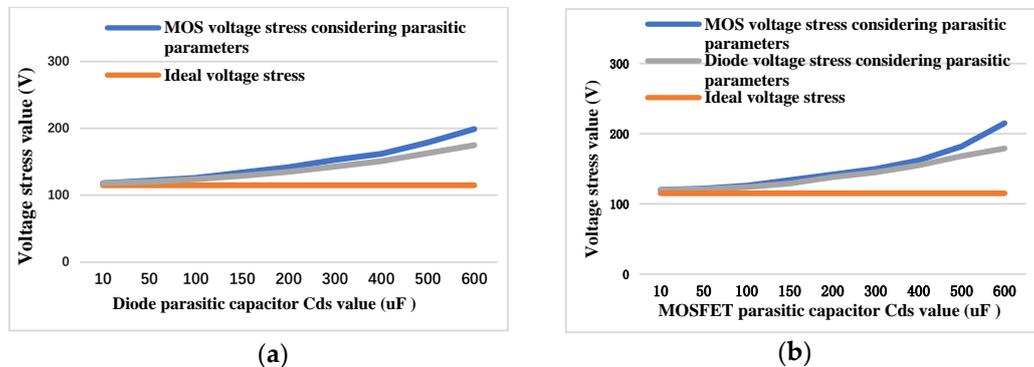


Figure 11. Comparisons of the influence of various parasitic parameters on the output gain. (a) The effects of the C_{ds} on the switching stress. (b) The effects of C_D on switching stress.

It can be seen from the above figures that, compared with the voltage stress under ideal conditions, the voltage stress when considering parasitic parameters of the converter is greater. The larger the values of the parasitic capacitors, the larger the amplitude of the resonance voltage of the switches. If the device selection does not consider the impacts of the inductor current fluctuations and the switching stress differences, it may cause new modes or circuit failures in the circuit, which means the selections of devices in circuits under high-frequency conditions must take the effects of parasitic parameters into account.

3.3. Influence of Parasitic Parameters Asymmetry on Circuit

In the ideal model, due to the symmetrical structure of the converter, the voltage balance of the switches S_1, S_2 can be achieved under both steady-state and dynamic conditions, and the centerline has no charge and discharge current. However, if the parasitic parameter values are different for the same type of devices, the symmetric circuit will present an asymmetric working state, which will bring adverse effects on the performance of the converter.

The analysis equations about the voltages of the MOSFET in the sneak modes is re-written in this paper to get the expressions of the voltage difference of the parasitic capacitors of the MOSFETs as follows:

$$\Delta U_{C_{ds}} = \frac{U_{C_{D01max}} - U_{C_{D02max}}}{2} - i_{L_{II}}(R_{s1} - R_{s2}) - (L_1 - L_2) \frac{di_{L_{II}}}{dt} \tag{14}$$

The analytical equations for the inductor current and diode voltage in Sneak Mode is re-wrote in this paper to get the difference expressions as follows:

$$\left\{ \begin{aligned}
 i_{L1IV} &= \frac{U_i - U_o - U_{C_D01max} - U_{C_D02max}}{\omega_{r1}(2L_1 + L_{e2} + L_q)} e^{-\rho_1(t-t_{off})} \sin \omega_{r1}(t - t_{off}) \\
 i_{L2IV} &= \frac{U_i - U_o - U_{C_D01max} - U_{C_D02max}}{\omega_{r2}(2L_2 + L_{e1} + L_q)} e^{-\rho_2(t-t_{off})} \sin \omega_{r2}(t - t_{off}) \\
 U_{C_{ds}01} &= \frac{U_i - U_{C_{ds}1min}}{R_{S1} + R_{L2} + R_{d1}} (1 - e^{-\frac{R_{S1} + R_{L2} + R_{d1}}{L_1} t}) \frac{\rho_1}{\omega_{r1}} \sin \omega_{r1}(t - t_{off}) \\
 U_{C_{ds}02} &= \frac{U_i - U_{C_{ds}2min}}{R_{S2} + R_{L1} + R_{d2}} (1 - e^{-\frac{R_{S2} + R_{L1} + R_{d2}}{L_2} t}) \frac{\rho_2}{\omega_{r2}} \sin \omega_{r2}(t - t_{off}) \\
 U_{C_D01} &= (U_i - U_o - U_{C_D01max} - U_{C_D02max}) e^{-\rho_1(t-t_{off})} [\cos \omega_{r1}(t - t_{off}) + \frac{\rho_1}{\omega_{r1}} \sin \omega_{r1}(t - t_{off})] \\
 U_{C_D02} &= (U_i - U_o - U_{C_D01max} - U_{C_D02max}) e^{-\rho_2(t-t_{off})} [\cos \omega_{r2}(t - t_{off}) + \frac{\rho_2}{\omega_{r2}} \sin \omega_{r2}(t - t_{off})] \\
 \rho_1 &= \frac{2R_{L1} + R_{e1}}{2L_1}, \rho_2 = \frac{2R_{L2} + R_{e2}}{2L_2} \\
 \omega_{r1} &= \sqrt{\frac{1}{L_1(2C_D + C_{e1})} - \rho_1^2} \\
 \omega_{r2} &= \sqrt{\frac{1}{L_2(2C_D + C_{e2})} - \rho_2^2}
 \end{aligned} \right. \quad (15)$$

The influences of the parasitic parameters C_{ds} , C_D are reflected in the influences on the oscillation frequency ω_r and equivalent inductor Lq . The influences of the parasitic parameter R_L are reflected in the influences on oscillation frequency ω_r , equivalent parameter ρ , and equivalent inductor Lq . The change of parasitic parameters will result in different inductor current values of i_{L1} , i_{L2} , and the occurrence times of the resonance currents, which makes the charge and discharge currents appear in the centerline of the circuit. The two MOSFETs and diodes have different resonance amplitudes and resonance appearance times. The operation symmetry of the circuit is destroyed, which may cause new modalities or circuit failures. Draw the waveform of the stress difference formulas considering the parasitic parameters as shown in Figure 12.

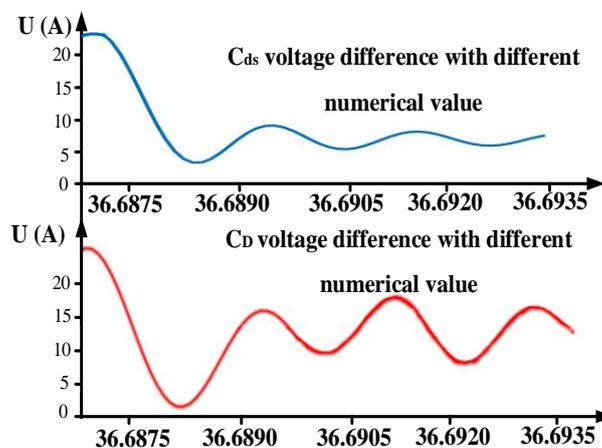


Figure 12. Waveforms of voltage stress with different parasitic parameter values.

4. Simulations and Experiment Verification

An experimental platform for the symmetric dual switch high-gain converter is built in the laboratory. The devices selections and parameter values settings of the experimental platform are shown in Table 1.

Table 1. Parameter values of devices.

Components	Parameter Values
U_i/U_o	30–50 V/200 V
F_S	200 kHz
S_1, S_2	IRFP250
D	SF24
C_D	126 pF
L_{d1}, L_{d2}	135 nH
L_{s1}, L_{s2}	12 nH
C_{ds1}, C_{ds2}	232 pF
R_L, R_d	0.05 Ω
R_{s1}, R_{s2}	0.1 Ω
C_{D01}, C_{D02}	60 pF

4.1. Simulations in Saber

The simulated waveforms of the inductor current, switch voltage and diode voltage are shown in Figure 13. The inductor current waveform shows a trend of first rising and then falling. The inductor current, MOSFET voltage, and diode voltage waveforms are all resonant. Compared with ideal conditions, the voltage amplitudes of MOSFETs and diodes are increased due to the influences of resonance when considering parasitic parameters under high-frequency conditions.

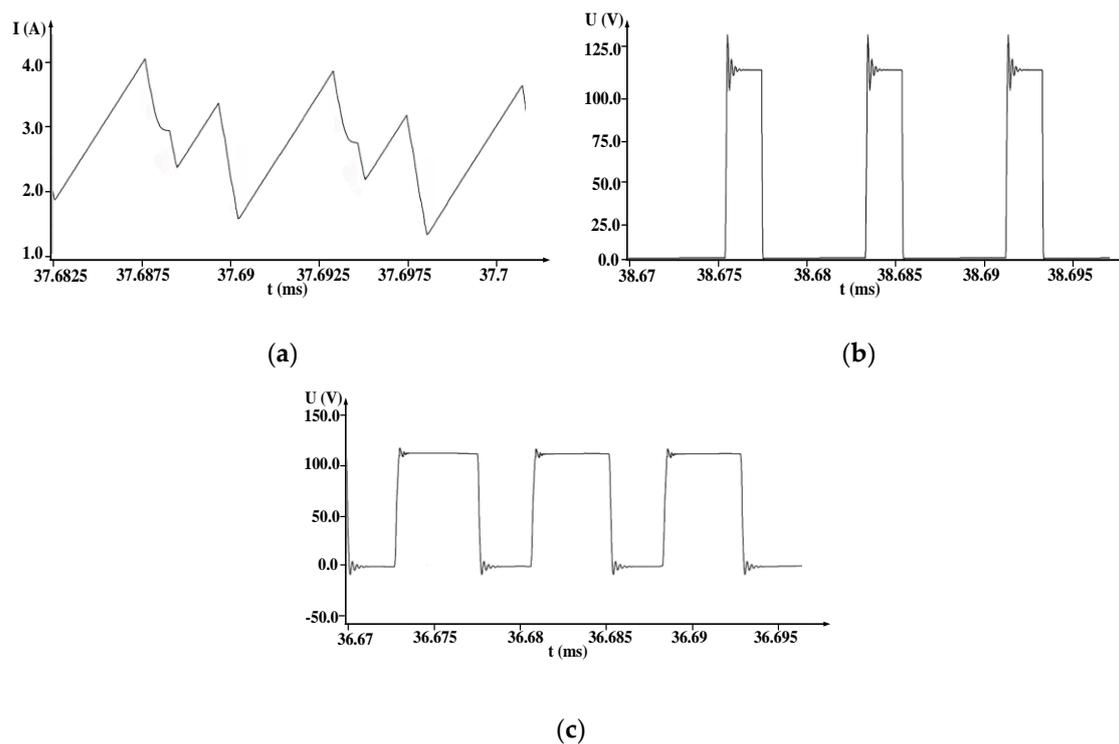


Figure 13. Circuit waveforms obtained through Saber simulation. (a) Simulation waveform of inductor current. (b) Simulation waveform of MOSFET (metal-oxide-semiconductor field-effect transistor) voltage. (c) Simulation waveform of diode voltage.

The simulation waveforms show that, due to the high-frequency resonance under high-frequency conditions, the amplitudes of inductor currents, MOSFET voltage and diode voltage all increases due to the parasitic capacitors resonate with the inductors in the sneak circuit, in line with the previous analysis.

4.2. Experimental Verification

The experimental platform of the dual-switch high-gain converter built in the laboratory is shown in the Figure 14 below.

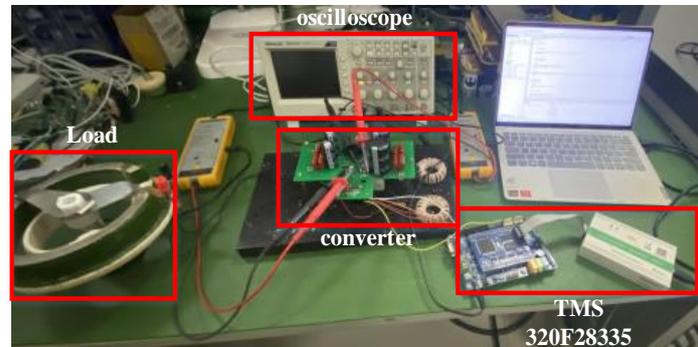


Figure 14. Experiment platform.

The parasitic parameter values of the devices are set as $R_{S1} = R_{S2} = 0.05 \Omega$, $C_{ds1} = C_{ds2} = 232 \text{ pF}$, in the case of symmetrical parasitic parameters, the experimental waveforms of $P_o = 200 \text{ W}$ are shown in Figure 15.

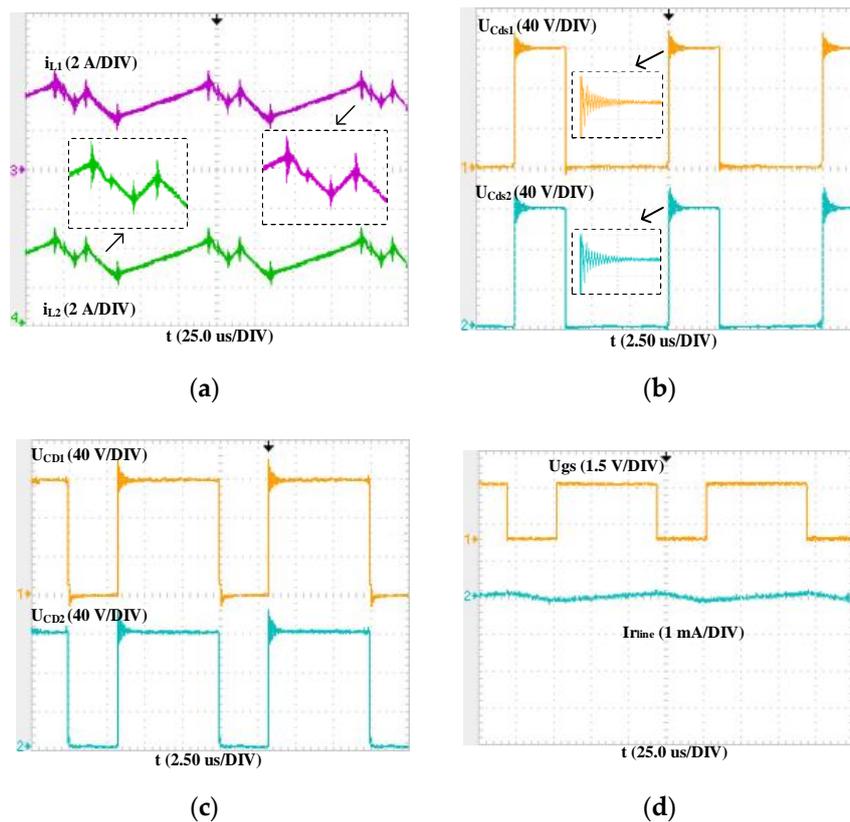


Figure 15. Experimental waveforms considering parasitic parameters for $P_o = 200 \text{ W}$. (a) Experimental waveform of inductor current. (b) Experimental waveform of MOSFET voltage. (c) Experimental waveform of diode voltage. (d) Experimental waveform of centerline current.

After the output power in the original experiment is adjusted from 200 W to 80 W, the diagrams of the experimental waveforms of $P_o = 80 \text{ W}$ are shown in Figure 16. From the diagrams of the

experimental waveforms, the amplitude of the current resonance reduces 0.4 A, and the amplitude of the MOSFET voltage reduces 8.5 V, which confirms the theoretical analysis.

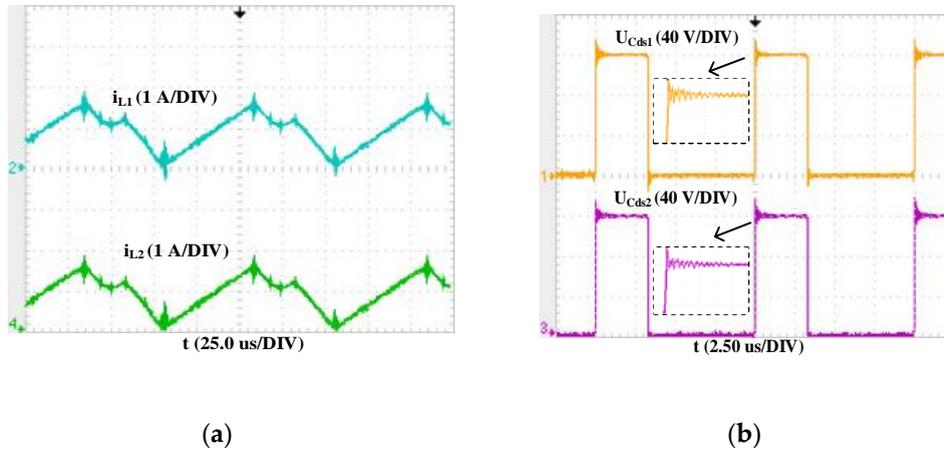


Figure 16. Experimental waveforms considering parasitic parameters for $P_o = 80$ W. (a) Inductor current experimental waveform. (b) MOSFET voltage (U_{Cds}) experimental waveform.

To verify the effects of different parasitic parameter values of the same type of devices on the converter under high-frequency conditions, the value of the parasitic resistance R_{L2} is adjusted from 0.05Ω to 0.1Ω . The experimental waveforms of $P_o = 200$ W are shown in Figure 17 below.

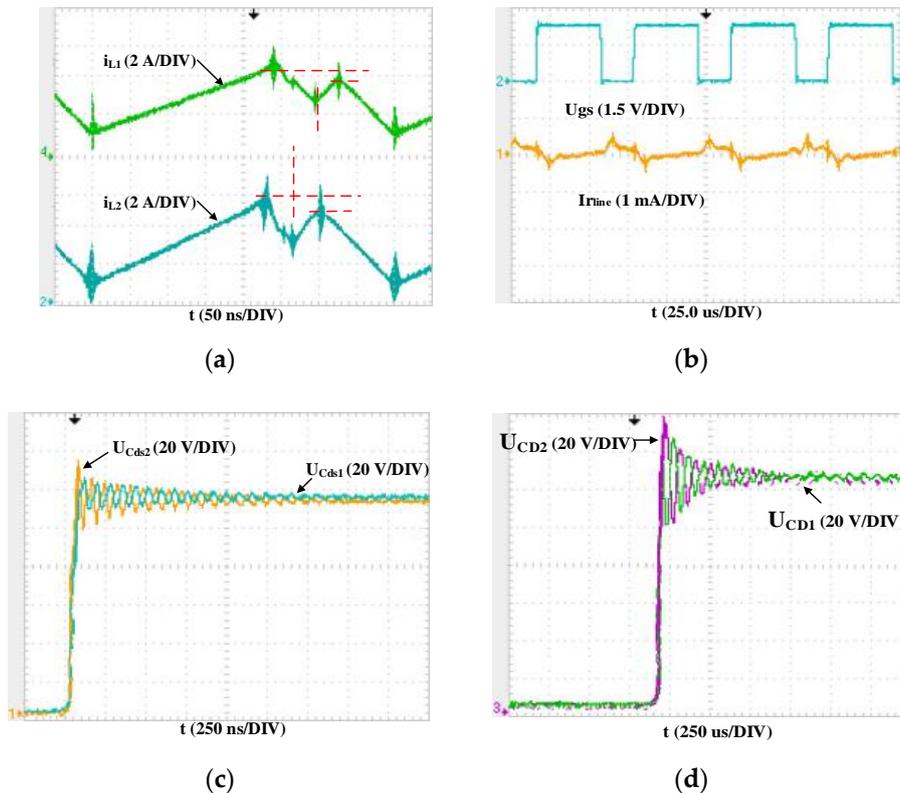


Figure 17. Experimental waveforms considering parasitic parameters for $P_o = 200$ W after the parasitic parameter R_{L2} value is changed. (a) Experimental waveform of inductor current. (b) Experimental waveform of centerline current. (c) Experimental waveform of MOSFET voltages. (d) Experimental waveform of diode voltages.

4.3. Comparative Analysis of Simulation and Experimental Waveforms

The resonance current amplitudes values in experimental waveforms Figure 15a are $i_{L1} = 8.8$ A, $i_{L2} = 8.7$ A, and resonance current amplitudes values in simulation waveforms Figure 13a are $i_{L1} = 8.9$ A, $i_{L2} = 8.7$ A. The amplitudes are almost the same.

By comparing the experimental waveforms, the simulation waveforms, and theoretical analysis of the inductor currents, it can be known that the analysis of the influences of the parasitic parameters on the inductor currents is in line with the actual working situations.

The resonance voltage amplitudes values in experimental waveforms Figure 15b are $U_{Cds1} = 188$ V, $U_{Cds2} = 183$ V, and voltage amplitudes values in simulation waveforms Figure 13b are $U_{Cds1} = 187$ V, $U_{Cds2} = 184$ V. The experimental waveforms of MOSFETs resonant voltages are consistent with the simulated waveforms.

From above analysis, it can be known that the parasitic capacitors and the inductors in the circuit resonate under high-frequency conditions, and the amplitudes of the voltages are increased by the influences of resonance, which is consistent with the conclusions obtained from theoretical analysis.

From the above experimental waveform Figure 17a, it can be seen that the resonance current peak value of the inductor current i_{L2} is enhanced by 0.64 A compared to i_{L1} , and the appearance time is advanced by 8.3 μ s. Since the inductor currents i_{L1} and i_{L2} no longer maintain the same phase and amplitude, the centerline will have charge and discharge currents. Experimental waveform Figure 17b shows the current in the converter centerline to prove this conclusion. Through the above analysis of the experimental waveforms of the inductor currents i_{L1} and i_{L2} in the asymmetric condition, it can be known that the symmetry of the ideal symmetric dual switch high-gain converter will be destroyed and the dynamic balance characteristics of converters will be affected when considering parasitic parameters under high-frequency conditions.

From the experimental waveform Figure 17c, it can be seen that the peak value of the resonance voltage U_{Cds2} increases by 7 V than U_{Cds1} , and the phases of the two voltages U_{Cds1} , U_{Cds2} are no longer the same. From the waveform Figure 17d, it can be seen that the peak value of the resonance voltage U_{CD02} increases by 13 V than U_{CD01} , and the phases of the two voltages U_{CD01} , U_{CD02} are different. Through the above analysis, it can be known that the amplitudes of the resonance voltages of MOSFETs and diodes no longer maintains the same values after considering the parasitic parameters values asymmetry, which puts more precise requirements for the selection of devices and the selection of device-rated voltages in actual applications.

From the above experimental waveforms, it can be seen when the values of the parasitic parameters become larger, the voltage stress values of the corresponding switches will be greater. Through the comparisons of experimental waveforms with the same and different parasitic parameter values, it can be seen that when the parasitic parameter values of the devices are different, the symmetry of the ideal symmetric dual switch high-gain converter will be destroyed and the dynamic balance characteristics of converters will be affected and the resonance voltages amplitudes of the MOSFETs are no longer the same, which puts more precise requirements for the selections of devices and the selections of device rated voltages in actual high-frequency application conditions.

A comparison of voltage gains obtained from the experiment and calculation is shown in Figure 18.

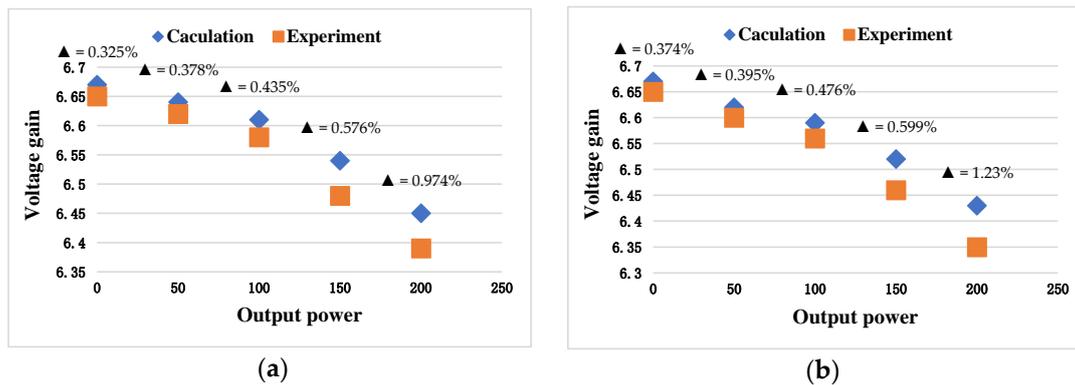


Figure 18. Experimental and calculated voltage gain under different cases. (a) Condition 1. (b) Condition 2.

In Condition 1, the values of parasitic parameters are: $C_{ds} = 232$ pF, $C_D = 60$ pF, $R_s = 0.05$ Ω , $L_e = 147$ nH. In Condition 2, the values of parasitic parameters are: $C_{ds} = 232$ pF, $C_D = 120$ pF, $R_s = 0.1$ Ω , $L_e = 147$ nH. The different values in Figure 18 are acquired by adding external capacitors, inductors, and resistors across the device terminals. Figure 18 proves that by varying the values of parasitic parameters while other parameters remain unchanged, the greater the parasitic parameter values, the more obvious the impacts on the output gain, which consistent with theoretical results. The results of the theoretical analysis and experiments verify that the sneak circuit phenomena can be reduced by choosing the value of parameters appropriately, which means higher requirements for the selection and optimization of power devices.

5. Conclusions

This paper takes the symmetrical dual-tube high-gain converter as the research object, and analyzes the characteristics of the high-frequency down-converter considering the parasitic parameters. A model of the symmetrical dual-switch high-gain converter considering parasitic parameters is established, and two sneak operating modes—Sneak Mode 1 and Sneak Mode 2—are found through sneak circuit analysis. Through the analysis of operating characteristics, it is found that considering the parasitic parameters of devices such as C_{ds} , C_D , R_L , L_S , L_d , and R_S under high frequency will reduce the voltage gain, increase the switching stress, and affect the symmetry of the circuit operation when the parasitic parameter values are different. Finally, the conclusions obtained through simulation and experiment are consistent with the theoretical analysis, which proves the correctness of the above analysis. The analysis of the working characteristics of the converter under high frequency in this paper has certain reference value for the selection of devices and the selection of margin under high frequency.

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