Article

Design, Analysis, and Implementation of an Equalizer Circuit for the Elimination of Voltage Imbalance in a Half-Bridge Boost Converter with Power Factor Correction

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Abstract: For the implementation of a boost converter, the half-bridge topology provides a simpler conversion circuit; however, the voltage imbalance between the capacitors is a critical factor since traditional control methodology decreases the power factor when correcting the imbalance. Consequently, this paper proposes a circuit to correct such imbalance keeping the power factor at the same time. Then, this work carries the analysis, simulation, and implementation of a strategy to reduce voltage imbalance in a half-bridge boost converter with correction of the power factor. The first part offers a description of the equalizer circuit; then, an average model is employed to perform the mathematical analysis. Later, a comparison via simulation is undertaken including other conventional converters in different scenarios. Moreover, an experimental laboratory setup is made; the results show that the equalizer circuit reduces voltage imbalance between the capacitors in a half-bridge booster converter.

Keywords: control; half-bridge boost; power electronics; power factor correction; voltage imbalance

1. Introduction

In electrical engineering, it is essential to supply power to the wide variety of devices connected to the network, achieved by energy conversion [1]. The devices connected to the network range from domestic use lamps to more complex technologies such as electrical microgrids [2]. The majority of distribution systems operate with alternating current (AC); thus, it is necessary to use power converters that serve as an interface to supply the electronic loads with direct current (DC). This is done through electronic converters; but means an issue for distribution networks since their operation includes harmonic currents, the injection of reactivities to the system, and the increase of the total harmonic distortion (THD) [3].

On the other hand, circuits with power factor correction (PFC) are a way to reduce the inconveniences generated by this type of converters. Circuits with PFC allow limiting harmonic currents while decreasing the THD value seen from the network, improving the efficiency of the conversion circuit [4]. With this approach, the waveform of the current supplied presents a sinusoidal behavior with a small phase angle between the current and the voltage, so that from the point of view of the network the load behaves in an almost resistive way [5,6].

According to [7], the high efficiency and power factor of converters are very important since can improve the electrical system's quality. Boost power factor correction via critical conduction mode (CRM) control, and power on control and valley detection technique are applied to converters with

PFC in electrical appliances, mainly light loads. However, these control schemes have low-efficiency problems due to a sudden increase in the switching frequency with light loads and low power factor associated with the limitation of the power on time.

Different converters with PFC have been implemented evaluating the efficiency under load conditions, such as the cascade buck-boost [8], Ćuk converter [9], flyback circuit [10] and boost converter [11]. In this regard, the boost converter has greater efficiency as it can operate in a wide range of loads in continuous and discontinuous mode [12]. Two of the most widely used variations of this converter are half-bridge and full-bridge topology. The half-bridge provides a simpler conversion circuit using fewer switching devices although it requires the use of an additional capacitor [6].

Regarding the applications using converters with power factor correction, in [10] the power-factor-correction converter of a single-stage forward-flyback with quasi-resonant (QR) control is studied. This uses a flyback and direct converters through a common transformer. Only the flyback sub-converter works when the input voltage is less than the reflected output voltage, while both the flyback sub-converter and the direct sub-converter operate to share the output power in the repose region. Other application for Ćuk-type converters can be seen in [13], where a control system for this converter is used to supply power to a fed brushless DC motor. For the design of the controller, moth-flame optimization (MFO) is used to make the settings of a fuzzy logic controller (FLC). The proposed Ćuk converter works in discontinuous conduction mode (DCM) to achieve better power factor.

An attractive control strategy to implement converters with PFC is predictive control; thus, reference [11] presents a digital predictive control strategy for a single-phase boost PFC converter. Considering the structure of the converter circuit, the values of the output voltage and the inductor current of the next switching cycle are predicted in advance. Duty cycle is calculated only through predicted output voltage and steady-state inductor current values, and the optimized duty cycle is predicted during the dynamic process. Meanwhile, in [14] a predictive control algorithm is proposed including the detection of the conduction mode for the power-factor-correction converter. In converters with PFC, the line current is often distorted due to the characteristics of the proportional-integral (PI) current controller. To improve the quality of the current, the optimum duty cycle is determined by estimating the next current state in the continuous conduction mode (CCM) and the discontinuous conduction mode.

Considering digital control applications, authors of [15] describe a digitally controlled power-factor-correction system based on two interleaved drive converters operating with pulse width modulation (PWM). Both converters are controlled independently by an internal regulator loop based on a discrete-time sliding mode (SM) approach that imposes a loss-free resistor (LFR) behavior. The switching surface implements an average current mode driver so that the power factor (PF) is high. Additional work can be seen in [16], where a mixed-signal control scheme is presented for a boost power-factor-correction rectifier. The digital controller modulates the maximum inductor current to produce low distortion at the AC line current in discontinued conduction mode and continuous conduction mode without detecting the average current.

Concerning other applications for the design of a digital control system for power electronic converters, the reference [17] presents an integrated interleaved dual-mode time-sharing inverter (IIDMI) for the grid-tied transformer-less photovoltaic systems. The IIDMI has low total harmonic distortion of the AC with reduced filtering requirements and reduced current of power devices. The current control, especially transitions between the buck and the boost modes of operation, is made using a fast response dead-beat control (DBC). Likewise, document [18] presents a single-phase transformer-less dual-mode interleaved multilevel inverter (DMIMI) that injects a highly sinusoidal AC to the grid. Dead-beat controllers are developed to calculate the optimal duty cycles directly. The DMIMI offers high efficiency, and fewer components conducting simultaneously in each operation mode. In addition, the work in [19] proposes the application of the dual-mode time-sharing technique in transformer-less photovoltaic inverters. The indirect current control, especially at transition

modes of operation, is improved using a fast dead-beat control scheme. The system obtains a low leakage current, which is a primary concern with the transformer-less PV inverters. On the other hand, the authors of [20] propose an extendable quadratic bidirectional DC-DC converter with an improved voltage transfer ratio (VTR), capable of redundancy and modularity for electric vehicle applications. The converter has a simple structure with the lowest rating of semiconductors in the family of quadratic bidirectional converters.

Regarding LED (Light-Emitting Diode) applications, the work in [21] presents the design and experimental evaluation of a one-stage AC/DC converter with PFC and a hybrid full-bridge rectifier to supply streetlights. The proposed converter consists of an LLC resonant tank, two boost circuits, and a shared inductor. By incorporating a relay switch on the secondary side of the circuit, the output stage can operate as two different types of rectifier: the first is as a full-bridge rectifier and the second type is as a full-bridge voltage doubling rectifier. In addition, paper [22] presents a single-stage controller with smooth switching and PFC functions for LED street lighting applications. The system integrates a PFC buck-boost converter interleaved with coupled inductors and a half-bridge LLC resonant converter in a single-stage power conversion circuit with reduced voltage across the DC connected capacitor and power switches. The inductors coupled in the interleaved PFC buck-boost converter operate in discontinuous conduction mode to achieve PFC. Additional work can be seen in [23] that presents the implementation of a two-stage light-emitting diode driver. The LED driver circuit design drives a 150 W LED module. The controller stages are: AC/DC power-factor-correction stage, and DC/DC power converter stage. The PFC stage implementation uses the NCP1608 integrated circuit, which uses the critical conduction mode to ensure unity power factor with a wide range of input voltages.

Regarding other applications made for power-factor-correction converters, reference [24] presents a built-in photovoltaic (PV) power interface circuit with a buck-boost converter and a full-bridge inverter. The circuit consists of five switches, an input inductor, and LC filters. The buck-boost converter operates at a high switching frequency to make the output current a sine wave, while the full-bridge inverter operates at a low switching frequency of 50–60 Hz. A high power factor is achieved in the output stage without an additional current driver due to the input inductor current operating in a discontinuous conduction mode.

The central aspect to consider in this paper is that for implementing a boost converter, the half-bridge topology provides a simpler conversion circuit by using fewer switching devices; however, the voltage imbalance between the capacitors is a critical study factor. Previous research [25] aims at finding alternatives to eliminate the cause of imbalance and outlines for designing a power circuit using a fixed band hysteresis current control (HCC) technique. In [26], it is proposed to add a DC bias to each phase's current source to solve the voltage imbalance problem. Elimination strategies are developed by carefully analyzing all possible paths of DC bias currents and their effect on voltage imbalance. Later in [27], these same authors study the adverse effects of the imbalance elimination control circuit on the input power factor. Finally, a related work to consider is presented in [28], which analyzes a four-switch voltage doubler boost rectifier. The authors propose a control scheme to eliminate output voltage imbalance when the load is imbalanced between the two output DC rails. To limit the output voltage imbalance, the controller employs a comparator with hysteresis. Unipolar pulse width modulation switching patterns are used to reduce the discharge rate of the output capacitor for low voltages. Figure 1 shows the traditional control methodology to correct the imbalance; however, injecting a direct component to $i_{L_{REF}}$ or generating a phase difference between i_g and v_g decreases the PF [6]. Therefore, the possibility is open for the development of alternatives to correct the imbalance.

Figure 1. Control diagram with differential voltage loop for a converter with power factor correction in half-bridge configuration.

Table 1 and Figure 2 describe the related works showing the relevance of low power factor converters, emphasizing the half-bridge boost converter. The main issue here is the voltage imbalance; moreover, some applications and control strategies are also displayed.

Table 1. Description of the related works.

Topic	Description	References
Power Factor	General aspects about power quality, power factor and harmonic distortion in electrical systems	[1–7]
Converters PFC	Provision of a general description of PFC converters, cascade buck-boost, Ćuk converter, flyback circuit, and boost converter	[6,8–10,10–12]
Fuzzy logic control	PFC converter control using fuzzy logic in the application to supply power to a fed brushless DC motor	[13]
Predictive control	Predictive control application for PFC converters, the system calculates the future value of the duty cycle	[11,14]
Digital Controller	It shows a brief review of different applications of converters using digital controllers	[15–20]
LED applications	Application of PFC converters for LED lighting using full-bridge and half-bridge rectifiers	[21–23]
Photovoltaic applications	Description of the application of PFC converters in photovoltaic systems	[17,24]
Voltage Imbalance	Describe main works related to the imbalance in half-bridge rectifiers. This issue is addressed in this work	[25–28]

Figure 2. Graphic description of the related works.

This article focuses on showing that the proposed topology allows the reduction of the capacitor imbalance in a half-bridge boost converter. For this, mathematical analysis and experimental tests are carried out. In classical topologies, when correcting the imbalance, the power factor is sacrificed as shown in [25]. Thus, it is presented a switched DC/DC converter circuit (equalizer) operating in discontinuous conduction mode that solves the voltage imbalance problem in the half-bridge boost converter. The proposed equalizer circuit is added to the voltage doubler boost rectifier. It is composed of two transistors, in this case, MOSFETs S_1 , S_2 and the respective diodes D_1 , D_2 , as well as an inductance L . As a result, a voltage doubler boost rectifier with equalizer is originated, which is shown in Figure 3. In addition, h is the duty cycle associated with the switches S_a and S_b of the doubler-rectifier-elevator, and $1 - h$ correspond to the complement.

The document is organized as follows: Section 2 qualitatively describes the equalizer circuit operation, its average circuit model is given in Section 3. Section 4 presents a detailed analysis of the equalizer's voltage elimination imbalance using its average circuit model. Aiming to eliminate the voltage imbalance, Section 5 proposes a hysteretic band control scheme to govern (control) the equalizer. A comparison with other classic converters via simulation appears in Section 6, later in Section 7 a prototype of the voltage doubler boost rectifier with the proposed equalizer circuit is built to test it and validate the theoretical analysis; finally, the conclusions are given.

Figure 3. Voltage doubler boost rectifier with equalizer.

2. Description of the Proposed Equalizer Circuit

As previously mentioned, the imbalance of voltages in the capacitors in a half-bridge boost converter is a critical factor, which is why this document analyzes, designs and implements a strategy called equalizer circuit to eliminate the voltage imbalance on the capacitors.

To explain the operation of the proposed equalizer circuit operating in DCM, it is considered that the output capacitors C_1 and C_2 are sufficiently large, so that the voltage ripples produced by switching frequency and line frequency can be neglected; on the other hand, all components of the equalizer circuit are ideal. According to the comparison between the voltages of the capacitors, two

modes arise in the operation of the equalizer circuit that affect the state of charge and discharge of both capacitors, as described below:

2.1. Analysis for the Case $V_1 > V_2$

In this mode, the transistor S_1 and the diode D_2 operate, as shown in Figure 4; likewise, the waveforms of the current i' and the voltage v' of the inductance for this mode are shown in Figure 5. The inductance current is equal to zero at the beginning of each switching period T_s , during the first interval $d_1 T_s$, simultaneously the transistor S_1 is turned on and the diode D_2 turns off; the voltage of the inductance is equal to V_1 ; hence, the current of the inductance increases with a slope equal to $\frac{V_1}{L}$, at the end of this first interval, the inductance current reaches its maximum value given by:

$$I_m = \frac{V_1}{L} d_1 T_s, \quad (1)$$

Figure 4. Equalizer circuit for the case $V_1 > V_2$.

Figure 5. Waveforms of v' and i' associated with the equalizer circuit for the case $V_1 > V_2$.

Therefore, the maximum current value I_m is directly proportional to the voltage of the capacitor C_1 , as well as to the duration of the first interval, therefore, the inductance absorbs energy from the capacitor C_1 , which is proportional to the square of I_m and is given by:

$$W = \frac{1}{2} L I_m^2 \quad (2)$$

During the second interval $d_2 T_s$ the transistor S_1 turns off. Meanwhile, the diode D_2 turns on, the inductance voltage is equal to $-V_2$, then, the inductance current decreases with a slope equal

to $-\frac{V_2}{L}$, at the end of this second interval the diode D_2 is polarized in inverse and the energy that the inductance absorbed during the first interval is transferred to the capacitor C_2 . The inductance current and voltage are kept at zero during the third interval $d_3 T_s$. Consequently, the equalizer circuit discharges the capacitor C_1 during the first interval and charges the capacitor C_2 during the second interval in this mode.

2.2. Analysis for the Case $V_2 > V_1$

In Figure 6, waveforms of the current i' and the voltage v' of the inductance are equal to the previous mode. Nevertheless, the direction of the current and the voltage polarity are reversed, as illustrated in Figure 7, where is seen that the transistor S_2 and the diode D_1 now operate. Similar to the previous mode, the inductance current is equal to zero at the beginning of each switching period T_s , during the first interval $d_1 T_s$, the transistor S_2 is turned on, simultaneously, diode D_1 turns off, the inductance voltage equals V_2 ; therefore, the inductance current increases with a slope equal to $\frac{V_2}{L}$, at the end of this first interval, the inductance current reaches its maximum value given by:

$$I_m = \frac{V_2}{L} d_1 T_s, \quad (3)$$

Figure 6. Waveforms of v' and i' associated with the equalizer circuit for the case $V_2 > V_1$.

Figure 7. Equalizer circuit for the case $V_2 > V_1$.

Therefore, the maximum value of current I_m is directly proportional to the voltage of the capacitor C_2 and the duration of the first interval; then, the inductance absorbs energy from the capacitor C_2 , which is proportional to the square of I_m and is given by (2). During the second interval $d_2 T_s$, the transistor S_2 turns off. Meanwhile, diode D_1 turns on, and inductance voltage is equal to $-V_1$,

which is why the inductance current decreases with a slope equal to $-\frac{V_1}{L}$; at the end of this second interval, diode D_1 is reverse biased, and the energy absorbed by the inductance during the first interval is transferred to the capacitor C_1 . The inductance current and voltage are kept at zero during the third interval $d_3 T_s$. As a result, the equalizer circuit discharges the capacitor C_2 during the first interval and charges the capacitor C_1 during the second interval in this mode.

From the above, when $V_1 > V_2$, the equalizer absorbs energy from C_1 , which is delivered to C_2 , then, V_1 decreases, at the same time V_2 increases; likewise, when $V_2 > V_1$, the equalizer absorbs energy from C_2 that is delivered to C_1 ; hence V_2 decreases while V_1 increases; to conclude, the equalizer circuit eliminates the voltage imbalance that occurs in the capacitors. In Section 4, a more detailed analysis is made using the average circuit model of the equalizer circuit.

3. Average Circuit Model

The average circuit model of the equalizer in each operating mode is obtained by following the average switch-modeling technique [29], which generates an equivalent circuit that models the average of the waveforms at the terminals of the switch network. In relation to the equalizer when $V_1 > V_2$, Figure 4 shows the equivalent circuit of the transistor S_1 and diode D_2 , which is obtained by averaging the respective waveforms of the inductance current, capacitor voltage, and duty cycle.

The average voltage associated with S_1 is v_3 , this is found by averaging the waveform v'_3 shown in Figure 8.

$$v_3 = d_2 (V_1 + V_2) + d_3 V_1, \quad (4)$$

from any of the waveforms, it follows that d_3 can be expressed as:

$$d_3 = 1 - d_1 - d_2, \quad (5)$$

replacing (5) in (4) is obtained:

$$v_3 = d_2 V_2 + (1 - d_1) V_1, \quad (6)$$

likewise, i_3 is the average current of S_1 and it is found by averaging the waveform i'_3 shown in Figure 8.

$$i_3 = \frac{1}{2} d_1 I_m, \quad (7)$$

substituting (1) in (7), yield:

$$i_3 = \frac{1}{2} \frac{d_1^2 V_1 T_s}{L} \quad (8)$$

Figure 8. Voltage and current waveforms associated with S_1 for the equalizer circuit when $V_1 > V_2$.

The average voltage of D_2 is v_4 , this voltage is found by averaging the waveform v'_4 shown in Figure 9.

$$v_4 = d_1 (V_1 + V_2) + d_3 V_2, \quad (9)$$

substituting (5) in (9) produces:

$$v_4 = d_1 V_1 + (1 - d_2) V_2 \quad (10)$$

Figure 9. Voltage and current waveforms associated with D_2 for the equalizer circuit when $V_1 > V_2$.

Similarly, i_4 is the average current of D_2 and it is found by averaging the waveform i'_4 shown in Figure 9.

$$i_4 = \frac{1}{2} d_2 I_m, \quad (11)$$

substituting Equation (1) in (11), yield:

$$i_4 = \frac{1}{2} \frac{d_1 d_2 V_1 T_s}{L} \quad (12)$$

On the other hand, Figure 5 shows no change in current i' over a commutation period, having as a result:

$$\frac{L}{T_s} [i'(t + T_s) - i'(t)] = \frac{1}{T_s} \int_t^{t+T_s} v' d\tau = 0 \quad (13)$$

and since:

$$v = \frac{1}{T_s} \int_t^{t+T_s} v' d\tau, \quad (14)$$

the average voltage of the inductance v is equal to zero and the average of the waveform v' shown in Figure 5, is given by:

$$v = d_1 V_1 - d_2 V_2 = 0, \quad (15)$$

solving d_2 then:

$$d_2 = d_1 \frac{V_1}{V_2}, \quad (16)$$

therefore, the average of each of the waveforms is obtained, at the terminals of S_1 and D_2 , substituting (16) in (6), (8), (10), and (12), is obtained:

$$v_3 = V_1 \quad (17)$$

$$v_4 = V_2 \quad (18)$$

$$i_3 = \frac{1}{2} \frac{d^2 v_3 T_s}{L} \quad (19)$$

$$i_4 = \frac{1}{2} \frac{d^2 v_3^2 T_s}{L v_4} \quad (20)$$

where d is the duty cycle equal to d_1 ; in conclusion, Equations (17)–(20) are simple expressions that represent the average of the waveforms of the transistor S_1 and diode D_2 of the equalizer circuit in DCM, when $V_1 > V_2$.

To find a circuit that models the S_1 and D_2 waveforms, it is considered that S_1 absorbs and D_2 delivers apparent average power. According to Figure 4, S_2 absorbs apparent power, since its current enters through the positive value of its voltage, at the same time, D_2 delivers apparent power, since its current leaves through the positive value of its voltage; in addition, the apparent average power of S_1 and D_2 are equal and expressed as:

$$v_3 i_3 = v_4 i_4 = \frac{1}{2} \frac{d^2 V_1^2 T_s}{L} \quad (21)$$

Also, the apparent average power of S_1 and D_2 is deduced considering the energy stored by the inductance and expressing its maximum current reached I_m , during the first interval of time dT_s in terms of the voltage V_1 ; therefore, replacing (1) in (2) is obtained:

$$W = \frac{1}{2} \frac{(dT_s V_1)^2}{L}, \quad (22)$$

dividing both sides of (22) by the commutation period T_s , it is obtained the power absorbed by the inductance during the first time interval, equal to the expression given in (21). As a result, it can be stated that during the first time interval, the power is transferred from the capacitor C_1 to the inductance L through the terminals of the transistor S_1 . During the second time interval the inductance L releases all the energy stored to the capacitor C_2 , through the terminals of diode D_2 ; then, the average power consumed by the transistor and the diode equals zero, i.e., the transistor S_1 behaves like a power source that absorbs P_1 . Simultaneously, the diode D_2 behaves like a power source that supplies P_2 . The power P_2 is dependent on the power P_1 , since the voltage and current of the S_1 terminals are independent of the voltage and current from the D_2 terminals.

Therefore, the equalizer average model when $V_1 > V_2$ is represented by two power sources that substitute transistor S_1 and diode D_2 , as shown in Figure 10. Source P_1 absorbs power that is later transferred to source P_2 , whereby source P_1 absorbs power from capacitor C_1 that flows to the source P_2 and then to capacitor C_2 . Also, in Figure 10 is seen the replacement of the inductance by a short circuit considering average voltage equal to zero; likewise, the current i that flows through this short circuit is the average current of inductance i' .

Figure 10. Average circuit model of the equalizer when $V_1 > V_2$.

The equalizer circuit when $V_2 > V_1$ is illustrated in Figure 7, this represents the equivalent circuit composed by the transistor S_2 and diode D_1 . By averaging the waveforms in terms of the equalizer input and state variables is obtained:

$$i_3 = \frac{1}{2} \frac{d^2 v_4^2 T_s}{L v_3} \quad (23)$$

$$i_4 = \frac{1}{2} \frac{d^2 v_4 T_s}{L} \quad (24)$$

The average circuit model of the equalizer when $V_2 > V_1$ consists of two power sources that replace the transistor S_2 and diode D_1 as shown in Figure 11. The source P_2 absorbs power that is transferred to the source P_1 ; hence, the source P_2 absorbs power from the capacitor C_2 that flows to P_1 , and then to C_1 . The inductance is replaced by a short circuit in the same way than in the average equalizer circuit when $V_1 > V_2$.

Figure 11. Average circuit model of the equalizer when $V_2 > V_1$.

4. Voltage Imbalance Analysis

To start the analysis in the voltage doubler boost rectifier, it is considered that the voltage variations in both capacitors are produced by the line frequency. The line voltage varies in a sinusoidal way and to obtain a unitary PF; also, the line current is sinusoidal, having:

$$v_g = V_p \sin(\theta) \quad (25)$$

$$i_g = I_p \sin(\theta) \quad (26)$$

On the other hand, the average circuit models of the proposed equalizer obtained in Section 3 are used to calculate the steady-state voltage imbalance in the voltage doubler boost rectifier capacitors, in each mode of operation of the equalizer proposed.

4.1. Analysis for the Case $V_1 > V_2$

In this mode, the average equalizer circuit is connected to the voltage doubling step-up rectifier capacitors, as shown in Figure 10, from which the average currents i_1 and i_2 are expressed as:

$$i_1 = -hi_g - I_s - i_3 \quad (27)$$

$$i_2 = (1-h)i_g - I_s + i_4 \quad (28)$$

By substituting (17) and (18) in (19) and (20), the average currents i_3 and i_4 are obtained in terms of the average voltages of the capacitors V_1 and V_2 having:

$$i_3 = \frac{d^2 V_1 T_s}{2L} \quad (29)$$

$$i_4 = \frac{d^2 V_1^2 T_s}{2LV_2} \quad (30)$$

The average voltage of the inductance L_g , in the voltage doubler boost rectifier [5,30] is given by:

$$L_g \frac{di_g}{dt} = v_g + V_1 - (1 - h) V_s, \quad (31)$$

where $V_s = V_1 + V_2$, and replacing (25) and (26) in (31) yield:

$$\omega L_g I_p \cos(\theta) = V_p \sin(\theta) + V_1 - (1 - h) V_s, \quad (32)$$

solving h from (32) is obtained:

$$h = \frac{\omega L_g I_p}{V_s} \cos(\theta) - \frac{V_p}{V_s} \sin(\theta) - \frac{V_1}{V_s} + 1, \quad (33)$$

comparing magnitude for sine and cosine signals $\frac{V_p}{V_s} \gg \frac{\omega L_g I_p}{V_s}$, it is established that $V_p \gg \omega L_g I_p$, then Equation (33) can be approximated to:

$$h = -\frac{V_p}{V_s} \sin(\theta) - \frac{V_1}{V_s} + 1, \quad (34)$$

replacing (26), (29), (30), and (34) in (27), and (28), is obtained:

$$i_1 = \frac{V_p I_p}{V_s} \sin^2(\theta) - \frac{V_2 I_p}{V_s} \sin(\theta) - I_s - \frac{d^2 T_s V_1}{2L} \quad (35)$$

$$i_2 = \frac{V_p I_p}{V_s} \sin^2(\theta) + \frac{V_1 I_p}{V_s} \sin(\theta) - I_s + \frac{d^2 T_s V_1^2}{2LV_2} \quad (36)$$

Considering that the duty cycle d is constant, then, the variations of the voltages in the capacitors V_1 and V_2 over a switching period are given by:

$$\delta V_1 = \frac{1}{\omega C_1} \int_0^{2\pi} i_1 d\theta = \frac{\pi}{\omega C_1} \left(\frac{V_p I_p}{V_s} - 2I_s - \frac{d^2 T_s V_1}{L} \right) \quad (37)$$

$$\delta V_2 = \frac{1}{\omega C_2} \int_0^{2\pi} i_2 d\theta = \frac{\pi}{\omega C_2} \left(\frac{V_p I_p}{V_s} - 2I_s + \frac{d^2 T_s V_1^2}{LV_2} \right) \quad (38)$$

It is assumed that C_1 and C_2 are equal to C ; hence, the variation of the voltage difference over a switching period, with the proposed equalizer when $V_1 > V_2$ is given by:

$$\delta V_2 - \delta V_1 = \frac{\pi d^2 T_s}{\omega LC} \left(\frac{V_1^2}{V_2} + V_1 \right) \quad (39)$$

4.2. Analysis for the Case $V_2 > V_1$

According to Figure 11, the average currents i_1 and i_2 of the average equalizer circuit are given by:

$$i_1 = -hi_g - I_s + i_3 \quad (40)$$

$$i_2 = (1 - h) i_g - I_s - i_4 \quad (41)$$

On the other hand, by replacing (17) and (18) in (23) and (24), respectively, the average currents i_3 and i_4 are obtained in terms of the average voltages of the capacitors V_1 and V_2 being:

$$i_3 = \frac{d^2 V_2^2 T_s}{2LV_1} \quad (42)$$

$$i_4 = \frac{d^2 V_2 T_s}{2L} \quad (43)$$

Substituting (26), (34), (42), and (43) in (40) and (41) yield:

$$i_1 = \frac{V_p I_p}{V_s} \sin^2(\theta) - \frac{V_2 I_p}{V_s} \sin(\theta) - I_s + \frac{d^2 T_s V_2^2}{2LV_1} \quad (44)$$

$$i_2 = \frac{V_p I_p}{V_s} \sin^2(\theta) + \frac{V_1 I_p}{V_s} \sin(\theta) - I_s - \frac{d^2 T_s V_2}{2L} \quad (45)$$

Since the duty cycle d is constant, the variations of the voltages in the capacitors V_1 and V_2 over a switching period are expressed as:

$$\delta V_1 = \frac{1}{\omega C_1} \int_0^{2\pi} i_1 d\theta = \frac{\pi}{\omega C_1} \left(\frac{V_p I_p}{V_s} - 2I_s + \frac{d^2 T_s V_2^2}{LV_1} \right) \quad (46)$$

$$\delta V_2 = \frac{1}{\omega C_2} \int_0^{2\pi} i_2 d\theta = \frac{\pi}{\omega C_2} \left(\frac{V_p I_p}{V_s} - 2I_s - \frac{d^2 T_s V_2}{L} \right) \quad (47)$$

Since C_1 and C_2 are equal to C , the variation of the voltage differs over a switching period, with the proposed equalizer when $V_2 > V_1$ is expressed as:

$$\delta V_1 - \delta V_2 = \frac{\pi d^2 T_s}{\omega LC} \left(\frac{V_2^2}{V_1} + V_2 \right) \quad (48)$$

From this analysis, it is stated that the variations in the difference voltage expressed in (39) and (48) are always positive; as a result, the voltage imbalance is eliminated in both modes of operation, using the proposed equalizer circuit. This elimination is achieved regardless of the load conditions in the voltage doubler boost rectifier.

5. Control Scheme

The proposed control scheme that governs the equalizer circuit in DCM, is shown in Figure 12, this scheme is a circuit that allows the passage of a carrier signal v_x to the transistor S_1 or S_2 .

When $V_1 > V_2$, the carrier pass to S_1 is enabled; simultaneously, S_2 is set to zero and then the equalizer circuit operates in mode $V_1 > V_2$, absorbing energy from C_1 which flows towards C_2 , so that V_1 decreases and V_2 increases. On the other hand, if $V_2 > V_1$, the carrier pass to S_2 is enabled, at the same time, S_1 is set to zero; therefore, the equalizer circuit operates in the mode $V_2 > V_1$, in which it absorbs energy from C_2 which then flows to C_1 ; as a result, V_2 decreases and V_1 increases. The carrier signal v_x establishes the duty cycle d and the switching period T_s of the equalizer, in addition, the duty cycle d is constant and its value is chosen to ensure the operation on DCM of the equalizer; therefore, the equalizer in mode $V_1 > V_2$ operates on DCM when:

$$d < \frac{V_2}{V_1 + V_2}, \quad (49)$$

on the other hand, the equalizer in the mode $V_2 > V_1$ operates in DCM if:

$$d < \frac{V_1}{V_1 + V_2}, \quad (50)$$

The conclusion from (49) and (50) is that the duty cycle d must be less than 0.5 to ensure the equalizer operation in DCM for both modes; also, the duty cycle d determines the energy absorbed by the inductance. On the other hand, the hysteresis band of the comparator must be selected carefully, a wide band produces a high voltage imbalance; likewise, as there is ripple in the voltages V_1 and V_2 , a narrow band can cause malfunctions in the proposed control scheme.

Figure 12. Control scheme of the equalizer circuit.

The hysteresis band was selected considering the variation that can be held in the voltage capacitors. In an experimental way using simulation, different values, displayed in Table 2, are obtained to determine this band, where BH is the hysteresis band and $V_d = V_1 - V_2$ is the difference voltage value between the capacitors. In Table 2, as BH increases, V_d also increases; therefore, it is appropriate to have a small value of BH ; however, the operation of the elements is not ideal implying practical limitations. Therefore, using the values of Table 2 in the real circuit, the smallest useful value of BH is 3 V, because for low values of BH undesired oscillations that do not appear in simulation are present in the real circuit.

Table 2. Hysteresis band values obtained in simulation.

BH (V)	V_d (V)
0.25	± 1.58
0.5	± 1.98
1	± 1.71
2	± 2.47
3	± 3
4	± 3.5

6. Simulation Results

This section presents the comparison of the proposed circuit versus other classic configurations via simulation. The first part of the results show that the proposed circuit does not affect drastically the power factor, the harmonic distortion and the power efficiency. Later it is observed the effect that the variation of the capacitors has on the PF for the simulated circuits. The converters considered are:

- CV1: Converter proposed with equalizer circuit. The simulation scheme is show in Figure 13.
- CV2: Classic PFC converter using half-bridge boost topology developed in [25]. The diagram of the simulation is show in Figure 14.
- CV3: Half-bridge PFC Boost converter with digital PID controller and pre-compensation loop developed in [6]. The scheme of the simulation is presented in Figure 15.

Figure 13. Simulation scheme for CV1.

Figure 14. Simulation diagram for CV2.

Figure 16. Waveforms obtained for CV1; i_g : 1 A/div, v_g , v_1 and v_2 : 100 V/div.

Figure 17. Waveforms obtained for CV2; i_g : 1 A/div, v_g , v_1 and v_2 : 100 V/div.

Figure 18. Waveforms obtained for CV3; i_g : 1 A/div, v_g , v_1 and v_2 : 100 V/div.

In the previous results, the condenser's value variations are disregarded; therefore, the following experimental test focuses on observing the effect when the condensers have value variations toward $\pm 5\%$ of the nominal value. Table 4 displays such results when considering the circuit operation at full load.

Table 4. Comparison results with capacitors variation.

Circuit	C_1 (μF)	C_2 (μF)	V_1 (V)	V_2 (V)	PF
CV1	95	105	225	225	0.9925
	105	95	225	225	0.9925
CV2	95	105	223.9	226.2	0.9845
	105	95	226.2	223.9	0.9845
CV3	95	105	227.9	227.9	0.9923
	105	95	227.9	227.9	0.9923

Table 4 shows that the CV1 configuration reduces the imbalance by presenting the best PF while CV2 displays the largest imbalance, also affecting PF. Moreover, circuit CV3 fulfills equality in the values V_1 and V_2 ; nevertheless, this is done employing a value greater than 225, which should be the operation value. It is noticeable that CV3 incorporates a feedback loop to correct the imbalance.

7. Experimental Results

A prototype of the voltage doubler boost rectifier with the proposed equalizer circuit was built in the laboratory (Figure 19), with the circuit parameters shown in Table 5. The selection is made considering the recommendations of [5], L is first calculated using the equation:

$$L = \frac{V_s}{4f_s \delta i_{L,p-p}} \quad (51)$$

where $\delta i_{L,p-p} = 0.4$ A maximum ripple current (value desired), $f_s = 50$ kHz switching frequency, $V_s = 450$ V output voltage; using these values the inductance value obtained is $L \approx 5$ mH. Afterwards, the capacitors $C_1 = C_2 = C$ are calculated using equation:

$$C = \frac{1}{\delta v_{s,p-p} V_s} \sqrt{\frac{(V_p + r_p I_p)^2 I_p^2}{\omega^2} + L^2 I_p^4} \quad (52)$$

where $\delta v_{s,p-p} = 10$ V is the peak-to-peak capacitors voltage variation (value desired), $V_p = 120\sqrt{2}$ V the source peak voltage, $I_p = 0.9927$ A peak current, $\omega = 2\pi 60$ rad/s line frequency, $r_p \approx 0$ loss resistance associated with components. Using these values, the capacitors C_1 and C_2 are 100 μF .

Figure 19. Prototype of the voltage doubler boost rectifier.

Likewise, the semiconductors employed are diodes MUR460, transistors STP13NK60ZFP (ST Microelectronics), and the integrated circuit HCPL-3120 as the trigger driver. The controller was implemented with the digital signal processor (DSP) Texas Instruments TMDX28069USB (Piccolo F28069). In addition, the measurement equipment used are:

- Oscilloscope: Agilent MSO-X 3014A.
- Current probe: Keysight 1146B 100 kHz/100 A.
- Current probe: N2783B 100 MHz/30 Arms AC/DC.

Table 5. Parameters of the voltage doubling step-up rectifier with the proposed equalizer circuit.

Circuit Parameter	Symbol	Value
Peak line voltage	V_p	170 V
Output voltage	V_s	450 V
Equalizer inductance	L	500 μ H
Rectifier inductance	L_g	5 mH
Output capacitors	$C = C_1 = C_2$	100 μ F
Load resistance	R	2 k Ω
Line frequency	f_L	60 Hz
Switching frequency rectifier and equalizer	f_s	50 kHz
Duty cycle of S_1 and S_2	d	0.125
Hysteresis band of the comparator	-	± 3 V

The experimental results show how the proposed equalizer circuit eliminates the voltage imbalance. Figures 20–23 illustrate the waveforms of v_1 , v_2 , S_1 and S_2 for values I_s of 222 mA, 198 mA, 153 mA and 110 mA, respectively. The signals of S_1 and S_2 are measured at the output of the DSP. The operation of the proposed equalizer circuit can be verified by the absence of voltage imbalance in the output capacitors for the load current values. Moreover, by the way S_1 and S_2 work, it can be seen that when $V_1 > V_2$, S_1 and D_2 commute so that L absorbs energy from C_1 which is delivered to C_2 ; then, V_1 decreases at the same time V_2 increases.

Figure 20. Waveforms of v_1 , v_2 , S_1 and S_2 for $I_s = 222$ mA.

Figure 21. Waveforms of v_1 , v_2 , S_1 and S_2 for $I_s = 198$ mA.

Figure 22. Waveforms of v_1 , v_2 , S_1 and S_2 for $I_s = 153$ mA.

Additionally, when $V_2 > V_1$, S_2 and D_1 commute so that L absorbs energy from C_2 which is delivered to C_1 ; hence, V_2 decreases and simultaneously V_1 increases; consequently, that mentioned in Sections 2 and 4 is confirmed regarding the circuit operation and elimination of voltage imbalance.

Figure 23. Waveforms of v_1 , v_2 , S_1 and S_2 for $I_s = 110$ mA.

On the other hand, Figures 24 and 25 shows how the input current i_g follows input voltage v_g , for values I_s of 222 mA and 198 mA, respectively, so that the proposed equalizing circuit does not affect the operation of the voltage doubling step-up rectifier; in addition, high power factor values were obtained under steady-state conditions, these values were 0.995 and 0.992 for values I_s of 222 mA and 198 mA.

Figure 24. Waveforms of v_g and i_g for $I_s = 222$ mA.

Figure 25. Waveforms of v_g and i_g for $I_s = 198$ mA.

As discussed, it is observed that the proposed circuit allows reducing the imbalance in the voltage of the condensers without affecting the power factor. However, it is mandatory to employ additional components with a control system, enhancing the construction and cost complexities.

8. Conclusions

An equalizing converter circuit operating on DCM was proposed to solve the voltage imbalance problem. The equalizer circuit operation was described qualitatively; moreover, an average circuit model was obtained consisting of two power sources. The model was used to analyze in detail how the equalizer eliminates the voltage imbalance in the capacitors; for this, the expressions that define the average currents that flow through both capacitors were calculated, obtaining the voltage variations, as well as the variation of the voltage difference over a switching period, in each operating mode of the equalizer. In addition, a simple hysteretic band control scheme was proposed that manages the “on” and “off” of the equalizer switches.

The analysis results were verified by experiments carried out on a prototype built in the laboratory. The results show how the equalizer circuit eliminates the voltage imbalance in steady state for different load conditions; thus, a high power factor is demonstrated at full load. Therefore, the equalizer circuit does not affect the operation of the voltage doubler boost rectifier.

The comparison made concerning to other classical topologies allows appreciation that the proposed circuit does not present a decrease in the power factor when there is variation in the capacitor's value; however, it is necessary to use additional components, which increases its complexity.

In further work, it is expected another controller be developed to eliminate voltage imbalance across the converter capacitors using the model of the two power sources proposed in this paper.

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