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Analysis of State-of-the-Art Spin-Transfer-Torque Nonvolatile Flip-Flops Considering Restore Yield in the Near/Sub-Threshold Voltage Region

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Abstract: Recently, the leakage power consumption of Internet of Things (IoT) devices has become a main issue to be tackled, due to the fact that the scaling of process technology increases the leakage current in the IoT devices having limited battery capacity, resulting in the reduction of battery lifetime. The most effective method to extend the battery lifetime is to shut-off the device during standby mode. For this reason, spin-transfer-torque magnetic-tunnel-junction (STT-MTJ) based nonvolatile flip-flop (NVFF) is being considered as a strong candidate to store the computing data. Since there is a risk that the MTJ resistance may change during the read operation (i.e., the read disturbance problem), NVFF should consider the read disturbance problem to satisfy reliable data restoration. To date, several NVFFs have been proposed. Even though they satisfy the target restore yield of 4σ, most of them do not take the read disturbance into account. Furthermore, several recently proposed NVFFs which focus on the offset-cancellation technique to improve the restore yield have obvious limitation with decreasing the supply voltage (V_{DD}), because the offset-cancellation technique uses switch operation in the critical path that can exacerbate the restore yield in the near/sub-threshold region. In this regard, this paper analyzes state-of-the-art STT-MTJ based NVFFs with respect to the voltage region and provides insight that a simple circuit having no offset-cancellation technique could achieve a better restore yield in the near/sub-threshold voltage region. Monte–Carlo HSPICE simulation results, using industry-compatible 28 nm model parameters, show that in case of V_{DD} of 0.6 V, complex NVFF circuits having offset tolerance characteristic have a better restore yield, whereas in case of V_{DD} of 0.4 V with sizing up strategy, a simple NVFF circuit having no offset tolerance characteristic has a better restore yield.

Keywords: magnetic tunnel junction (MTJ); near/sub-threshold voltage region; nonvolatile flip-flop (NVFF); read disturbance; restore yield

1. Introduction

Recently, while technology node shrinks down, the leakage power consumption has been increased, as shown in Figure 1 [1]. The leakage power consumption of digital device such as Internet of Things (IoT) has become the main issue due to the limited battery lifetime [2]. In order to overcome this issue, the low leakage power design technique has been receiving a lot of attention. To improve the battery lifetime of IoT devices and minimize the leakage power consumption, various circuit techniques have been proposed such as power gating, stacked transistors, and the multiple threshold complementary metal oxide semiconductor (CMOS) techniques [3,4]. Among these techniques, the most straightforward method is to operate at low voltages (i.e., near/sub-threshold voltage region) during active mode and turn off the device during standby mode, since the IoT devices are usually operated in the standby mode. If supply voltage (V_{DD}) is zero during standby mode, no current flows through the circuit,

resulting in zero standby power consumption. However, all computing data for the operation will disappear due to the flip-flop's volatile nature. To realize the zero V_{DD} scheme during standby mode, the IoT devices must contain the nonvolatile flip-flop (NVFF) using the nonvolatile elements.

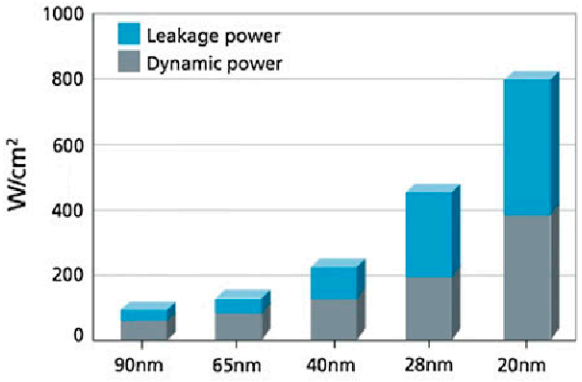

Figure 1. Leakage power vs. dynamic power [1].

Among various nonvolatile elements, the spin-transfer-torque magnetic tunnel junction (STT-MTJ) is regarded as a strong candidate because of its various advantages, such as high endurance, scalability, and easy integration with CMOS technology [5,6]. The STT-MTJ can save the computing data by using the two different resistance values such as low resistance (R_L) and high resistance (R_H). To save the computing data into the STT-MTJ, the current flowing through the STT-MTJ should be larger than the critical switching current (I_C) and longer than I_C pulse width. Furthermore, when the saved data is sensed (restored), the current flowing through the STT-MTJ should be smaller than the I_C and shorter than I_C pulse width. If the sensing current is larger than the I_C and/or longer than I_C pulse width during sensing (restoring) operation, there is a risk that the MTJ resistance value may change, known as the read disturbance problem [7–9]. Thus, a proper sensing current strength and pulse width needs to be considered for the STT-MTJ-based NVFF designs.

Generally, NVFF has four operation modes, such as normal, standby, write, and sensing modes. In case of the normal mode, the NVFF behaves as a conventional volatile FF (e.g., transmission-gate-based master-slave FF). In case of the write mode, the computing data of the FF is saved into the MTJs prior to blocking the supply power. In case of the standby mode, supply power is fully turned off to actualize the zero standby leakage power, and the MTJ has the stored data of FF core. In case of the sensing mode, it is possible to restore the stored data of STT-MTJ into the FF core.

To date, several separated latch and sensing circuit (SLS) structure based NVFFs have been proposed [10–13] to independently optimize the circuit and flip-flop core. Even though they satisfy the target restore yield of 4σ (it was set to 4σ to guarantee a 96.88% (=$\Phi(4\sigma)^{1000}$) yield when 1000 NVFFs are assumed, where Φ() is the cumulative distribution function of the standard normal distribution [11–13]) in super-threshold voltage region, it is hard for them to satisfy target restore yield of 4σ in the near/sub-threshold voltage region no matter how much the size and time increase. Furthermore, although the NVFF operating in the near-threshold voltage region [11] was proposed, it is difficult to satisfy the target restore yield of 4σ if the target read disturbance margin of 6σ (it was set to guarantee 99% yield when 10,000 access per a single cell is assumed by considering the stochastic nature of MTJ [13]) is considered. Thus, most of the state-of-the-art STT-MTJ-based NVFFs cannot satisfy the target restore yield and target read disturbance margin simultaneously at all corners in the near/sub-threshold voltage region.

In this paper, among the various recently proposed state-of-the-art NVFFs employing different emerging nonvolatile elements, such as field-induced magnetization reversal MTJ [14,15], STT-MTJ [10–13,16–23], complementary polarizer MTJ [24], spin-orbital-torque MTJ [25,26], memristor [27–30], ferroelectric capacitor (FeCAP) [31–34], and ferroelectric field-effect transistor (FeFET) [35,36], four state-of-the-art STT-MTJ-based NVFFs with the SLS structure were simulated and

described why the NVFFs do not satisfy the target restore yield according to V_{DD}. The analysis of the silicon-proven NVFFs with the merged latch and sensing circuit (MLS) structure can be found in the reference texts (see [13]). The rest of this paper is as follows. Section 2 describes the operation and analysis of the four state-of-the-art STT-MTJ-based NVFFs. Section 3 describes simulation results and comparison. Section 4 presents the conclusions.

2. State-of-the-Art STT-MTJ-Based NVFFs

In this section, the operation of four state-of-the-art STT-MTJ-based NVFFs [10–13] is described. Figure 2 shows the sensing circuit diagrams of the state-of-the-art NVFFs proposed by Na et al. [10], Song et al. [11], Na et al. [12], and Choi et al. [13].

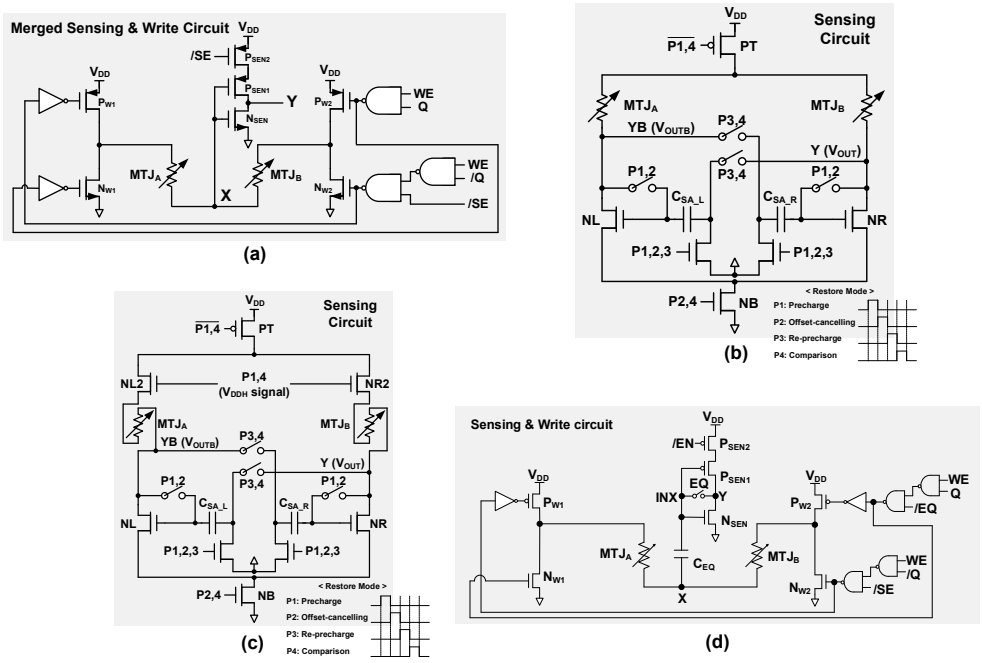

Figure 2. Sensing circuit diagrams of state-of-the-art NVFFs. (**a**) Na et al. [10]. (**b**) Song et al. [11]. (**c**) Na et al. [12]. (**d**) Choi et al. [13].

In the sensing mode of Na's NVFF [10] (Figure 2a), SE signal becomes 1. Then, P_{W1} and N_{W2} are turned on and the sensing inverter (P_{SEN2}, P_{SEN1} and N_{SEN}) starts to operate. Current flows from P_{W1} to N_{W2}. When the resistance of MTJ_A (R_{MTJA}) is low resistance (R_L) and the resistance of MTJ_B (R_{MTJB}) is high resistance (R_H), the X node voltage (V_X) becomes high voltage ($V_H = V_{DD} \times R_H/(R_L + R_H)$). In the similar manner, when R_{MTJA} is R_H and R_{MTJB} is R_L, V_X becomes low voltage ($V_L = V_{DD} \times R_L/(R_L + R_H)$). If trip voltage of the sensing inverter is ideal ($V_{TRIP} = V_{DD}/2 = (V_L + V_H)/2$), the output voltage ($V_Y$) of the sensing inverter is amplified to V_{DD} or GND by the inverter gain (A_{INV}) ($V_Y = V_X \times A_{INV}$). Then, the V_Y is delivered to FF core. Thus, the stored data in MTJ is restored.

In the sensing mode of Song's NVFF [11] (Figure 2b), the SE (SE = P1 + P2 + P3 + P4, meaning logical ORing of P1, P2, P3, and P4) signal becomes 1. The threshold voltage (V_{TH}) of NL and NR is stored in capacitors C_{SA_L} and C_{SA_R}, respectively. Then, the output node voltages (V_{OUT} and V_{OUTB}) are precharged to GND. If R_{MTJA} is R_L and R_{MTJB} is R_H, the V_{OUTB} becomes higher voltage and V_{OUT} becomes lower voltage because the current flowing through MTJ_A is higher than the current flowing through MTJ_B. Since the gate voltage of NR is higher than NL, the NR quickly discharges V_{OUT} because of the cross-coupled NMOS structure. As a result, V_{OUTB} becomes V_{DD} and V_{OUT} becomes almost GND, respectively. Then, the V_{OUT} is delivered to FF core. Thus, the stored data in MTJ is restored.

The sensing mode operation of Na's NVFF [12] (Figure 2c) is the same as the operation of Song's NVFF except for the inclusion of NL2 and NR2 and reverse-connected MTJ structure. The purpose

of the NL2 and NR2 is to isolate between the V_{OUT} and V_{OUTB} during the offset-cancelling phase, leading to the improvement in the offset tolerance characteristic. The reverse-connected MTJ structure improves the read disturbance margin by reducing the read current (I_{read}) causing the read disturbance.

The sensing mode operation of Choi's NVFF [13] (Figure 2d) is similar to the operation of Na's NVFF [10] but auto-zeroing and dynamic reference voltage (DRV) techniques are added to improve the read yield. The auto-zeroing technique cancels the offset voltage (V_{TRIP} variation) caused by the process variation in the sensing inverter. The DRV technique improves the restore yield further by doubling the X node voltage difference from $\min(V_{TRIP} - V_L, V_H - V_{TRIP})$ to $V_H - V_L$.

3. Simulation Results and Comparison

3.1. Simulation Conditions

In this paper, only the SLS structure based NVFFs [10–13] are simulated and compared for the purpose of optimizing the sensing circuit (restore yield, read disturbance margin) and flip-flop core (clock to Q delay) independently. The simulation and comparison of the silicon-proven merged latch and sensing circuit (MLS) structure based NVFFs can be found in the reference texts (see [13]).

To fairly compare the four state-of-the-art NVFFs [10–13], similar or identical transistor sizes are used to equalize the effect of process variation of devices that affect the sensing operation of stored data. All transistors use the minimum length of 30 nm. All capacitor values are 4 fF. For the write driver, PMOS (P_{W1} and P_{W2}) width is 3 µm and NMOS (N_{W1} and N_{W2}) width is 1 µm. For the transmission gate access transistors which act as switches, NMOS and PMOS width is 0.5 µm. In case of Na's NVFF [10] and Choi's NVFF [13], PMOS (P_{SEN2}, P_{SEN1}) width is 1 µm and NMOS (N_{SEN1}) width is 0.5 µm for the sensing inverter. In case of Song's NVFF [11] and Na's NVFF [12], PMOS header width is 2 µm and NMOS footer width is 1 µm. Width of NL, NL2, NR, and NR2 is 0.5 µm. R_L of 3 kΩ and R_H of 6 kΩ are selected by a tunnel magnetoresistance (TMR) ratio of 100% [37], where the TMR is defined as $(R_H - R_L)/R_L \times 100$. To consider the MTJ resistance (R_L and R_H) variation, a standard deviation of 4% is assumed for MTJ [38]. The I_C of the MTJ relies on the QCT benchmark 20 nm perpendicular MTJ model [10,39], as shown in Figure 3.

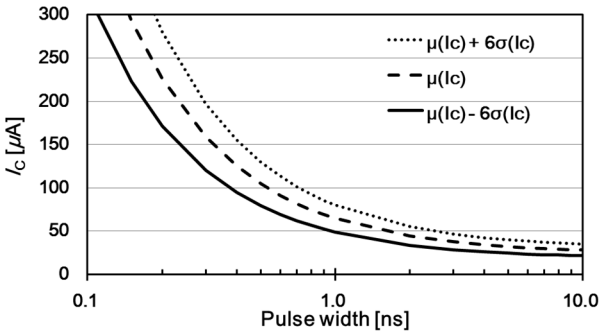

Figure 3. Critical switching current (I_C) of MTJ according to pulse width [10].

The target restore yield is set to 4σ, which satisfies the yield of 96.88% ($=\Phi(4\sigma)^{1000}$) assuming 1000 FFs. The target read disturbance margin is set to 6σ, which satisfies the yield of 99% assuming 1000 access per a single cell when considering the stochastic nature of MTJ. For satisfying more than 6σ read disturbance margin, the sensing current and its pulse width flowing through MTJ must be below the solid line of $\mu(I_C) - 6\sigma(I_C)$ in Figure 3. The sensing time is optimized according to the read disturbance margin of state-of-the-art NVFFs. The NVFF restore yield is obtained by performing HSPICE Monte Carlo simulations using industry-compatible 28 nm model parameters. The V_{DD} of 0.6 V and 0.4 V are used for super-threshold and near/sub-threshold voltage operations, respectively. The transistor type is low V_{TH} type for better performance at near/sub-threshold voltage region. The target restore yield of 4σ is estimated at all corners of the NMOS and PMOS.

3.2. Simulation Results and Comparison

Figure 4 shows the restore yield of three state-of-the-arts NVFFs [11–13] having the offset-tolerant characteristic relative to the capacitance (C_{SA} or C_{EQ}) value at SS corner (NMOS = Slow, PMOS = Slow), which is the worst corner in the NVFF design. The capacitance value is important to capture and hold the V_{TH} of NL, NR [11,12] and V_{TRIP} [13] for offset cancellation. Furthermore, the larger capacitance value can achieve a higher restore yield since it is possible for capacitor to transfer the more voltage variation values effectively known as capacitive coupling. Thus, the sufficient capacitance value is selected to achieve the target restore yield of 4σ. Even though Song's NVFF [11] accepts the offset tolerant scheme, Song's NVFF [11] shows lower restore yield than other offset tolerant NVFFs. The reason is that Song's NVFF shows low offset cancellation effectiveness because the two output nodes Y and Y_B are connected through MTJ_A and MTJ_B during the offset cancellation phase. It makes Song's NVFF achieve low restore yield.

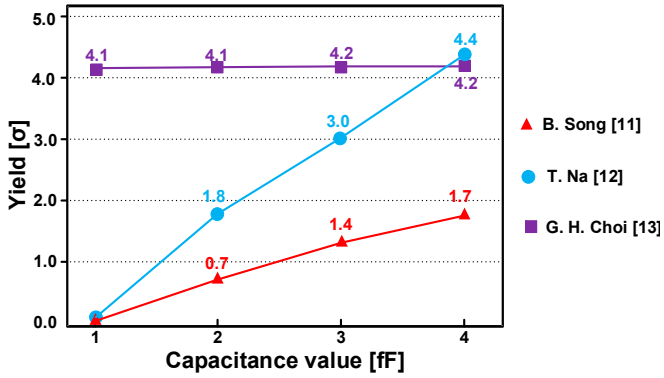

Figure 4. Restore yield of three state-of-the-arts NVFFs [11–13] having the offset-tolerant characteristic relative to the capacitance (C_{SA} or C_{EQ}) value at SS corner (NMOS = Slow, PMOS = Slow). For this simulation, V_{DD} of 0.6 V is used.

Figure 5 shows the restore yield of four state-of-the-art NVFFs [10–13] relative to the MTJ variation at SS corner. The restore yield of state-of-the-art NVFFs reduces according to the increase in the MTJ variation because it is possible to reduce the resistance difference between MTJ_A and MTJ_B. In other words, if the sufficient resistance difference margin is not satisfied, the sensing will be failed since the sensing margin decreases. This figure also clearly shows that if the MTJ variation is more than 8%, all NVFFs cannot satisfy the target restore yield of 4σ, meaning that the MTJ variation is a critical factor degrading the restore yield.

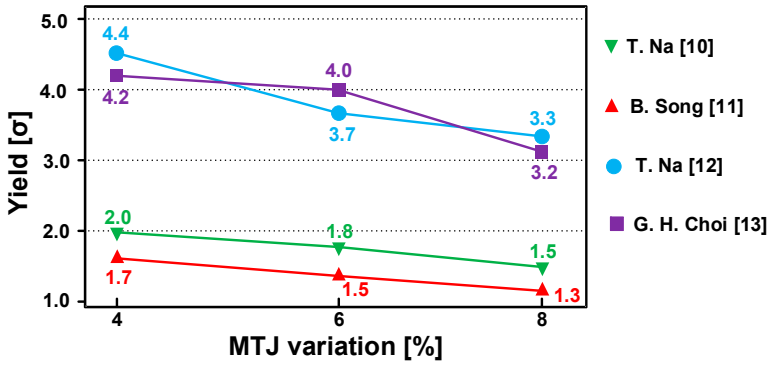

Figure 5. Restore yield of four state-of-the-art NVFFs [10–13] relative to the MTJ variation at SS corner. For this simulation, V_{DD} of 0.6 V is used.

Figure 6 shows the restore yield of state-of-the-art NVFFs relative to the MTJ stress time during the sensing mode at SS corner, where the MTJ stress time is the current pulse width flowing through

the MTJ during the sensing (restore) mode. It is worth noting here that not only reducing I_{read} but also reducing the MTJ stress time is important to prevent the read disturbance. Generally, the restore yield of the state-of-the-art NVFFs increase when MTJ stress time increases. The NVFFs with effective offset cancellation techniques [12,13] show much higher restore yield than the NVFFs without offset cancellation [10] and with ineffective offset cancellation [11].

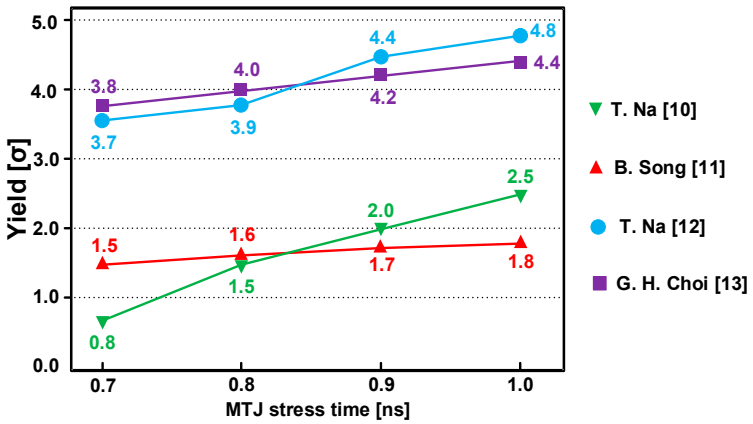

Figure 6. Restore yield of state-of-the-art NVFFs relative to the MTJ stress time during the sensing mode at SS corner. For this simulation, V_{DD} of 0.6 V is used.

Figure 7 shows the restore yield relative to V_{DD} during the sensing mode at SS corner. Generally, the restore yield reduces with decreasing V_{DD} as expected. Note that at V_{DD} = 0.5 V, Na's NVFF without offset cancellation technique [10] achieves the highest restore yield than other three NVFFs having the offset cancellation characteristic. Because the offset-cancellation technique uses switch operation in the critical path, the increase in the variation of the transmission gates with decreasing V_{DD} increases the offset voltage of the three NVFFs [11–13], resulting in the restore yield degradation in the near/sub-threshold voltage region further compared to the non-offset tolerant NVFF [10].

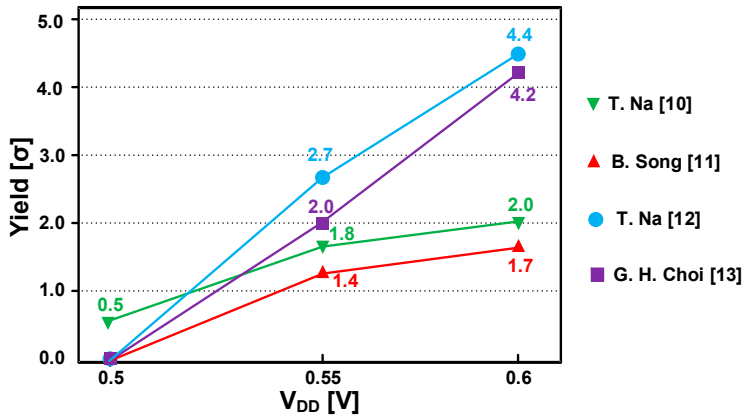

Figure 7. Restore yield of state-of-the-art NVFFs relative to V_{DD} during the sensing mode at SS corner. For this simulation, the MTJ stress time was fixed to 0.9 ns.

Figure 8 shows the restore yield of state-of-the-art NVFFs relative to the V_{DD} when the MTJ stress time is increased from 0.9 ns (Figure 7) to 1.5 ns at SS corner. To prevent the restore yield degradation caused by the lack of the sensing time as V_{DD} decreases, a sufficient MTJ stress time of 1.5 ns is applied. Generally, the restore yield of all state-of-the-art NVFFs decreases as V_{DD} decreases. Like the result of Figure 7, Na's NVFF [10] shows the highest restore yield than other offset tolerant NVFFs [11–13] when V_{DD} is equal to 0.5 V.

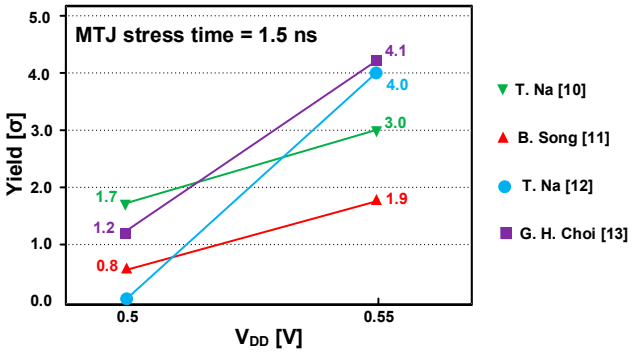

Figure 8. Restore yield of state-of-the-art NVFFs relative to the V_{DD} when the MTJ stress time is increased from 0.9 ns (Figure 7) to 1.5 ns.

Figure 9 shows the restore yield of state-of-the-art NVFFs relative to the width size of all devices when MTJ stress time = 1.5 ns, V_{DD} = 0.5 V, and SS corner. The default size (×1) for all devices can be found in Section 3.1. Generally, the restore yield increases as the size increases because of the decrease in the process variation. Interestingly, from ×1 to ×4 width sizes, Na's NVFF [10] has the highest restore yield. Unlike the three NVFFs [11–13] having the offset-tolerant characteristic, Na's NVFF [10] does not have any complex circuit operation. Similar to the notion that the simplest is the best, these simulation results provide insight that a simple circuit can provide the best performance in the near/sub-threshold voltage region.

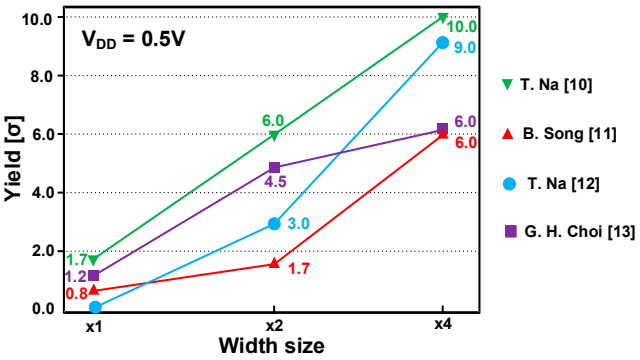

Figure 9. Restore yield of state-of-the-art NVFFs relative to the width size of all devices when MTJ stress time = 1.5 ns, V_{DD} = 0.5 V, and SS corner.

Figure 10 shows the restore yield of state-of-the-art NVFFs relative to the V_{DD} when MTJ stress time is 1.5 ns and width size of all devices is equal to the default size times 4 (×4) during the sensing mode at SS corner. It clearly shows that the simple circuit (NVFF [10]) provides a much better restore yield compared to the complex circuits (other NVFFs [11–13]) in the near/sub-threshold voltage region.

Tables 1 and 2 summarize the comparison between the four state-of-the-art NVFFs [10–13] in cases of V_{DD} of 0.6 V and 0.4 V, respectively. In case of Table 1, because V_{DD} is relatively high (slightly higher than near-threshold voltage region), the NVFFs [12,13] having the offset tolerance characteristic show better restore yield achieving the target restore yield of 4σ under the design and reliability constraint, especially the read disturbance margin of 6σ. In case of Table 2, on the other hand, because V_{DD} is in the near/sub-threshold region, the offset tolerant NVFFs [12,13] do not provide better restore yield, while the simplest NVFF having no offset tolerance characteristic shows the highest restore yield of 3.5σ. These simulation results provide insight that a simple circuit having no additional offsets which come from switch operations can provide a better restore yield in the near/sub-threshold voltage region.

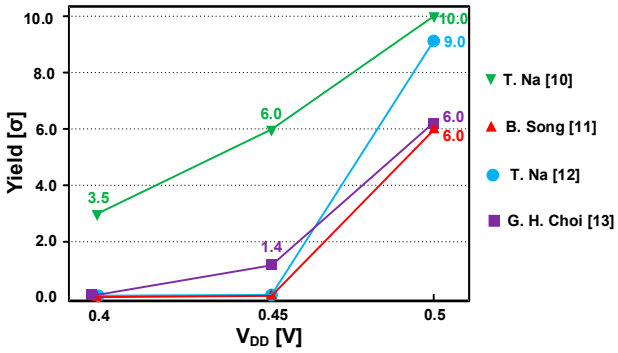

Figure 10. Restore yield of state-of-the-art NVFFs relative to the V_{DD} when MTJ stress time is 1.5 ns and width size of all devices is equal to the default size times 4 (×4) during the sensing mode at SS corner.

Table 1. Performance summary and comparison between the four state-of-the-art NVFFs [10–13] in case of V_{DD} of 0.6 V.

	T. Na, ISCAS 14′ [10]	**B. Song, TCAS-1 19′ [11]**	**T. Na, IEEE ACCESS 20′ [12]**	**G. H. Choi, IEEE ACCESS 20′ [13]**
V_{DD} [V]	0.6	0.6	0.6	0.6
Default size	×1	×1	×1	×1
MTJ stress time [ns]	0.9	0.9	0.9	0.9
Restore yield [σ]	2.0	2.1	4.4	4.2
Circuit Complexity	Simple (no offset tolerance)	Complex (less offset tolerance)	Complex (offset tolerance)	Complex (offset tolerance)

Table 2. Performance summary and comparison between the four state-of-the-art NVFFs [10–13] in case of V_{DD} of 0.4 V.

	T. Na, ISCAS 14′ [10]	**B. Song, TCAS-1 19′ [11]**	**T. Na, IEEE ACCESS 20′ [12]**	**G. H. Choi, IEEE ACCESS 20′ [13]**
V_{DD} [V]	0.4	0.4	0.4	0.4
Default size	×4	×4	×4	×4
MTJ stress time [ns]	1.5	1.5	1.5	1.5
Restore yield [σ]	3.5	0	0	0
Circuit Complexity	Simple (no offset tolerance)	Complex (less offset tolerance)	Complex (offset tolerance)	Complex (offset tolerance)

4. Conclusions

While the technology node scales down, the battery lifetime of the IoT device is suffering from leakage current problems. To solve this problem, the STT-MTJ based NVFF to store data and turn off supply voltage is important when the IoT device is in the standby mode. In this paper, the four state-of-the-art STT-MTJ-based NVFFs with the SLS structure for the purpose of optimizing the sensing circuit without the degradation of the slave latch operation were selected and simulated with considering the restore yield, and observed that (1) in the above-threshold voltage region (e.g., 0.6 V) under design and reliability constraint, it cannot guarantee reliable restore yield if offset tolerant scheme is not applied or its effectiveness is too low, and (2) in the near/sub-threshold voltage region (e.g., 0.4 V) with sizing up strategy, a simple circuit having no offset tolerance characteristic provides a better restore yield. In other words, to achieve the ultralow power operation by using the near/sub-threshold voltage region, a simple circuit can be much better, similar to the notion that the simplest is the best. This analysis is expected to help to improve the circuit design methods of NVFF sensing further for ultralow power IoT applications.

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Conflicts of Interest: The author declares no conflict of interest.

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