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A New High Voltage Gain DC to DC Converter with Low Voltage Stress for Energy Storage System Application

Javed Ahmad ¹ , Chang-Hua Lin ¹ , Mohammad Zaid ² , Adil Sarwar ² , Shafiq Ahmad ^{3,*} , Mohamed Sharaf ³, Mazen Zaindin ⁴ and Muhammad Firdausi ³

¹ Department of Electrical Engineering, National Taiwan University of Science and Technology, No. 43, Keelung Rd., Sec.4, Da'an Dist., Taipei City 10607, Taiwan; D10807822@mail.ntust.edu.tw (J.A.); link@mail.ntust.edu.tw (C.-H.L.)

² Department of Electrical Engineering, ZHCET, Aligarh Muslim University, Aligarh, Uttar Pradesh 202002, India; zaidahmadzhcet@gmail.com (M.Z.); adil.sarwar@zhcet.ac.in (A.S.)

³ Industrial Engineering Department, College of Engineering, King Saud University, P.O. Box 800, Riyadh 11421, Saudi Arabia; mfsharaf@ksu.edu.sa (M.S.); 438106660@student.ksu.edu.sa (M.F.)

⁴ Department of Statistics and Operations Research, College of Science, King Saud University, P.O. Box 800, Riyadh 11421, Saudi Arabia; zaindin@ksu.edu.sa

* Correspondence: ashafiq@ksu.edu.sa; Tel.: +966-543200930

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Abstract: Increasing energy demand globally has led to exploring ways of utilizing renewable resources for sustainable development. More recently, the integration of renewable distributed resources in small- and large-scale grid has been seriously researched. Development in renewable power sources and its integration with the grid require voltage level conversion to match the grid/micro-grid level. The voltage level conversion is brought about by employing Direct Current-Direct Current (DC-DC) converters with boosting features. The paper presents a wide gain range DC-DC boost converter with a low-stress on switching devices. The proposed converter's voltage gain is high compared with the conventional quadratic boost converter and other recently developed high gain boost converters. The topology has been compared with recently proposed topologies, and comparative analysis based on various performance parameters has shown that the topology is suitable for renewable and sustainable energy storage and grid integration. The power loss analysis has been done by incorporating the switching and conduction losses. A hardware prototype of 150 W has been developed to validate the converter's performance in steady-state as well as in dynamic conditions.

Keywords: energy storage system; high gain DC-DC converter; voltage stress; micro-grid

1. Introduction

DC-DC converter works on the principle of energy transfer between energy storage elements. By controlling this transfer of energy in one complete cycle, constant and high voltage can be obtained at the output. Conventional boost converter uses a single inductor and capacitor to obtain high voltage at the output. Other variants such as Cuk converters, Single Ended Primary Inductor Converters (SEPIC), and ZETA converters are also being developed to get high DC voltage output. These converters have a simple structure, but the voltage gain is limited [1]. Moreover, the stress across the switching devices is high, and efficiency is low. The converter cannot be operated at very high duty ratios as the conduction losses become elevated due to parasitic resistances and voltage gain decreases. Due to these problems, high gain DC-DC converters employing more than one inductor, and multiple capacitors can be employed to increase the converter's gain [2].

High gain DC-DC converters have increasingly become popular due to their suitability in solar Photovoltaic (PV) systems and electric vehicles. The output voltage from solar PV modules, fuel cells, and batteries is generally low and needs to be boosted up to maintain the DC-link voltage at the inverter's input [3]. The power flow in DC-DC converters can be unidirectional or bidirectional. Isolated topologies are suitable for high power applications and where efficiency required is high. Non-isolated topologies are usually used in low and [4] medium power applications where efficiency and electromagnetic interference are not significant concerns. Several isolated and non-isolated topologies use voltage multiplier cells (VMC) made up of switched inductors and capacitors to increase the converter's output voltage. In some topologies, a coupled inductor is also used in VMC to increase the gain of the converter. Another advantage of using VMC is that a high output voltage can be obtained at lower duty ratios [5].

Multilevel DC-DC structures use multiple switched capacitors [6] at the output stage to boost the output voltage. Authors have proposed a novel buck-boost and boost converters with continuous input current in [7] and [8], but the voltage gain is limited at higher duty ratios. A single switch modified SEPIC converter with a high voltage gain, and low voltage stress is proposed in [9]. Switched inductor topologies have an advantage that peak transient current through the switch is avoided as the capacitor is not charged directly through the source. The input current is also continuous if the inductor is on the input side. However, the gain is less as compared to the switched capacitor topology. The use of many inductors increases the weight and size of the circuit. Whereas multiple switched capacitors can easily enhance the converter's voltage gain substantially [10–12]. Switched capacitors, when employed with DC-DC converters, increase the gain of the converter substantially but the high charging current decreases the efficiency of the converter. In steady-state, the capacitors are in series and transfer their energy to load. Inductors are charged in the ON cycle, and during the OFF mode, the inductor discharges [13], and capacitors are charged in parallel. A new buck-boost converter with continuous input current with a quadratic gain is proposed [14].

Coupled inductor topologies have a high voltage gain, higher efficiency, and reduced voltage and current stresses across switches. The problem with coupled inductor topologies is that energy trapped in the leakage inductance needs to be recycled to avoid voltage transients across the switch and increase the circuit's overall efficiency. For this, an additional clamped circuit needs to be designed for these topologies [15–18], which increases the circuit's complexity. A new triple mode converter is proposed in [19], but many switches and inductors are required to obtain high voltage gain. The converter in [20] uses a Cockcroft-Walton based VMC to increase the gain of the converter. A new converter boost converter with VMC with switched capacitors is presented. The topology uses only a single inductor with switched capacitors, but the voltage gain [21] is limited. At lower duty ratios, the gain is little. Interleaved boost converters are characterized by a low ripple in current and low stress across the switches but require multiple VMCs (Voltage Doublers, Dickson Cells) at the output to boost the voltage.

Researchers have made efforts to optimize the number of VMCs to be used at the output so that a smaller number of components are required [22–24]. Another family of the DC-DC converter is quasi Z source converters. The input current for these converters is continuous, and the stress across switching devices and capacitors are low. However, these converters have limited voltage gain [25], [26], and cannot be operated at higher duty ratios. The DC-DC converter performance with non-ideal components is discussed in [27]. It is shown that at low input voltages and high duty ratios, the converter performance deteriorates. The voltage gain and efficiency both decreases substantially. Some other new and efficient topologies of the DC-DC converter with high gain is discussed in [28] and [29]. Quadratic boost topologies have the advantage that very high gain ratios can be obtained at [30] low duty ratios. Low duty ratio operation reduces the stress across devices and improves the efficiency of the converter. Quadratic boost converters (QBC) generally use switched inductors and capacitors to increase the converter's gain. Non-isolated QBC provides high gain with reduced stress on switches but at the cost of reducing the efficiency at higher duty ratios efficiency [31–33].

The advantages of non-isolated QBC over other topologies makes it a suitable choice for low and medium power applications [34,35]. The DC power supply can be given to a high gain converter and can be used even for a DC-AC high conversion application [36,37]. The switched capacitor application has also been discussed in [38–41].

This work's motivation and objective is to develop a new quadratic boost converter with voltage multiplier cells. The proposed converter's performance is an improvement over conventional QBC (CQBC) and other recently developed topologies. The voltage gain of the proposed converter is much higher than the conventional boost and CQBC. Along with low voltage stress across all components, the proposed converter's input current is also continuous, which is another desired feature of the proposed converter. The converters utilize only two inductors with the same gate signal to generate a high output voltage. The converter has a simple structure, and its control is easy. The converter performance is analysed in an open loop structure, and the converter's working in CCM is shown in Section 2. Voltage stress and design of passive components are shown in Section 3. A comparison of the proposed converter with other topologies is discussed in Section 4. The simulation and experimental results along with efficiency calculation discussed in Sections 5 and 6, respectively. The working of the proposed converter in dynamic conditions is discussed in Section 7. Discussion and conclusion are in Sections 8 and 9, respectively.

2. Proposed Topology

The conventional quadratic boost converter has one switch. The switch is connected across the load and hence has to bear the voltage stress equal to the output voltage (V_o). It utilizes two inductors, but the voltage gain remains limited.

The Proposed converter topology is shown in Figure 1. It has six passive components, namely two inductors and four capacitors. The proposed converter comprises two voltage multiplier cells (VMC), as shown in Figure 1. These VMCs are used to improve the voltage gain further and reduce the voltage stress on the switching components.

The proposed converter has two switches, and the same switching signal controls both. That is, both the switches are turned ON and turned OFF simultaneously. During the first mode of operation, when the control signal is high, both the switches are turned ON, diode D_2 and D_4 are conducting as shown in Figure 2.

The KVL equations during the first mode of operation are as follows:

$$V_{L1} = V_{in} + V_{C1} = V_{C2} \quad (1)$$

$$V_{L2} = V_{in} = V_{C4} \quad (2)$$

During the first mode of operation, the current in both the inductor increases, capacitor C_2 and C_4 charged while C_1 and C_3 discharged, as shown in Figure 3.

During the second mode of operation, when both the switches are turned OFF, diode D_1 and D_3 are conducting while remaining two diodes are reversed biased as shown in Figure 4. The current in both the inductor decreases, capacitor C_1 and C_3 are charged while the other two capacitors are discharged. The related equations during this mode of operation are as follows:

$$V_{L1} = 2V_{in} + 2V_{C1} - V_o \quad (3)$$

$$V_{L2} = V_{in} - V_{C1} \quad (4)$$

Figure 1. (a) Conventional quadratic boost converter (CQBC); (b). Proposed converter.

Figure 2. First mode of operation.

Figure 3. Related waveforms in continuous conduction mode (CCM).

Figure 4. The second mode of operation.

Now applying volt-sec balance in inductor L_2 .

$$\int_0^T V_{L2}(t) \cdot dt = 0 \quad (5)$$

$$V_{in} \times DT + (V_{in} - V_{C1}) \times (1 - D)T = 0 \quad (6)$$

$$V_{C1} = \frac{V_{in}}{1 - D} \quad (7)$$

Now applying volt-sec balance in inductor L_1 .

$$\int_0^T V_{L1}(t) \cdot dt = 0 \quad (8)$$

$$(V_{in} + V_{C1}) \times DT + (2V_{in} + 2V_{C1} - V_O) \times (1 - D)T = 0 \quad (9)$$

After combining Equations (7) and (9), the voltage gain (M) of the converter can be written as:

$$V_O = \frac{V_{in}(4 - 4D + D^2)}{(1 - D)^2} \quad (10)$$

Effect of Inductor's Parasitic Resistance on Voltage Gain

Due to the circuit's various components' internal resistance, there are some power losses in the circuit. Because of these power losses, the voltage gain is not the same as explained before; it is reduced to some lower value. The output voltage, considering the power loss in the inductors, could be calculated as follows:

$$P_{in} = P_o + P_{L_{loss_{total}}} \quad (11)$$

$$P_{in} = \frac{V_{in}V_o(4 - 4D + D^2)}{R(1 - D)^2} \quad (12)$$

$$P_{L_{loss_{total}}} = \left(\frac{V_o}{R(1 - D)}\right)^2 r_{L1} + \left(\frac{V_o(2 - D)}{R(1 - D)^2}\right)^2 r_{L2} \quad (13)$$

$$P_o = \frac{V_o^2}{R} \quad (14)$$

After combining the above equations, the output voltage obtained as:

$$V_o = \frac{V_{in}R(1 - D)^2(4 - 4D + D^2)}{R(1 - D)^4 + r_{L1}(1 - D)^2 + r_{L2}(2 - D)^2} \quad (15)$$

Using Equation (15), the proposed converter's non-ideal voltage gain is calculated with the inductor's parasitic resistance, which is 0.3Ω for each inductor. The results are compared with the ideal conditions and presented in Figure 5. At lower duty ratios, both the ideal and real voltage gains are the same, but as the duty ratio increases, the deviation between these two becomes large. Further, the deviation increases with the decrease in the load resistance because a reduction in the load resistance increases the current in the circuit, which increases the power loss in the circuit. As the duty ratio is increased, the current in the circuit also increases, which increases conduction power loss in the circuit. Due to this reason, the efficiency of the DC-DC converters decreases at higher duty ratios, and the output voltage gain starts decreasing after reaching its maximum value. It is always recommended to use these converters below a certain value of a duty ratio.

Figure 5. Ideal voltage gain and real voltage gain.

3. Voltage Stress, Current and Passive Component Selection

The voltage stress across S_1 , S_2 , D_2 , and D_4 is obtained by applying KVL during the second mode of operation, as shown in Figure 4. The voltage stress across diodes D_1 and D_3 could be obtained by applying KVL during the first mode of operation. The voltage stress and current across the switches and the diodes are shown in Table 1. It can be inferred from Table 1 that the voltage stress across

switches and diodes is much less than the output voltage, which makes the converter highly efficient. The low voltage stress across capacitors, switches, and diodes and the high voltage gain at lower duty ratios is the distinguishing feature of the proposed converter, making it superior to the literature's proposed topologies.

Table 1. Voltage stress and current across the switches and diodes.

Component	Voltage Stress (Volt)	Average Current during Their Conduction (Amp)	Average Current for the Complete Cycle (Amp)	RMS Current (Amp)
S_1	$\frac{V_{in}}{(1-D)} = \frac{V_O(1-D)}{(4-4D+D^2)}$	$\frac{V_O(2-D)}{R(1-D)^2}$	$\frac{V_O(2-D)D}{R(1-D)^2}$	$\frac{V_O(2-D)\sqrt{D}}{R(1-D)^2}$
S_2	$\frac{V_{in}}{(1-D)^2} = \frac{V_O}{(4-4D+D^2)}$	$\frac{V_O}{RD(1-D)}$	$\frac{V_OD}{RD(1-D)}$	$\frac{V_O\sqrt{D}}{R(1-D)}$
D_1	$\frac{V_{in}}{(1-D)} = \frac{V_O(1-D)}{(4-4D+D^2)}$	$\frac{V_O(2-D)}{R(1-D)^2}$	$\frac{V_O(2-D)}{R(1-D)}$	$\frac{V_O(2-D)}{R(1-D)^{3/2}}$
D_2	$\frac{2V_{in}}{(1-D)} = \frac{2V_O(1-D)}{(4-4D+D^2)}$	$\frac{V_O}{RD}$	$\frac{V_O}{R}$	$\frac{V_O}{R\sqrt{D}}$
D_3	$\frac{V_{in}(2-D)}{(1-D)^2} = \frac{V_O(2-D)}{(4-4D+D^2)}$	$\frac{V_O}{R(1-D)}$	$\frac{V_O}{R}$	$\frac{V_O}{R\sqrt{1-D}}$
D_4	$\frac{V_{in}}{(1-D)} = \frac{V_O(1-D)}{(4-4D+D^2)}$	$\frac{V_O}{RD}$	$\frac{V_O}{R}$	$\frac{V_O}{R\sqrt{D}}$

For the continuous mode of operation, the minimum current of each inductor should be greater than zero. The minimum current of the inductor depends on the current ripple and average current. The average current of each inductor and the minimum value of inductance of each inductor could be calculated as follows:

$$I_{L1} = \frac{V_O}{R(1-D)} \quad (16)$$

$$I_{L2} = \frac{V_O(2-D)}{R(1-D)^2} \quad (17)$$

$$L_1 \geq \frac{R(1-D)^2(2-D)D}{2f_s(4-4D+D^2)} \quad (18)$$

$$L_2 \geq \frac{R(1-D)^4D}{2f_s(4-4D+D^2)(2-D)} \quad (19)$$

The selection of the capacitors is based on the switching frequency as well as the permissible ripple in the voltage across the relationship between the capacitance, and other parameters are as follows:

$$C_1 = \frac{V_O}{R(1-D)f_s\Delta V_{C1}} = \frac{V_{in}(4-4D+D^2)}{R(1-D)^3f_s\Delta V_{C1}} \quad (20)$$

$$C_2 = \frac{V_O}{RDf_s\Delta V_{C2}} = \frac{V_{in}(4-4D+D^2)}{RD(1-D)^2f_s\Delta V_{C2}} \quad (21)$$

$$C_3 = \frac{V_OD}{Rf_s\Delta V_{C3}} = \frac{V_{in}D(4-4D+D^2)}{R(1-D)^2f_s\Delta V_{C3}} \quad (22)$$

$$C_4 = \frac{V_O}{Rf_s\Delta V_{C4}} = \frac{V_{in}(4-4D+D^2)}{R(1-D)^2f_s\Delta V_{C4}} \quad (23)$$

4. Comparison with Other Recent Topologies

This section compares the proposed topology with some other recent structures of step-up converters. The proposed topology is compared with topologies with quadratic gain and ultra-high gain boost converter [24]. Table 2 shows the overall comparison of the proposed topology with other recent topologies, where N denotes the number of components. As depicted in Figure 6, the proposed topology has the highest gain in the entire operation range in the non-isolated category of converters with 12 components. The topology's gain in [9] is less than the proposed converter, although it utilizes four inductors and a total of 14 components. The ultra-high gain boost converter is proposed in [24] and employs 12 components, but its gain is less than the proposed topology. The normalized voltage stress curve versus voltage gain is shown in Figure 7. The switch S_1 has the lowest stress across all compared to the stress on all other topologies. The voltage stress across S_2 is greater than S_1 , but for the voltage gain up to 10 times, it is lower than the stress of the converters in [9,10], [CQBC], and [33].

Table 2. Comparison of the proposed topology with other similar topologies.

Topology	N_L (Inductors)	N_C (Capacitors)	N_{SW} (Switches)	N_D (Diodes)	M (V_o/V_{in})	S (V_S/V_{in})
[9]	2	4	1	4	$\frac{3+D}{2(1-D)}$	$\frac{1}{1-D}$
[10]	4	1	2	7	$\frac{1+3D}{(1-D)}$	$\frac{1+D}{1-D}$
[11]	2	3	2	3	$\frac{3+D}{(1-D)}$	$\frac{1}{1-D}$
[17]	1+1 coupled inductor	3	1	5	$\frac{2-D}{(1-D)^2}$ $n=1$	$\frac{2}{1-D}$
[CQBC]	2	2	1	3	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[24]	2	4	2	4	$\frac{4}{(1-D)}$	$\frac{1}{1-D}$
[33]	2	3	1	3	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$
Proposed	2	4	2	4	$\frac{4-4D+D^2}{(1-D)^2}$	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1}{(1-D)^2}$

Figure 6. Comparison of Voltage gain vs. Duty ratio of proposed converter with other converters.

Figure 7. Normalized voltage stress vs. Voltage gain.

5. Simulation Results and Experimental Verification of the Proposed Converter

5.1. Simulation Results

To test the effectiveness of the proposed converter, the simulations are performed using PLECS software. The V_o at V_{in} of 24 V and $D = 0.4$ is found to be 167 V, as shown in Figure 8. The small voltage drop is because of the parasitic and ON state resistances of the converter. The inductor current is continuous, and the average value of I_{L1} and I_{L2} is found to be 1.1 A and 3.3 A, respectively, as shown in Figure 9. The capacitor voltages are shown in Figure 10. The capacitor voltages of C_1 , C_2 and C_4 are 39 V, 63 V, and 23 V, respectively, which is an agreement with the theoretical analysis. The voltage stress across the capacitor is much less than the V_o , which leads to the selection of capacitors of low voltage rating. The choice of low rating components increases the efficiency of the converter. The stress across switch S_1 and S_2 is 40 V and 66 V, as depicted in Figure 11.

Figure 8. Output Voltage at 24 V input and $D = 0.4$.

5.2. Experimental Verification

The hardware prototype is developed on the power circuit board (PCB) by using Altium Designer software. The designed PCB layout is shown in Figure 12. The hardware prototype is shown in Figure 13a, and the experimental setup is shown in Figure 13b. The specifications of the developed hardware prototype are shown in Table 3. The theoretical and simulation results are confirmed by developing a prototype and of 150 W in the lab. Figure 14 shows the experimental waveform of the V_o at $V_{in} = 24$ V and $D = 0.4$. V_o is found to be 167 V, which is in agreement with the derived voltage gain. The high gain of 7 times is obtained at a low-duty ratio is the converter's main advantage. The experimental inductor current waveforms are shown in Figure 15. The capacitor voltages are

shown in Figure 16. The capacitor voltages of C_1 , C_2 , and C_4 are much less than the output voltage V_o , which means that except for the output capacitor C_3 all the other capacitors have low voltage stress across them.

Figure 9. Inductor currents of L_1 and L_2 at $D = 0.4$.

Figure 10. Capacitor voltages of C_1 , C_2 , and C_4 at $D = 0.4$.

Figure 11. Output voltage and voltage stress across switch S_1 and S_2 at $D = 0.4$.

Figure 12. Proposed Converter power circuit board (PCB) Layout.

Figure 13. (a) Proposed converter; (b) experimental set-up.

Table 3. Specifications of the proposed converter.

Elements	Specification
Input Voltage (V_{in})	24 V
Maximum Output Power	150 W
Switching Frequency	50 kHz
Load Resistance	$R = 250 \, \Omega$, Electronic load simulator
Inductors	$L_1 = L_2 = 330 \, \mu\text{H}$, ESR = $0.3 \, \Omega$
Capacitors	$C_1 = 47 \, \mu\text{F}/100 \, \text{V}$ ESR = $0.26 \, \Omega$, $C_2 = C_3 = 33 \, \mu\text{F}/200 \, \text{V}$ ESR = $0.3 \, \Omega$ & $C_4 = 220 \, \mu\text{F}/50 \, \text{V}$ ESR = $0.20 \, \Omega$
Power MOSFET (S_1 & S_2)	SPW52N50C3, $R_{DSon} = 70 \, \text{m}\Omega$
Diodes (D_1 , D_2 , D_3 & D_4)	SF8L60USM, $V_d = 0.6 \, \text{V}$
Gate Drivers IC	TLP250H
Gate Driver Voltage Regulator IC	MCWI03-48S15
Microcontroller	STM32 Nucleo H743ZI2

Figure 14. Output voltage at 24 V input and $D = 0.4$.

Figure 15. Inductor currents of L_1 and L_2 at $D = 0.4$.

Figure 16. Capacitor voltages of C_1 , C_2 , and C_4 at $D = 0.4$.

The stress across switch S_1 and S_2 , as depicted in Figure 17, is found to be 40 V and 66 V, which is also much less than the V_o .

Figure 17. Output voltage and voltage stress across switch S_1 and S_2 at $D = 0.4$.

6. Efficiency Calculation

For the calculation of efficiency, the power loss in each component needs to be determined. The losses in switches are bifurcated into switching and conduction losses. The parasitic and ON state resistances are shown in Table 2. The total switching loss in switches S_1 and S_2 is found to be 0.298 W. The total conduction loss is found to be 0.773 W. The loss in capacitors:

$$\left\{ \begin{array}{l} P_{S_{loss_{conduction}}} = P_{S1_{loss_{conduction}}} + P_{S2_{loss_{conduction}}} \\ P_{S_{loss_{conduction}}} = i_{S1_{RMS}}^2 \times r_{S1} + i_{S2_{RMS}}^2 \times r_{S2} \\ = \left(\frac{V_O(2-D)\sqrt{D}}{R(1-D)^2} \right)^2 r_{S1} + \left(\frac{V_O\sqrt{D}}{R(1-D)} \right)^2 r_{S2} \\ P_{S_{loss_{conduction}}} = 0.285 \text{ W} \\ P_{S_{loss_{switching}}} = \frac{(t_{on} + t_{off})(I_{S1on}V_{S1off} + I_{S2on}V_{S2off}) \times f_s}{2} = 0.298 \text{ W} \\ P_{S_{loss_{(conduction+switching)}}} = 0.583 \text{ W} \end{array} \right. \quad (24)$$

The diode cut-in voltage for all diodes is 0.6 V the resistance is 0.06 Ω . The power loss for each of the diodes for an output voltage of 167 V and output power of 111.56 W can be calculated as shown.

$$\left\{ \begin{array}{l} P_{D1_{loss}} = V_{D1}I_{D1_{avg}} + i_{D1_{RMS}}^2 r_{D1} \\ P_{D1_{loss}} = 1.386 \text{ W} \\ P_{D2_{loss}} = V_{D2}I_{D2_{avg}} + i_{D2_{RMS}}^2 r_{D2} \\ P_{D2_{loss}} = 0.57 \text{ W} \\ P_{D3_{loss}} = V_{D3}I_{D3_{avg}} + i_{D3_{RMS}}^2 r_{D3} \\ P_{D3_{loss}} = 0.475 \text{ W} \\ P_{D4_{loss}} = V_{D4}I_{D4_{avg}} + i_{D4_{RMS}}^2 r_{D4} \\ P_{D4_{loss}} = 0.57 \text{ W} \\ P_{D_{loss_{total}}} = 3.001 \text{ W} \end{array} \right. \quad (25)$$

The total conduction losses in diodes are found to be 3 W.

The total conduction losses in capacitors are found to be 2.04 W.

$$\left\{ \begin{array}{l} P_{C_{loss_{total}}} = i_{C1_{RMS}}^2 r_{C1} + i_{C2_{RMS}}^2 r_{C2} + i_{C3_{RMS}}^2 r_{C3} + i_{C4_{RMS}}^2 r_{C4} \\ = \left(\frac{V_O}{R(1-D)} \sqrt{\frac{1+D-D^2}{D}} \right)^2 r_{C1} + \left(\frac{V_O}{R} \sqrt{\frac{1}{D(1-D)}} \right)^2 r_{C2} + \left(\frac{V_O}{R} \sqrt{\frac{D}{(1-D)}} \right)^2 r_{C3} + \left(\frac{V_O}{R} \sqrt{\frac{1}{D(1-D)}} \right)^2 r_{C4} \\ = 0.9 \text{ W} + 0.55 \text{ W} + 0.22 \text{ W} + 0.37 \text{ W} \\ P_{C_{loss_{total}}} = 2.04 \text{ W} \end{array} \right. \quad (26)$$

The parasitic resistance of each coil is found to be 0.3Ω . The loss in coils L_1 and L_2 can be computed as:

$$\left\{ \begin{array}{l} P_{L_{loss_{total}}} = i_{L1_{RMS}}^2 r_{L1} + i_{L2_{RMS}}^2 r_{L2} \\ = \left(\frac{V_O}{R(1-D)} \right)^2 r_{L1} + \left(\frac{V_O(2-D)}{R(1-D)^2} \right)^2 r_{L2} \\ = 0.372 \text{ W} + 2.64 \text{ W} \\ = 3.01 \text{ W} \end{array} \right. \quad (27)$$

The total conduction losses in inductors are found to be 3.01 W. The bifurcation of losses in various components are shown in Figure 18. The loss in diodes and switches constitute around 46 percent of the total losses. The total loss in the converters is found to be 8.634 W.

Figure 18. Bifurcation of losses in the proposed converter.

Efficiency (η) of the converter can be expressed as:

$$\left\{ \begin{array}{l} \eta = \frac{P_0}{P_0 + P_{loss} + P_{D,loss} + P_{C,loss} + P_{L,loss}} \\ \eta\% = \frac{\frac{167^2}{250}}{\frac{167^2}{250} + 8.634} \times 100 = 92.82\% \end{array} \right. \quad (28)$$

For an output power of 111.56 W, the efficiency is found to be 92.82%. The variation of efficiency with output power is shown in Figure 19a. The efficiency of the converter increases as the input voltage is increased. This increase in efficiency is because at higher input voltages, a small duty ratio is required to get the same amount of voltage gain, and hence conduction losses are significantly reduced.

In Figure 19b, the comparison of efficiency at an input voltage of 24 V is shown. The coupled inductor topology proposed in [17] has higher efficiency than the proposed converter.

Figure 19. (a) Experimental efficiency of the converter; (b) Comparison of efficiency of the proposed converter.

7. Performance of the Proposed Converter in Dynamic Conditions

The dynamic conditions are presented in Figures 20 and 21. While changing the duty ratio, the load resistance is kept constant at $200\ \Omega$. With the increase in the duty ratio, the voltage gain increases without any transient, as shown in Figure 20. To capture the dynamic load change, the electronic load is set to change its load between 100% and 75% of the rated load, and the duty ratio is kept constant at 0.4. With the increase in the load, the output current increases, which increases the internal power losses in the circuit, and output voltage decreases a little bit, as shown in Figure 21.

Figure 20. Effect of the change in duty on V_O and I_O .

Figure 21. Effect of change in load on V_O and I_O .

8. Discussion

From the steady-state and dynamic performance, it can be observed that the converter is working satisfactorily in an open loop. The output voltage and currents obtained through experimental investigations closely match the theoretical and simulation results. Further, the stress across switches capacitors and diodes is less than the output voltage. The low voltage stress leads to the selection of devices with low voltage ratings, which ultimately improves efficiency and decreases the converter's cost. The proposed converter is suitable for low and medium power applications. It is to be noted that the parasitic resistances of inductors decrease the voltage gain and the efficiency of the converter [38,39]. To increase the converter's gain and efficiency at high duty ratios, a coupled inductor can also be used in the proposed topology instead of two separate inductors.

9. Conclusions

The main challenge in developing high gain DC-DC converters is to get high voltage gain by keeping the stress across devices low. Further, the number of components should also be optimized so that the converter cost is low and high efficiency can be obtained. These features are obtained in the proposed high gain converter. The converter has been successfully developed, and its performance is validated through simulation and experimental results. The converter's loss analysis reveals its good performance with more than 91% efficiency throughout the input power range. The peak efficiency was found to be 93.6% at 66 W output power. The voltage gain of the converter is high at low duty ratios. A gain of more than 12 times can be achieved in ideal conditions at a duty ratio of 0.6. However, the actual gain depends on the parasitic values of different components and the load resistance. Overall, the proposed converter has shown good performance in non-isolated category of converters and can be employed in industrial, energy storage, and PV applications.

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Abbreviation

V_{in}	Input Voltage
V_O	Output Voltage
V_L	Inductor Voltage
V_C	Capacitor Voltage
ΔV_C	Capacitor Voltage Ripple
ΔI_L	Inductor Current Ripple
R	Load Resistance
D	Duty Ratio
P_{in}	Input Power
P_O	Output Power
P_{loss}	Power Loss
r_{L1}, r_{L2}	Parasitic resistance of inductor
$r_{C1}, r_{C2}, r_{C3}, r_{C4}$	Parasitic resistance of capacitors
$r_{D1}, r_{D2}, r_{D3}, r_{D4}$	Parasitic resistance of diodes

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