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Instability in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ Quantum-Well MOSFETs with Single-Layer Al_2O_3 and Bi-Layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ Gate Stacks Caused by Charge Trapping under Positive Bias Temperature (PBT) Stress

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Abstract: The instability of transistor characteristics caused by charge trapping under positive bias temperature (PBT) stress in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ metal oxide semiconductor field-effect transistors (MOSFETs) with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks was investigated. The equivalent field across the multi-gate stacks was compared with a single layer used to compare the instability of electrical characteristics. The observed threshold voltage degradation (ΔV_T) was consistent with the phenomenon of fast transient trapping of injected electrons at pre-existing shallow defects in the high- κ dielectric of HfO_2 , in which this charging was recovered by applying a relaxation voltage. Excluding the fast-transient charging components, the power law exponent (n), with respect to the time-dependent threshold voltage degradation, ranged from 0.3 to 0.35 for both single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks. This long-term (slow) V_T shift, which was strongly correlated with transconductance (G_m) degradation, was attributed to significant charge trapping in the border trap or/and defect sites within the high- κ dielectric.

Keywords: InGaAs MOSFET; atomic layer deposition (ALD); interfacial trap density (D_{it}); charge trapping; instability of electrical characteristics; transconductance (G_m) degradation; positive bias temperature (PBT) stress

1. Introduction

III-V n -channel metal oxide semiconductor field-effect transistors (MOSFETs) have demonstrated much better electron mobility and injection velocity than transistors with a silicon (Si) channel, making them attractive for future high-speed, low-power logic applications [1–3]. Among the various channel materials (GaAs, InP, GaN, and InGaAs) in III-V MOSFETs [1–5], interest in indium-rich $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel materials, $x > 0.53$, have recently been considered the most promising replacement of conventional Si-based n -channel materials because of their high electron mobility, high drive current capability, and mature technology for defense applications [3–5]. The small electron effective mass of indium-rich $\text{In}_x\text{Ga}_{1-x}\text{As}$ quantum-well (QW) channels has led to a significant increase of importance of a ballistic transport in the overall electron transport because of the carrier confinement to a deep quantum well [4,5]. The QW structures compared with the n -MOSFET provide better electrostatic control of the channel from the top gate as the devices are aggressively scaled down [4,5]. However, the unstable native oxides on III-V channel materials, such as As_2O_3 , As_2O_5 , and InO_x , lead to poor electrical properties [6,7]. To fully benefit from intrinsic properties, it is important to minimize the

interfacial defect sites in the interfacial self-cleaning reaction process via atomic layer deposition (ALD) using trimethylaluminum (TMA) as the precursor for the Al_2O_3 layer [6–8]. An Al_2O_3 layer is insufficient for providing a low equivalent oxide thickness (EOT) and low gate leakage current [4,5]. Therefore, several researchers have deposited high- κ dielectrics, such as HfO_2 (~25) and ZrO_2 (~30), on ultrathin Al_2O_3 layers, improving the electrical properties [4,5,9,10]. The defect sites associated with interfacial traps and high- κ dielectric layers deteriorate the subthreshold-swing (SS) and mobility in the channel, and therefore degrade the on current (I_{ON})/off current (I_{OFF}) ratio [4]. Electron trapping phenomena for InGaAs QW MOSFETs with a high- κ dielectric during device operation can cause a frequency dispersion and shift in ΔV_T , which would cause a severe reliability concern [9,10]. Use of the InGaAs QW MOSFETs to realize the next n-MOSFET application has faced major reliability issues [9,10]. In particular, the electrical parameters under the positive bias temperature (PBT) stress condition may change over operation time, including the on current, threshold voltage degradation, SS, and transconductance (G_m) degradation [9,10]. The degradation of InGaAs QW MOSFETs under the PBT stress condition might be more important than that of the Si-based MOSFETs due to higher interfacial trap density (D_{it}) and border and bulk traps with high- κ dielectric. There have been only a few reports regarding the relevant instability of electrical characteristics issues in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs with high- κ dielectrics.

In this paper, we report a study on the instability of electrical characteristics for $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$. To verify the degradation mechanism of $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs with the high- κ dielectric under PBT stress condition, the electrical field across single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks were observed. Finally, we investigated the relationship between ΔV_T degradation, injected charge, and $G_{m,\text{Max}}$ degradation under different PBT stress conditions in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks.

2. Experimental Details

The epitaxial layer in the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs consists of a heavily doped n^+ InGaAs capping layer, an $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ channel, an inverted Si δ -doping layer, and an $\text{In}_{0.48}\text{Al}_{0.52}\text{As}$ back buffer or barrier on an InP substrate [3–5]. Mesa etching was performed by wet chemical etching to isolate the devices. Source and drain ohmic contacts to the n^+ InGaAs were formed using e-beam evaporation and subsequent lift-off of the Mo/Ti/Au metal stack. SiO_2 was deposited at the temperatures $<150^\circ\text{C}$ by plasma-enhanced chemical vapor deposition (PECVD), and the gate pattern was defined by electron beam lithography (EBL). SiO_2 on the heavily doped n^+ InGaAs capping layer was etched using CF_4 reactive ion etching (RIE). Gate recess process of the heavily doped n^+ InGaAs capping layer was etched to expose the InP layer using an H_3PO_4 based solution. Then, either Al_2O_3 (2.0 nm) or Al_2O_3 (0.7 nm)/ HfO_2 (1.6 nm) stacked dielectrics were grown sequentially on the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ channel using ALD. Deposition temperatures used for the Al_2O_3 and HfO_2 were 250°C and 150°C , respectively. After deposition of the high- κ gate stack on the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ channel, a 5-nm TiN metal-gate (MG) was deposited in-situ by ALD. Finally, a Ti/Au gate metal pad was deposited by beam evaporation. The electrical characteristics were evaluated using an Agilent 4156C semiconductor parameter analyzer. The PBT stress condition ($V_{\text{GS}} - V_T = V_{\text{stress}}$), which was normalized to V_T , was applied at the gate with the other terminals grounded. The instability of electrical characteristics under PBT stress condition was performed by a Summit 11K Cascade probe station with an integrated Temptronic thermochuck able to heat the wafer till temperatures to 200°C . The injected electron on each stress time was being monitored by the gate current under the PBT stress condition. The injected charge (Q_{inj}) was obtained from the monitored gate current integral of each stress time.

3. Results and Discussion

3.1. Distribution of the Electrical Field Across Gate Stacks on the Applied Stress Voltage

To compare the instability of electrical characteristics of single layer and multi-gate stacks, it is imperative to consider the equivalent field across the multi-gate stacks compared with a single layer because it is further complicated by the interaction between different materials [11,12]. The $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs structure with a high- κ dielectric usually consists of multi-gate stacks, including the interfacial layer and the high- κ dielectric layer. Hence, the electrical field across multi-gate stacks can be determined easily base on simple electrostatics rules as reported in References [11,12]. The electrical field in bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks in the $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs is given by Equation (1) [11]

$$\begin{aligned} E_{\text{Al}_2\text{O}_3} &= \frac{V_A}{\left(\frac{\epsilon_{\text{Al}_2\text{O}_3}}{\epsilon_{\text{HfO}_2}}\right)t_{\text{HfO}_2} + t_{\text{Al}_2\text{O}_3}} \\ E_{\text{HfO}_2} &= \frac{V_A}{\left(\frac{\epsilon_{\text{HfO}_2}}{\epsilon_{\text{Al}_2\text{O}_3}}\right)t_{\text{Al}_2\text{O}_3} + t_{\text{HfO}_2}} \end{aligned} \quad (1)$$

where E_{HfO_2} and $E_{\text{Al}_2\text{O}_3}$ are the electrical fields across the high- κ dielectric and interfacial layers, respectively. t_{HfO_2} and $t_{\text{Al}_2\text{O}_3}$ are the physical thicknesses. κ_{HfO_2} and $\kappa_{\text{Al}_2\text{O}_3}$ are the dielectric constants. V_A is the applied voltage or the applied stress voltage across gate stack.

To understand the role of the interfacial layer and high- κ dielectric layer, the calculated electrical field and the energy-band diagram for single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ is plotted with respect to the applied stress voltage as shown in Figure 1. If the electrical field in the ultra-thin interfacial layer is sufficiently high, most carriers of InGaAs channel easily tunnel across the interfacial layer to border traps or/and defect sites within the high- κ dielectric layers [11,13,14]. It is important to verify the degradation of the main high- κ dielectric layer caused by the applied stress voltage.

Figure 1. Distribution of each electrical field across (a) single-layer Al_2O_3 and (b) bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ on the applied stress voltage. Schematics of energy band diagram of (c) single-layer Al_2O_3 and (d) bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ under positive bias temperature (PBT) stress conditions.

The electric field in the main high- κ layers, which are HfO₂ for bi-layer Al₂O₃/HfO₂ gate stacks and Al₂O₃ for single-layer Al₂O₃, is similar according to the calculated effective thickness. Generally, the electrical stress fields in the silicon dioxide layer in Si-based high- κ dielectric and silicon germanium (SiGe) MOSFETs have been reported to be on the order of 5–6 MV/cm, which is a dominant region in the Fowler–Nordheim (F-N) tunneling mechanism [11,12]. Although the time zero dielectric breakdown (TZDB) voltage of the high- κ dielectrics in III-V MOSFETs is similar to the values previously reported for high- κ dielectrics [11,12], the smaller band gap of the InGaAs channel and higher D_{it} between the InGaAs channel and interfacial layer in III-V MOSFETs may seriously degrade the dielectric/substrate interface and high- κ region because of the high vertical field [11,12]. Because these phenomena are related to the properties (effective mass, band gap, etc.) of the channel materials themselves, these stress conditions for the QW III-V MOSFETs, which are 5–6 M/cm, may be inadequate. Therefore, the appropriate PBT stress voltage should be chosen considering the properties of the channel materials and the higher D_{it} between the InGaAs channel and high- κ dielectric.

3.2. Impact of Charge Trapping in Defect Sites under Positive Bias Temperature (PBT) Stress Condition

Figure 2 presents the trapping and relaxation characteristics during two stress/recovery cycles for single-layer Al₂O₃ and bi-layer Al₂O₃/HfO₂ In_{0.7}Ga_{0.3}As QW MOSFETs under different PBT stress conditions. The observed threshold voltage degradation (ΔV_T) is consistent with the phenomenon of electron trapping at defect sites within the high- κ dielectric layer. These charges can be detrapped by applying a relaxation voltage at $V_{GS} = 0$ V, as shown in Figure 2. The ΔV_T degradation may be related to two types of traps: The fast-transient trap over short durations (<1 msec) and the slow trap over long durations [13–18]. The initial V_T shift for single-layer Al₂O₃ and bi-layer Al₂O₃/HfO₂ In_{0.7}Ga_{0.3}As QW MOSFETs during the first 1 s of DC stress shows a substantial change because of the fast transient charging at defect sites in the HfO₂ dielectric, while the initial ΔV_T shift is much less in the Al₂O₃ In_{0.7}Ga_{0.3}As QW MOSFETs [15–18]. The fast-transient charging is from electron tunneling from the InGaAs surface directly into the pre-existing shallow traps within the high- κ dielectric layer, which should be subtracted from the initial 1 s stress for a more accurate evaluation [13,14]. The time dependence of the ΔV_T degradation was investigated to quantitatively studying the charge trapping phenomenon. After subtracting the fast-transient charge trapping component, which is reported to fully saturate within <1 s of stress, the time dependency of the V_T shift ($\Delta V_T - \Delta V_{T,initial} (1\text{ s})$) can be described by a power law expression $\Delta V_T \sim t^n$ [13–19]. The exponent n of this dependency is in the range of 0.3 to 0.35 for single-layer Al₂O₃ and bi-layer Al₂O₃/HfO₂ gate stacks, as shown in Figure 3. Note that ΔV_T values for bi-layer Al₂O₃/HfO₂ gate stacks are greater than that for single-layer Al₂O₃ while the exponent n values are similar, which are likely associated with the higher trap density in the HfO₂.

Figure 2. Comparison of charge trapping and relaxation characteristics in In_{0.7}Ga_{0.3}As metal oxide semiconductor field-effect transistor (MOSFET) with (a) single-layer Al₂O₃ and (b) bi-layer Al₂O₃/HfO₂ gate stacks under PBT stress at different overdrive conditions.

Figure 3. The power law time dependency of the observed threshold voltage degradation (ΔV_T) excluding the fast-transient charge trapping components ($\Delta V_T - \Delta V_{T,initial}$ (1 s)) in single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks under PBT stress conditions. The power law exponent n is 0.30–0.35.

To further investigate the charge trapping characteristics, ΔV_T was plotted as a function of the injected charge under different PBT stress conditions as shown in Figure 4a. The similar slopes of $Q_{trapped}/Q_{inj}$ for single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks (Figure 4b) indicate that these stacks exhibited similar charge trapping efficiencies [11,15,16,20–22]. The injected charges from the InGaAs channel are mostly trapped in defect sites within the high- κ dielectric. The long-term V_T shift, $\Delta V_T - \Delta V_{T,initial}$ (1 s), correlates well with the percentage of transconductance ($\%G_{m,Max}$) degradation for single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks, as shown in Figure 5. Generally, $G_{m,Max}$ degradation is related to the generation of interfacial state traps and Coulomb centers in the near-interface dielectric region [21,22]. However, $G_{m,Max}$ degradation increases as the amount of trapped electrons increases, as shown in Figure 5, which means that remote scattering is a sensitive factor in high- κ dielectric [11,15,16,20–22]. Therefore, the correlation seen between the $G_{m,Max}$ and $\Delta V_T - \Delta V_{T,initial}$ (1 s) implies that significant charge trapping occurred in the border trap or/and defect sites within the high- κ dielectric, which is in the main high- κ dielectric layers for single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks.

Figure 4. Cont.

Figure 4. (a) ΔV_T degradation as a function of the injected charge for an $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ quantum-well (QW) MOSFETs with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks under PBT stress conditions and (b) the $Q_{\text{trapped}}/Q_{\text{inj}}$ ratio as a function of the injected charge for both gate stacks.

Figure 5. $\Delta V_T - \Delta V_{T,\text{initial}}$ (1 s) shift versus $\%G_{m,\text{Max}}$ degradation in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MOSFETs with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks. Correlation between $\Delta V_T - \Delta V_{T,\text{initial}}$ (1 s) and $\%G_{m,\text{Max}}$ degradation is detectable in single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks.

Although the bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stack in $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW MOSFETs demonstrated superior electrical performance (compared with the Al_2O_3) because of its lower EOT [3–5], a large density of oxygen vacancies within high- κ dielectrics still caused V_T instability [11,15–18,20–23]. Since the defects in the HfO_2 -based dielectrics are related to oxygen vacancies in different charge states, from V^{2+} to V^{2-} levels as shown in Figure 1c [11,17,21–23], which can reversibly trap the injected electrons, improving the reliability characteristics of high- κ dielectric devices requires oxygen vacancies to be passivated. One of the methods is a high-pressure hydrogen or deuterium annealing.

4. Conclusions

We investigated the instability of electrical characteristics of III-V MOSFETs with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks under PBT stress. The initial (within the first stress second) ΔV_T shift in the bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ III-V MOSFETs was consistent with the phenomenon of fast transient trapping/detrapping of injected electrons at pre-existing shallow defects in the high- κ dielectric film. Long-term V_T degradation with single-layer Al_2O_3 and bi-layer $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate stacks in III-V QW

MOSFETs exhibited slow charging responsible for the ΔV_T power law time dependency. The observed correlation between the $\%G_{m,Max}$ and $\Delta V_T - \Delta V_{T,initial}$ (1 s) degradations indicated that this slow charge trapping occurred in border trap or/and defect sites within the high- κ dielectric, which was in the main high- κ dielectric layers of the single-layer Al_2O_3 and bi-layer Al_2O_3/HfO_2 gate stacks. These results indicate that the defect density must be reduced in the high- κ dielectric to improve the stability of $In_{0.7}Ga_{0.3}As$ QW MOSFETs with single-layer Al_2O_3 and bi-layer Al_2O_3/HfO_2 gate stacks.

Author Contributions: H.-M.K. conducted most of the experiments and wrote the manuscript including preparing figures and electrical characterization; D.-H.K. supervised the work and reviewed the manuscript; T.-W.K. initiated the work, provided the main idea, and supervised the entire process. All authors analyzed and discussed the results. All authors have read and agreed to the published version of manuscript.

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