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Thermal Stress Reduction of Power MOSFET with Dynamic Gate Voltage Control and Circulation Current Injection in Electric Drive Application

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Abstract: While operating an electric drive under different load conditions, power switch devices experience thermal stress which provokes wear-out failures and compromises lifetime. In this paper, a model-based dynamic gate voltage control strategy is proposed to reduce the thermal stress by shaping the profile of conduction losses. Thermal stability criteria are investigated, which limit the gate voltage operating range; thus, current focalization and associated local heat up are avoided. After that, simulations and lifetime estimation are conducted for performance evaluation in two different operation scenarios, which show promising results at high speed operation conditions. Furthermore, a current injection method is applied for low-speed operating conditions to improve the compensation effort. This method is experimentally verified by using a custom proof-of-concept gate driver that supplies an adjustable three-level gate voltage. A three-phase electric drive is prototyped, on which power cycling tests are conducted. The junction temperature is measured and the results confirm the thermal control method.

Keywords: power MOSFET modelling; thermal instability; gate voltage control; three-level gate driver; current injection; power cycling

1. Introduction

In aerospace and traction applications, the electric drive system can adopt multi-phase machines and power converters that comprise more power switch devices to achieve fault-tolerant operation [1]. In linear motion control applications, such as the wafer stage of a lithography machine, a multiplicity of power switches is incorporated to meet high efficiency and high precision requirements [2]. Therefore, the lifetime of power switches significantly influences the availability of the power converters.

Failure mechanisms of power switch devices are typically categorized as either catastrophic or aging failures. Catastrophic failures happen in short time periods, which range from micro- to milliseconds. Root causes of such failures are semiconductor-die related abnormal events, which include among others overvoltage, overcurrent, short circuit, unclamped inductive switching and overtemperature [3]. Moreover, single event effects such as cosmic radiation induced failure happens when the device is hit by energetic particles during the off state, and concentrated amounts of charge are deposited which enables current flowing [4]. Furthermore, abnormal events due to instabilities are thoroughly studied in [5], which indicates that the nonuniform distribution of some internal parameters, such as gate resistance and breakdown voltage, can provoke current filament and thermal runaway. Protection schemes such as derating and fault detection methods are applied to improve the system reliability [6]. To the contrary, aging failures take years to happen and root causes

are package related wear-out, such as bond-wire liftoff, heal crack or solder fatigue [7]. These are caused by the mechanical stress between contact materials with different thermal expansion coefficients and local temperature values.

Countermeasures to reduce the thermal stress have been reported in [8] by mitigating the junction temperature swing ΔT_J for lifetime enhancement. The circulation current injection method is well adopted in applications where a fluctuating load profile is required. For instance, an auxiliary-pole topology is proposed in [9] for a reluctance motor drive, where the phase current reduces to zero after commutation, and the power losses of the corresponding switch device are compensated by a circulation current, therefore reducing the power variations and temperature swing.

Active thermal management through the gate drive unit is found to be a promising solution due to its flexible implementation. For instance, a two-step gate driver is introduced in [10] to regulate both the gate signal level and duration, and therefore controlling both the switching and conduction losses. By taking advantage of this scheme, voltage stress during the turn-off transient is reduced. In [11], gate voltage as a control variable is applied to adjust the switching losses to achieve less T_J . In [12], the power MOSFET is operated in the saturation region to dissipate additional losses for further reducing T_J . To dynamically manipulate the switching losses, switching frequency control along with a gate driver that uses switchable gate resistor arrays are proposed in [13], where resistors with a different value are selected according to the virtual junction temperature obtained from a thermal observer. In the above methods, the regulation process is based on a junction temperature feedback controller and therefore compromising control accuracy. A model-based gate voltage control method is proposed in [14,15], which calculates the required gate voltage to smooth the temperature profile by adjusting the conduction losses. However, associated local heat up and current focalization problems are observed in [16], when operating with low gate voltage.

The objective of this paper is to develop a dynamic gate voltage control method for thermal stress reduction of silicon-carbide power MOSFETs. The paper is structured as follows. In Section 2, a compact model is introduced to describe characteristics of the SiC power MOSFET. Section 3 begins by deriving a dynamic gate voltage control strategy to shape the conduction losses of the power MOSFET while conducting low frequency current. After that, thermal stability criteria are investigated to confine the gate voltage range, such that current focalization and associated local heat-up are avoided. In Section 4, the gate control method is adapted to accommodate operations with high frequency current. Section 5 applies the developed methods to the electric drive application, where case studies are conducted based on two different operation scenarios. In addition to that, a circulation current injection method is implemented to improve the compensation efforts, which significantly reduces the junction temperature swing. Lifetime estimation is conducted in Section 6, and the results shows an improvement of the lifetime in these operation scenarios. Section 7 focuses on experimental verification, where a proof-of-concept three-level gate driver and an electric motor drive prototype are realized, on which thermal cycling tests are conducted. The junction temperature is measured, and the results confirm the capability of the proposed thermal control method. At last, conclusions are presented in Section 8.

2. Power MOSFET Model Description

To describe and analyze the power MOSFET characteristics, a physics based analytical model is required. The original 2nd order model is proposed in [17], which performs relatively accurate in the linear region. This model has been improved in [18] to account for the linear behavior of the transfer curve at high current and gate voltage, whereas the electron mobility is reduced as a result of a high transverse electric field. Moreover, to incorporate the effect of carrier diffusion due to nonuniform channel dopant density, separate linear and saturation transconductance with different values are used.

The MOSFET model used in this work adopts the structure proposed in [19,20], which represents the drain current by paralleled channel currents. They are described by the low current I_{mosL} , that is conducted in the corners of MOSFETs cell, and the high current I_{mosH} , that is conducted by the

main portion of the MOSFET cell, respectively. The corner regions of the MOSFET cell have a lower threshold gate voltage and transconductance compared to the main portion, which results in earlier turn-on and lower channel current. The MOSFET drain current I_d is then expressed as

$$I_d = I_{mosL} + I_{mosH}. \quad (1)$$

The detailed expression of the channel currents are represented as follows:
Low current in corner regions:

$$I_{mosL} = \begin{cases} \frac{K_{fl}K_{lin} \left[(V_{gs} - V_{thL})V_{ds} - \frac{P_{vf}^{y-1}V_{ds}^y(V_{gs} - V_{thL})^{2-y}}{y} \right]}{[1 + \theta \times (V_{gs} - V_{thL})]}, & \text{if } V_{ds} \leq V_{pinL}, \\ \frac{K_{fl}K_p(V_{gs} - V_{thL})^2}{2[1 + \theta \times (V_{gs} - V_{thL})]} [1 + \lambda(V_{ds} - V_{pinL})], & \text{if } V_{ds} > V_{pinL}. \end{cases} \quad (2)$$

High current in the main channel:

$$I_{mosH} = \begin{cases} \frac{(1 - K_{fl})K_{lin} \left[(V_{gs} - V_{thH})V_{ds} - \frac{P_{vf}^{y-1}V_{ds}^y(V_{gs} - V_{thH})^{2-y}}{y} \right]}{[1 + \theta \times (V_{gs} - V_{thH})]}, & \text{if } V_{ds} \leq V_{pinH}, \\ \frac{(1 - K_{fl})K_p(V_{gs} - V_{thH})^2}{2[1 + \theta \times (V_{gs} - V_{thH})]} [1 + \lambda(V_{ds} - V_{pinH})], & \text{if } V_{ds} > V_{pinH}. \end{cases} \quad (3)$$

where $V_{pinL} = (V_{gs} - V_{thL})/P_{vf}$, $V_{pinH} = (V_{gs} - V_{thH})/P_{vf}$, and $y = 2K_{lin}/(2K_{lin} - P_{vf} \times K_p)$. And temperature dependent parameters are described as: $K_{lin}(T_J) = K_{lin}(T_0) \times [T_0/T_J]^{K_{lin1}}$, $K_p(T_J) = K_p(T_0) \times [T_0/T_J]^{K_{p1}}$, and $V_{th}(T_J) = V_{th}(T_0) + V_k \times [T_J - T_0]$.

The model is synthesized such that the channel current and its first derivative are continuous at the pinch-off voltage points (i.e., V_{pinL} and V_{pinH}). An additional channel-length modulation parameter λ proposed in [21] is adopted to account for the MOSFET static behavior in the saturation region, which provides a more precise estimation of the switching transient.

The parameter extraction methods have been investigated in [19–21], where the Levenberg–Marquardt (LM) method with a high fitting accuracy is applied in this work. The LM method is a combination of the Gauss–Newton method and Gradient Descent Method, and generally applied for solving nonlinear least square regression problems. This method adaptively varies the parameter update step to approach the local minimum, at which the optimized parameter value is achieved [21–23]. The method is implemented in Matlab and the algorithm is illustrated in Figure 1. The algorithm starts with a given initial parameter set $\mathbf{h}_0$, and calculates the errors $r(\mathbf{h})$ between the measurement data $\mathbf{y}$ and the model $f(\mathbf{h}, \mathbf{X})$. In this case, the vector matrix $\mathbf{y}$ of dimension m represents the measured drain current I_d , the matrix $\mathbf{X}$ represents the input variables (V_{ds} , V_{gs}) and $\mathbf{h}$ are the parameters used in (2) and (3). To find the parameter set $\mathbf{h}$ that minimize the sum of squares of the errors

$$g(\mathbf{h}) = \sum_j^m (y_j - f(\mathbf{h}, x_j))^2, \text{ with row element } y_j \text{ and } x_j \text{ of } \mathbf{y} \text{ and } \mathbf{X}, \quad (4)$$

the LM method calculates the changes of the parameter set $\Delta\mathbf{h}$ iteratively based on the damping factor λ , the jacobian matrix $\mathbf{J}$ and a identity matrix $\mathbf{I}$. The update step is then evaluated and dynamically adapted by varying λ according to $\rho(\Delta\mathbf{h})$ and a user-defined factor ε as illustrated in Figure 1. When the criteria matched, the changes of the parameter set $\Delta\mathbf{h}$ is compared with the step tolerance ε_2 (in

this case $\varepsilon_2 = 10^{-6}$). If $\Delta \mathbf{h} < \varepsilon_2$, the parameter value is optimized, otherwise the algorithm updates $\mathbf{h}$ for next iteration.

Figure 1. Flow chart of the Levenberg–Marquardt fitting algorithm.

By implementing this algorithm, the parameter values are extracted and listed in Table 1.

Table 1. MOSFET model parameters.

Parameter Name	Parameter Symbol	Value at 25 °C	Value at 150 °C
Linear region transconductance (A/V^2)	K_{lin}	1.4318	0.7998
Saturation region transconductance (A/V^2)	K_{p}	1.8106	1.0113
Low current region transconductance factor	K_{fl}	0.2000	0.2000
Transverse electric field parameter (V^{-1})	θ	0.1093	0.1093
Low current MOSFET channel threshold voltage (V)	V_{thL}	2.6000	1.7000
High current MOSFET channel threshold voltage (V)	V_{thH}	8.7369	3.0000
Channel-length modulation parameter (V^{-1})	λ	0.0200	0.0200
Pinch-off voltage factor	P_{vf}	0.7038	0.7038
Pinch-off voltage exponent	y	1.6501	1.9021

The measurement data of the IV-characteristics at 25 °C and 150 °C obtained from the data sheet are used for model fitting. The fitted model and the original data are then illustrated in Figure 2, where the model shows good accuracy compared to the measurement data.

Figure 2. Simulated model and measured IV-characteristics for 1200 V SiC MOSFET at (a) 25 °C and (b) 150 °C.

To quantify the fitting accuracy, discrepancies between the model and measured IV-characteristics at each gate voltage are calculated by finding the root-mean-square deviation (RMSD) with:

$$\text{RMSD} = \frac{\sqrt{\frac{1}{N} \sum_{i=1}^N (x_{i,(mes)} - x_{i,(model)})^2}}{\text{Mean}(x_{i,(mes)})} \times 100\% , \quad (5)$$

and the results are included in Table 2.

Table 2. Discrepancies between the model and measured data.

Gate Voltage V_{gs} (V)	RMSD at 25 °C	RMSD at 150 °C
12	1.84%	1.19%
14	1.33%	1.15%
16	1.02%	0.63%
18	1.98%	1.69%

3. Dynamic Gate Voltage Control with Low Frequency Current

While the frequency ω_o of a sinusoidal load current $I_{load}(t)$ ranges around few tens Hertz, the junction temperature profile follows the shape of power losses, which is determined by the square of the drain current and varies at twice the load frequency. To reduce the junction temperature swing ΔT_J of a power MOSFET, this power loss profile has to be controlled. During on-state, the power losses P_{con} depend on the duty cycle $d(t)$, drain-source voltage V_{ds} and drain current I_d (i.e., $I_d = I_{load}$). Therefore, by adjusting $V_{ds}(t)$ with a proper gate voltage $V_{gs}(t)$ during the conduction stage, fluctuations of P_{con} and the corresponding junction temperature ΔT_J profile caused by a varying load current can be stabilized and minimized. However, because of the thermally unstable behavior of MOSFET under low gate-voltage operation, nonuniform current distribution among MOSFET cells occurs, which provokes current focalization and thermal runaway. In the next paragraphs, the adjustable gate voltage control method and countermeasures to the associated thermal instabilities will be detailed.

3.1. Gate Voltage Derivation

By taking the model accuracy and complexity into account, a simplified Hefner model in [18] is used to derive an analytical expression of the gate voltage. This model can be described by

$$I_d = \begin{cases} \frac{K_{lin} \left[(V_{gs} - V_{th}) V_{ds} - \frac{K_{lin} V_{ds}^2}{2K_p} \right]}{[1 + \theta \times (V_{gs} - V_{th})]}, & \text{if } V_{ds} \leq V_{pin}, \\ \frac{K_p (V_{gs} - V_{th})^2}{2 [1 + \theta \times (V_{gs} - V_{th})]} [1 + \lambda (V_{ds} - V_{pin})], & \text{if } V_{ds} > V_{pin}. \end{cases} \quad (6)$$

with $V_{pin} = (V_{gs} - V_{th}) \times K_p / K_{lin}$, $K_{lin}(T_J) = K_{lin}(T_0) \times [T_0 / T_J]^{K_{lin1}}$, $K_p(T_J) = K_p(T_0) \times [T_0 / T_J]^{K_{p1}}$, and $V_{th}(T_J) = V_{th}(T_0) + V_k \times [T_J - T_0]$.

During the conduction stage, the MOSFET operates in the linear region and therefore the fitting method only takes the linear region data into account to improve the local fitting accuracy. The parameters of both 25 °C and 150 °C are extracted by the LM fitting method, and the results are listed in Table 3. The fitted model and the original data are depicted in Figure 3, where the model shows good accuracy in the linear region and relatively larger discrepancy in the saturation region.

Figure 3. Simulated model and measured IV-characteristics for 1200 V SiC MOSFET at (a) 25 °C, (b) 150 °C, and NTC and PTC areas at (c) gate voltage of 12 V and 14 V, (d) gate voltage of 16 V.

Table 3. MOSFET model parameters.

Parameter Name	Parameter Symbol	Value at 25 °C	Value at 150 °C
Linear region transconductance (A/V ²)	K _{lin}	1.0314	0.5231
Saturation region transconductance (A/V ²)	K _p	1.0869	0.5512
Transverse electric field parameter (V ⁻¹)	θ	0.0563	0.0563
MOSFET channel gate threshold voltage(V)	V _{th}	6.8396	0.5000
channel-length modulation parameter (V ⁻¹)	λ	0.0100	0.0100

It is worth noting that the extracted parameter values in Table 3 might be physically inviable, for instance, the gate threshold voltage V_{th} is too large at 25 °C and close to zero at 150 °C. In spite of this, the gate voltage V_{gs}(t) can be derived based on this model, since discrepancies listed in Table 4 are very small, which shows its capability of providing a precise numerical description.

Table 4. Discrepancies between the model and measured data.

Gate Voltage V _{gs} (V)	25 °C	150 °C
12	5.35%	1.39%
14	2.23%	2.51%
16	1.33%	0.93%
18	1.28%	2.37%

Next, the average conduction losses produced during switching cycle k at period time T_s with duty cycle d(t) are set to a constant P_{const} by

$$\langle P_{con,T_s} \rangle(t) = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} V_{ds} \times I_d dt = V_{ds}(t) \times I_{ds}(t) \times d(t) = P_{const}, \quad (7)$$

with P_{const} = Max [⟨P_{con,T_s}⟩(t)].

The gate voltage V_{gs,T_s}(t) is then obtained by solving the simultaneous equations consisting of (7) and the linear region part of (6), which is indicated by the intersections in Figure 3a,b, yielding

$$V_{gs,T_s}(d(t), I_d(t)) = \left(\frac{K_{lin} P_{const}/d(t)}{2K_p |I_d(t)|} + \frac{I_d(t)^2}{K_{lin} P_{const}/d(t)} \right) / \left(1 - \frac{\theta \times I_d(t)^2}{K_{lin} P_{const}/d(t)} \right) + V_{th}, \quad (8)$$

while |I_d(t)| > I_{min}(t), and I_{min}(t) = $\left[\frac{(K_{lin} P_{const}/d(t))^2}{2K_p} \right]^{\frac{1}{3}}$.

However, the simultaneous equations have no solution when |I_d(t)| ≤ I_{min}(t), and the corresponding pinch-off voltage V_{pin}(I_d(t)) can be applied to maximize the compensation efforts [12]. By solving the simultaneous equations consisting of (7) and the saturation region part of (6), V_{pin}(I_d(t)) is expressed as

$$V_{pin}(I_d(t)) = \frac{|I_d(t)| \times \theta + \sqrt{(I_d(t) \times \theta)^2 + 2K_p |I_d(t)|}}{K_p} + V_{th}, \quad (9)$$

3.2. Thermal Stability Criteria

By observing Figure 3a,b, a relatively high drain-source voltage V_{ds} is required while the drain current I_d is low to achieve constant conduction losses. However, operating in such a condition might trigger secondary breakdown, which commonly occurs in the minority carrier devices like BJTs. Because the minority carrier density is proportional to the intrinsic carrier density, which possesses a positive temperature coefficient (PTC) property. For majority carrier devices, like MOSFETs are generally immune from this issue [24].

Despite this, failures are observed from the last generation power MOSFET devices while operating with low gate voltage. In [16], test results of a trench power MOSFET reveal its thermal instability while operating in the saturation region (i.e., linear mode). As a result of the high transconductance and negative temperature coefficient (NTC) property of gate threshold voltage (i.e., $dV_{th}/dT_J < 0$), MOSFET channel resistance has a NTC property (i.e., $dI_d/dT_J > 0$) at low gate voltage and low current level, which provokes current focalization and thermal runaway [25–27].

Thermal stability criteria has been usually investigated, whereas large scale integration (LSI) MOSFETs are studied at high temperature concerning their temperature dependent parameters and the corresponding thermal instability [28,29]. In addition, power MOSFETs operate in the saturation region as a constant current source is studied in [30]. A so-called temperature compensation point (TCP) is defined as the intersection of the transfer curve at different junction temperatures, on which $dI_d/dT_J = 0$. Above the TCP, the MOSFET current has a negative dI_d/dT_J . In other words, the MOSFET saturation current decreases at higher junction temperature, which balances the current among MOSFET cells. On the contrary, if operating the MOSFETs below the TCP with a low gate voltage, inhomogeneous current distribution occurs and the cooling capability should be enhanced to prevent thermal runaway.

However, in order to achieve high power processing efficiency, for instance in motor drive applications, power MOSFETs operate in the linear region during conduction stage, yet previous little work has been devoted to thermal stability in this region. In this work, the gate voltage is decreased or increased according to the drain current to achieve constant conduction losses. Therefore, the operation range should be constrained to the positive temperature coefficient (PTC) areas, which is illustrated in Figure 3c,d. On each IV-characteristic curve of different gate voltage, the TCP that separates the NTC and PTC areas is defined as the thermally stable boundary condition. The gate voltage $V_{gs,TCP}$ at the TCP is derived by setting the linear region current of (6) as follows

$$\frac{dI_d}{dT_J} = 0. \quad (10)$$

which gives:

$$\frac{K_{lin}}{2K_{sat}} V_{ds} = (V_{gs,TCP} - V_{th}) - \left[n + \frac{\theta}{1 + \theta \times (V_{gs,TCP} - V_{th})} \right]^{-1}. \quad (11)$$

Moreover, by complying to (11), thermal instabilities cannot be fully eliminated as parameter drifting occurs in the manufacturing stage and aging process, which causes model inaccuracy. Therefore, to improve the system robustness, operation margins are incorporated in the gate voltage derivation process (A1) in Appendix A, which gives

$$V_{gs,TCP}(I_d(t)) = \left(\frac{n|I_d(t)|}{2K_p} + \frac{1}{n} \right) / \left(1 - \frac{\theta n|I_d(t)|}{2K_p} \right) + V_{th}, \quad (12)$$

where $n = \frac{1}{K_{lin}} \times \left| \frac{dK_{lin}}{dT_J} \right| \times \left| \frac{dV_{th}}{dT_J} \right|^{-1}$.

Therefore, to operate in the PTC area, the dynamic gate voltage $V_{gs}(t)$ has to be larger than (12), and synthesized by taking the larger one of (8) and (12) as

$$V_{gs}(t) = \begin{cases} \text{Max} [V_{gs,Ts}, V_{gs,TCP}], & \text{if } |I_d(t)| > I_{min}(t), \\ V_{gs,TCP}, & \text{if } |I_d(t)| \leq I_{min}(t), \end{cases} \quad (13)$$

because $V_{gs,TCP}(I_d(t)) \geq V_{pin}(I_d(t))$ always holds while $|I_d(t)| \leq I_{min}(t)$.

It is claimed in [5], that instabilities are hard to avoid by using protection circuits because there is no clear external evidence when they occur. As proposed in [31], online temperature monitoring via an embedded thermal sensor that using a PN junction of the power MOSFETs could be a possibility to

counteract thermal runaway, however by properly constraining the gate voltage as discussed above, thermal runaway will not occur in the first place.

4. Dynamic Gate Voltage Control with High Frequency Current

When a motor drive operates at high speed (generally between a few hundreds to thousand Hertz), the junction temperature T_j is determined by the load profile I_L instead of the instantaneous current, since the phase current frequency then becomes significantly higher than the thermal cut-off frequency of T_j . In the next paragraphs, the gate voltage control method is modified to accommodate such high speed operation scenario.

By applying a sinusoidal load current $I_{load}(t)$ at a frequency of ω_o , with the duty cycle $d(t)$ that is modulated with index d and d_3 for the 1st the 3rd order harmonic, respectively. The RMS current in a load cycle T_L can be derived as

$$I_{d,rms,T_L}(t) = \sqrt{\frac{1}{T_L} \int_{kT_L}^{(k+1)T_L} I_{load}(t)^2 \times d(t) dt} = \frac{I_L(t)}{2}, \text{ whereas } I_{load}(t) = I_L(t) \times \cos(\omega_o t), \quad (14)$$

and the duty cycle $d(t) = \frac{d}{2} \cos(\omega_o t + \phi_{load}) + \frac{d_3}{2} \cos(3\omega_o t + 3\phi_{load}) + \frac{1}{2}$, with load angle ϕ_{load} .

By following the method developed in Section 3, the conduction loss produced in each load cycle T_L is set to a constant by

$$\langle P_{con,T_L} \rangle(t) = \frac{1}{T_L} \int_{kT_L}^{(k+1)T_L} V_{ds} \times I_d dt = V_{ds,rms,T_L}(t) \times I_{d,rms,T_L}(t) = P_{const}, \quad (15)$$

with $P_{const} = \text{Max} [\langle P_{con,T_L} \rangle(t)]$.

Similar to (8), the gate voltage $V_{gs,T_L}(t)$ is then found to be

$$V_{gs,T_L}(I_L(t)) = \left(\frac{K_{lin}}{K_p} \times \frac{P_{const}}{I_L(t)} + \frac{I_L(t)^2}{4K_{lin} \times P_{const}} \right) / \left(1 - \frac{\theta \times I_L(t)^2}{4K_{lin} \times P_{const}} \right) + V_{th}, \quad (16)$$

while $\frac{I_L(t)}{2} > I_{min}(t)$, and $I_{min}(t) = \left[\frac{(K_{lin} \times P_{const})^2}{2K_p} \right]^{\frac{1}{3}}$.

To operate the power MOSFETs in the PTC area, the gate voltage has to be larger than (12), and therefore by combining with (16), it can be synthesized as:

$$V_{gs}(t) = \begin{cases} \text{Max} [V_{gs,T_L}(I_L(t)), V_{gs,TCP}(I_L(t))] , & \text{if } I_L(t) > 2I_{min}(t), \\ V_{gs,TCP}(I_L(t)), & \text{if } I_L(t) \leq 2I_{min}(t), \end{cases} \quad (17)$$

where $V_{gs,TCP}(I_L(t)) = \left(\frac{nI_L(t)}{2K_p} + \frac{1}{n} \right) / \left(1 - \frac{\theta n I_L(t)}{2K_p} \right) + V_{th}$, and $V_{gs,TCP}(I_L(t)) \geq V_{gs,TCP}(I_d(t))$ always holds.

5. Electric Motor Drive Application

In this section, load-profile based system-operation principles and the associated dynamic gate-voltage control methods are introduced. In the next paragraphs, case studies and simulations are conducted to evaluate the system performance. Moreover, to enhance the compensation efforts at low speed, a circulation current injection method is developed.

5.1. Electro-Thermal Model

To verify the proposed gate voltage control method, an electro-thermal model (ETM) of the power MOSFET is built up and illustrated in Figure 4. According to (1), the ETM encompasses two voltage dependent current sources, which represent the low current I_{mosL} and high current I_{mosH} . The power switch contains three parasitic nonlinear capacitors C_{gd} , C_{gs} and C_{ds} respectively, which depend on the drain-source voltage V_{ds} [32]. The dependency is described by look-up tables. The equivalent thermal network is simulated with a third order network, where parameters are obtained from data sheets.

Figure 4. Equivalent electro-thermal model based on an 1200 V SiC power MOSFET with TO-247 package.

5.2. Case 1: Electric Drive of Rotating Machine under High Speed Operation

In a high speed operation scenario, simulations are conducted by using PLECS in the Matlab Simulink environment with a load condition of 200 Hz and varying amplitude $I_L(t)$. It can be observed from (17) that after measuring the load current $I_L(t)$ (i.e., phase current), the gate voltage control scheme can be readily applied to each power MOSFETs in an electric motor drive. Instead of a conventional gate driver that produces two-level pulses, a dynamic gate driver is proposed to generate a three-level gate signal. This gate signal starts with a high voltage stage (18 V for this case) for a fast switching performance, followed by the adjustable gate voltage $V_{gs}(t)$ during the conduction stage to adjust the conduction losses. In Figure 5, the system operation principle shows that its implementation can be readily realized by merely integrating three dynamic gate drivers. Other aspects, such as the power converter topology, modulation method, and control scheme (i.e., field-oriented-control in this case) will not be affected.

Figure 5. Operation principle of the gate voltage control in the electric motor drive application.

By observation of Figure 6a, the dynamic gate voltage $V_{gs}(t)$ of switch Cu, as obtained from (17), follows the envelope of load current and is always higher than the required level $V_{gs,TCP}(I_{loadC}(t))$ to operate the switch Cu in the PTC area. After that, the corresponding junction temperature response of switch Cu is then obtained from the electro-thermal model in Figure 4. Simulations with a conventional two-level gate signal under the same load conditions are conducted to obtain the junction temperature for reference. Temperature swings ΔT_J at different load transitions are depicted in Figure 6b, and the values are listed in Table 5. The power losses increase slightly as expected, however, the overall system efficiency is merely affected while operating with high output power (i.e., 4262 W in this case).

Table 5. Performance evaluation at high speed operation with 10 kHz switching frequency.

	ΔT_J (K) 30A $\rightarrow$ 20A	ΔT_J (K) 30A $\rightarrow$ 15A	ΔT_J (K) 30A $\rightarrow$ 10A	Power Losses per Switch (W)	Output Power (W)	Efficiency (%)
$V_{gs}(t) = 18$ V	34.9	45.4	51.4	24.4	4262	98.3
$V_{gs}(t)$ in (17)	21.4	37.4	49.2	27.4	4262	98.1

Figure 7. System operation principle of a motor driver consisting of six half-bridge legs.

Figure 8. Simulation results of (a) Gate voltage profile and load current of phase C, (b) Conduction losses P_{ref} of switch Cu with conventional 18 V two-level gate signal, (c) Conduction losses P_{dyn} of switch Cu with the adjustable three-level gate signal, and (d) Junction temperature response under low speed operation condition.

By observation of Figure 8a, part of $V_{gs}(t)$ is clipped to the value of $V_{gs,TCP}$ to avoid entering the NTC region. The conduction losses are illustrated in Figure 8b,c. It can be observed that, by adopting the three-level gate signal, the conduction losses profile P_{dyn} is raised and flattened compared to P_{ref} , where the conventional two-level gate signal pulse are applied. As shown in Figure 8d and Table 6, the junction temperature response $T_{J,dyn}$ indicate similar ΔT_J but higher average temperature $T_{J,avg}$ with respect to $T_{J,ref}$. There are two reasons behind this behavior: on one hand, the thermal capacitance of the chip die is quite small and therefore temperature drops immediately while power losses become lower; on the other hand, gate voltage is not allowed to be lower than $V_{gs,TCP}$ and the thermal compensation efforts are largely reduced as a consequence. It worth noting that, while $V_{gs}(t) = 18$ V, the system efficiency drops to 88.8% compared to 97.6% in Table 5 obtained at high speed operating condition. This is due to relatively small back-emf at low speed and consequently lower output power.

Table 6. Performance evaluation at low speed operation with 10 kHz switching frequency.

	ΔT_{J1} (K)	ΔT_{J2} (K)	$T_{J,avg}$ (K)	Power Losses per Switch (W)	Output Power (W)	Efficiency (%)
$V_{gs}(t) = 18$ V	18.4	22.8	325.9	20.7	984	88.8
$V_{gs}(t)$ in (13)	23.3	23.3	314.2	29.8	984	84.6

To improve the compensation efforts under low speed operation, the proposed motor drive containing six half-bridge legs and interconnected inductors is implemented in Figure 9.

Figure 9. System operation principle of the circulation current injection method.

Two interconnected inductors are used to circulate high frequency current between two half-bridge legs. The circulation current frequency ω_{cir} should be above 20 times of the load current frequency ω_o for sufficient compensation resolution. The circulation currents flow within the power converter itself and are not influencing the three-phase load current. Therefore, the inductor currents of phase C can be expressed as

$$\begin{aligned} I_{L\delta5}(t) &= I(t) + I_{cir}(t) \times \cos(\omega_{cir}t), \\ I_{L\delta6}(t) &= I(t) - I_{cir}(t) \times \cos(\omega_{cir}t), \end{aligned} \quad (18)$$

$$\text{where } I(t) = \frac{1}{2} I_{loadC}(t) = I_l(t) \times \cos(\omega_o t), \text{ and } I_l(t) = \frac{1}{2} I_L(t).$$

By following Equation (18), the inductor currents of other phases can be described similarly. To regulate the three-phase load current in a dq synchronously rotating reference frame [33], a PI controller and space-vector modulation are adopted. For controlling the circulation current, a proportional-resonant (PR) controller with a resonant frequency ω_{cir} (i.e., 8 kHz in this case) is applied in the stationary reference frame [34] as:

$$H(s) = K_P + \frac{K_R s}{s^2 + \omega_{cir}^2}. \quad (19)$$

While conducting the circulation current, the drain current equals to the corresponding inductor current, and the RMS value of the drain current $I_{d,rms,T_j}(t)$ of the switch Cu in each circulation current period T_j can be represented as

$$I_{d,rms,T_j}(t) = \sqrt{\frac{1}{T_j} \int_{kT_j}^{(k+1)T_j} I_{L\delta5}(t)^2 \cdot D_{cu}(t) dt} = \sqrt{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}} \cdot \sqrt{d(t)}, \quad (20)$$

where as the duty cycle $D_{cu}(t) = d(t) + (L \times \omega_{cir} \times I_{cir}(t) \times \cos(\omega_{cir}t + \pi/2)) / (2V_{dc})$.

Similar to (7), the conduction losses produced during each circulation current period T_j are set to a constant P_{const} by

$$\langle P_{con,T_L} \rangle(t) = \frac{1}{T_j} \int_{kT_j}^{(k+1)T_j} V_{ds} \times I_d dt = \frac{V_{ds,rms,T_j}(t)}{\sqrt{d(t)}} \times \frac{I_{d,rms,T_j}(t)}{\sqrt{d(t)}} \times d(t) = P_{const}, \quad (21)$$

with $P_{const} = \text{Max}[\langle P_{con,T_L} \rangle(t)]$.

The gate voltage $V_{gs}(t)$ is then found to be

$$V_{gs}(t) = \left(\frac{K_{lin}}{2K_{sat}} \frac{P_{const}/d(t)}{\sqrt{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}} + \frac{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}{K_{lin} \times P_{const}/d(t)} \right) / \left(1 - \frac{\theta \times \left(I_l(t)^2 + \frac{I_{cir}(t)^2}{2} \right)}{K_{lin} \times P_{const}/d(t)} \right) + V_{th}. \quad (22)$$

In order to operate the power MOSFETs in the PTC area, the gate voltage has to suffice

$$V_{gs}(t) \geq V_{gs,TCP}(I_d(t)). \quad (23)$$

Following the derivation steps from (A2)–(A4) in Appendix A, the minimum circulation current amplitude $I_{cir}(t)$ has to satisfy

$$I_{cir}(t) \geq \left(\frac{n}{2K_p} + \sqrt{\left(\frac{n}{2K_p} \right)^2 - \frac{2d(t)}{K_{lin} \times P_{const}} \left(\frac{I(t)^2 d(t)}{K_{lin} \times P_{const}} - \frac{n|I(t)|}{2K_p} - \frac{1}{n} \right)} \right) \times \frac{K_{lin} \times P_{const}}{d(t)}. \quad (24)$$

In addition, by following the steps from (20) to (24), the circulation currents of other phases and gate voltages of the rest of switches can be derived similarly. By using the control scheme in Figure 9, simulations are conducted with load current of 45 A, 10.4 Hz and results are illustrated in Figure 10.

Figure 10. Simulation results of (a) inductor current of phase C, (b) Dynamic gate voltage profile, (c) Conduction losses and (d) Junction temperature response with circulation current injection method of the switch Cu.

Figure 10a shows the inductor current $I_{L\delta 5}$ of phase C, which consists of half of the load current with frequency of 10.4 Hz and the circulation current with a frequency of 8 kHz. Therefore, a higher switching frequency (40 kHz in this case) is required to regulate the circulation current and thus producing more switching losses. The gate voltage $V_{gs}(t)$ obtained from (22) is depicted in Figure 10b, which suffices the requirement of (23) to operate the power MOSFET in the PTC area. As shown in Figure 10c, by applying $V_{gs}(t)$, the conduction losses profile $P_{cir+dyn}$ is flattened compared to P_{cir} , in the interval where no circulation occurs. The junction temperature responses are compared in Figure 10d, and details are listed in Table 7. It can be observed that, the junction temperature swing is significantly reduced down to 4.2 K by compromising the system efficiency, which results from higher losses due to the circulation current and higher switching frequency. In addition to that, low output power at low speed operation is another factor that reduces the system efficiency. Therefore, the thermal stress related failures will be avoided and lifetime is expected to increase. It is worth noting that this current injection method is only specified for applications with large current variation and consequently higher ΔT_J , and critical requirement on the lifetime, such that efficiency can be compromised.

Table 7. Performance evaluation at low speed operation with 40 kHz switching frequency and 8 kHz circulation current.

	ΔT_{J1} (K)	ΔT_{J2} (K)	T_{Javg} (K)	Power Losses per Switch (W)	Output Power (W)	Efficiency (%)
$V_{gs}(t) = 18 \text{ V} + \text{Circulation current}$	13.5	14.3	356.6	42.2	984	79.5
$V_{gs}(t)$ in (22) + Circulation current	0.8	4.2	364.1	47.7	984	77.5

It is worth noting that, the gate voltage is calculated based on the obtained MOSFET parameters in Table 3, which are fitted from the data-sheet. In other words, open-loop junction temperature control is applied by adjusting the gate voltage. As an inherent property of the loop-open controller, the controller output (i.e., V_{gs}) will be influenced in case of device parameter drifts. Therefore, a model-based closed-loop temperature control is recommended by adding a real-time temperature observer to improve the system performance. In terms of the controller safety robustness, thermal runaway is avoided by incorporating operation margins in (A1), (A3) and (A4) in Appendix A, which ensures the PTC operation of the power MOSFETs.

6. Lifetime Estimation

Lifetime considering thermal stress is generally estimated based on the linear damage accumulation principle [35]. If the same failure mechanism is shared within a full thermal stress profile, all stress levels can be added up to calculate the total accumulated damage (AD) as:

$$AD = \sum_{i=1}^k \frac{n_i}{N_{fi}} = \frac{n_1}{N_{f1}} + \frac{n_2}{N_{f2}} + \frac{n_3}{N_{f3}} \cdots + \frac{n_k}{N_{fk}}. \quad (25)$$

where N_{fi} represents the number of cycles to failure at stress ΔT_{Ji} , and n_i is the number of cycles accumulated at this stress level. The end of life can be expected when AD reaches one. The number of cycles to failure N_f under a certain stress can be estimated by an empirical equation

$$N_f = A_c \Delta T_J^\alpha \exp(E_a / k_B T_{Javg});$$

where

$$\begin{aligned} \text{Activation energy } E_a &= 9.89 \times 10^{-20} \text{ J}, \\ \text{Boltzmann-constant } k_B &= 1.38 \times 10^{-23} \text{ J} \times \text{K}^{-1}, \\ A_c &= (650,790 \text{ K})^{-\alpha}, \text{ and } \alpha = -4.67. \end{aligned} \quad (26)$$

The parameters are obtained from [36] by testing the DCB based transfer molded TO-247 package. It is worth noting that the parameters are fitted for a temperature swing ΔT_J that is larger than 110 K, which exceeds the simulated value of ΔT_J in our case. Despite this, to compare the system performance with different compensation methods, a rough lifetime estimation based on these parameters is still highly meaningful. When using different package technologies, the value of α or A_c changes, however, similar results can be expected if the empirical model in (26) holds.

By analyzing the simulation results obtained from the above cases, a lifetime estimation is conducted of which the results are listed in Tables 8 and 9. The lifetime is improved by a factor of four while operating in the above high speed case by using the gate voltage control method, and more than 10^5 times while adopting both the circulation current injection and gate voltage control method in the low speed case. In [37], power cycling tests of IGBT transistors indicate that the lifetime can strongly increase while ΔT_J becomes very small, that meaning (26) does not agree with measurement results. This is because the thermomechanical stress will mainly cause reversible elastic deformation at low ΔT_J , and in that case the absolute temperature has a large impact on the lifetime. Therefore, the lifetime estimation of the last case in Table 9 can be inaccurate, however with negligible ΔT_J , the thermal stress related number of cycle to failures are expected to be significantly increased.

Table 8. Lifetime estimation and system efficiency for case 1.

	$\Delta T_{J1}(\text{K}), T_{Javg1}(\text{K})$	$\Delta T_{J2}(\text{K}), T_{Javg1}(\text{K})$	$\Delta T_{J3}(\text{K}), T_{Javg1}(\text{K})$	Efficiency (%)	Lifetime N_f
$V_{gs}(t) = 18 \text{ V}$	34.9, 337.4	45.4, 332.2	51.4, 329.2	98.3	3.8×10^7
$V_{gs}(t)$ in (17)	21.4, 344.2	37.4, 336.2	49.2, 330.3	98.1	1.7×10^8

Table 9. Lifetime estimation and system efficiency for case 2.

	$\Delta T_{J1}(\text{K})$	$\Delta T_{J2}(\text{K})$	$T_{Javg}(\text{K})$	Efficiency (%)	Lifetime N_f
$V_{gs}(t) = 18 \text{ V}$	18.4	22.8	325.9	88.8	1.95×10^9
$V_{gs}(t)$ in (13)	23.3	23.3	336.9	84.6	4.63×10^8
$V_{gs}(t) = 18 \text{ V} + \text{Circulation current}$	13.5	14.3	356.6	79.5	1.61×10^9
$V_{gs}(t)$ in (22) + Circulation current	0.8	4.2	364.1	77.5	3.26×10^{14}

7. Experimental Verification

In Figures 11 and 12a, a proof-of-concept for a three-level gate driver is shown. It is operated to trigger the power MOSFET with a switching frequency f_s of 10 kHz. The gate signal is generated by first activating the turn-on FET to produce a short high voltage V_h stage (+18 V for 1.2 μs in this case) for fast switching, thus avoiding extra voltage harmonic distortions on the load side. The voltage V_h is selected to has a reasonable large amplitude depends on the MOSFET type, which enables fast switching and not destroying the gate. To accommodate higher f_s , the width of the +18 V stage can be adjusted and its duration should be at least longer than the minimum required switching-on time. During the on-state, the power op-amp is enabled to adjust the gate voltage level to $V_{gs}(t)$ for controlling the conduction losses. The conduction stage duration t_{cond} of the gate signal is expressed by $t_{cond} = d(t)/f_s - 1.2 \mu\text{s}$. At last, the turn-off FET with a lower gate resistance is switched on for switching off the power MOSFET.

A saturation detection scheme is developed, which monitors the on-state drain-source voltage drop to guarantee a safe operation of the transistor. A protection circuit is implemented, which compares the drain-source voltage with two different voltage levels. When V_{ds} is higher than the low level, the gate voltage will be switched back to +18 V to prevent saturation, such that no hard stops would occur, and when cross conduction happens, the power MOSFET will be switched off by Soff for short circuit or over current protection.

Figure 11. Three-level dynamic gate driver schematics.

Figure 12. (a) Gate driver board and (b) Three-phase electric motor drive setup.

To conduct the power cycling test, a 3 kW electric motor drive presented in Figure 12b is built up, where the phase current and gate voltage regulation algorithms are implemented by using the Arduino DUE controller. The on-state drain-source voltage $V_{ds,on}$ is measured by a voltage clamping circuit, and it can be observed from Figure 13a,b that, $V_{ds,on}$ increases from 0.6 V to 1 V when reducing the gate voltage from 18 V to 13 V. As a temperature sensitive electric parameter (TSEP), a look-up table in Figure 13c, which contains the on-state resistance $R_{ds,on}(18\text{ V})$ measured under 18 V gate voltage is used for the junction temperature estimation. In order to acquire $R_{ds,on}(18\text{ V})$, a periodical 18 V gate signal illustrated in Figure 13a is produced for every 1 ms to measure the $V_{ds,on}$. At the center of the 18 V gate signal, a trigger signal is generated by the controller to initiate the logging function of the oscilloscope. After that, the electric motor drive is driven by a 50 Hz three-phase current with a load profile $I_L(t)$ as depicted in Figure 13d for power cycling. The gate voltage profile $V_{gs}(t)$ is then regulated based on $I_L(t)$, with its amplitude changes from 18 V to 13 V. Junction temperature is estimated at last, which shows a reduction of 34.3% of the temperature swing by applying the proposed method.

Figure 13. (a) V_{ds} response of the three-level gate signal, (b) V_{ds} response of the three-level gate signal zoom in view, (c) Look-up table for junction temperature T_J estimation, and (d) Load profile and temperature profile during power cycling test.

8. Conclusions

In this paper, an extensive analytical power MOSFET model and the corresponding parameter extraction methods are introduced. Based on the presented model, a method is proposed to dynamically adjust the conduction losses for thermal stress reduction and lifetime enhancement of the power MOSFETs, by a novel dynamic gate driver. After that, thermal stability criteria are investigated to confine the gate voltage range, such that current focalization and the associated local heat up problems are prevented. The system performance and lifetime estimation are evaluated under different operation scenarios of an electric motor drive, which suggests an improvement of lifetime with a factor of four by hardly compromising the system efficiency at the high speed case. In addition, for applications that have a critical requirement on the lifetime, a circulation current injection method is applied to enhance the compensation efforts at low speed operation case, which significantly reduces the junction temperature swing down to 4.2 K. For experimental verification, a dynamic gate driver that supplies an adjustable gate voltage is realized. At last, power cycling tests are conducted on a three-phase electric motor drive prototype and the results show a reduction of 34.3% of the temperature swing, which confirms the thermal control method.

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Appendix A

Appendix A.1 Gate Voltage Derivation at TCP

The gate voltage at TCP is derived by setting the derivative of the linear region current in (6) over temperature to zero.

$$\frac{dI_d}{dT_J} = 0,$$

$$\text{which gives } \frac{K_{lin}}{2K_{sat}} V_{ds} = (V_{gs,TCP} - V_{th}) - \left[n + \frac{\theta}{1 + \theta \times (V_{gs,TCP} - V_{th})} \right]^{-1},$$

To improve the system robustness, operation margins are added as follows:

$$\frac{K_{lin}}{2K_{sat}} V_{ds} \leq (V_{gs,TCP} - V_{th}) - n^{-1} \leq (V_{gs,TCP} - V_{th}) - \left[n + \frac{\theta}{1 + \theta \times (V_{gs,TCP} - V_{th})} \right]^{-1},$$

By reforming the equation of the linear region current in (6), V_{ds} is expressed as:

$$V_{ds} = \frac{1}{C} (V_{gs,TCP} - V_{th}) - \sqrt{\frac{1}{C^2} (V_{gs,TCP} - V_{th})^2 - \frac{2I_d}{CK_{trvlin}}}, \text{ whereas } (V_{gs,TCP} - V_{th})^2 \geq \frac{2CI_d}{K_{trvlin}}$$

$$\text{with } C = \frac{K_{lin}}{K_p} \text{ and } K_{trvlin} = \frac{K_{lin}}{1 + \theta \cdot (V_{gs} - V_{th})}.$$

By plugging the V_{ds} expression into the above inequality, we have:

$$\sqrt{(V_{gs,TCP} - V_{th})^2 - \frac{2CI_d}{K_{trvlin}}} \geq -(V_{gs,TCP} - V_{th}) + \frac{2}{n}.$$

Finally, the gate voltage at TCP is derived as:

$$V_{gs,TCP}(I_d(t)) = \left(\frac{n|I_d(t)|}{2K_p} + \frac{1}{n} \right) / \left(1 - \frac{\theta n|I_d(t)|}{2K_p} \right) + V_{th} \text{ with } n = \frac{1}{K_{lin}} \times \left| \frac{dK_{lin}}{dT_J} \right| \times \left| \frac{dV_{th}}{dT_J} \right|^{-1}. \quad (A1)$$

Appendix A.2 Derivation of the Amplitude of Circulation Current

The minimum circulation current amplitude $I_{cir}(t)$ has to satisfy (23), and equivalently:

$$\left(\frac{K_{lin}}{2K_{sat}} \frac{P_{const}/d(t)}{\sqrt{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}} + \frac{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}{K_{lin} \times P_{const}/d(t)} \right) / \left(1 - \frac{\theta \times \left(I_l(t)^2 + \frac{I_{cir}(t)^2}{2} \right)}{K_{lin} \times P_{const}/d(t)} \right) \geq \left(\frac{n|I_d(t)|}{2K_p} + \frac{1}{n} \right) / \left(1 - \frac{\theta n|I_d(t)|}{2K_p} \right) \quad (A2)$$

To satisfy the above inequality, two conditions are required.

Condition one:

$$\frac{\theta \cdot \left(I_l(t)^2 + \frac{I_{cir}(t)^2}{2} \right)}{K_{lin} \cdot P_{const}/d(t)} \geq \frac{\theta n |I_d(t)|}{2K_p}, \text{ whereas}$$

$$I_d(t) = I(t) + I_{cir}(t) \times \cos(\omega_{cir}t) \text{ with } I(t) = I_l(t) \times \cos(\omega_0t).$$

By adding operation margins, it becomes:

$$\frac{\theta \cdot \left(I_l(t)^2 + \frac{I_{cir}(t)^2}{2} \right)}{K_{lin} \times P_{const}/d(t)} \geq \frac{\theta n (|I_{cir}(t)| + |I_l(t)|)}{2K_p}, \text{ and therefore,} \quad (A3)$$

$$I_{cir}(t) \geq$$

$$\left(\frac{n}{2K_p} + \sqrt{\left(\frac{n}{2K_p} \right)^2 - \frac{2d(t)}{K_{lin} \times P_{const}} \left(\frac{I(t)^2 d(t)}{K_{lin} \times P_{const}} - \frac{n |I(t)|}{2K_p} \right)} \right) \times \frac{K_{lin} \times P_{const}}{d(t)}.$$

Condition two:

$$\frac{K_{lin}}{2K_{sat}} \frac{P_{const}/d(t)}{\sqrt{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}} + \frac{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}{K_{lin} \times P_{const}/d(t)} \geq \frac{n |I_d(t)|}{2K_p} + \frac{1}{n}$$

By adding operation margins, it requires:

$$\frac{I_l(t)^2 + \frac{I_{cir}(t)^2}{2}}{K_{lin} \times P_{const}/d(t)} \geq \frac{n (|I_{cir}(t)| + |I_l(t)|)}{2K_p} + \frac{1}{n}, \text{ and therefore,} \quad (A4)$$

$$I_{cir}(t) \geq$$

$$\left(\frac{n}{2K_p} + \sqrt{\left(\frac{n}{2K_p} \right)^2 - \frac{2d(t)}{K_{lin} \times P_{const}} \left(\frac{I(t)^2 d(t)}{K_{lin} \times P_{const}} - \frac{n |I(t)|}{2K_p} - \frac{1}{n} \right)} \right) \times \frac{K_{lin} \times P_{const}}{d(t)}.$$

By comparing these two conditions, conclusion is made that (23) is met while condition two is satisfied.

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