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Subthreshold Characteristics of AlGaN/GaN MIS-FinFETs with Controlling Threshold Voltages

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Abstract: AlGaN/GaN metal-insulator-semiconductor field-effect transistors with fin structures (AlGaN/GaN MIS-FinFETs) were fabricated and characterized by changing fin width and using different dielectric layers. The FinFET with 20 nm-thick SiO_2 dielectric layer exhibits a very small subthreshold swing (SS) of 56 mV/decade. However, the threshold voltage of the device is too low to ensure low off-state leakage current (at the gate voltage of 0 V), even though the fin width of the device is reduced to 30 nm, which would not meet the requirement for low standby power consumption. On the other hand, the FinFET with a 10 nm-thick Al_2O_3 dielectric layer and a much wider fin width of 100 nm shows normally-off operation with a threshold voltage of 0.8 V, SS of 63 mV/dec, and very low off-state current of 1 nA/mm. When the fin width is reduced to 40 nm, the threshold voltage of the FinFET is increased to 2.3 V and the SS is decreased to 52 mV/decade. These excellent switching performances convince us that the FinFETs might be promising either for low voltage logic or for efficient power switching applications. The observed SS values, which are smaller than the theoretical Boltzmann limit (60 mV/decade), can be explained by the concept of the voltage-dependent effective channel width.

Keywords: AlGaN/GaN; FinFET; Sub-60 mV/decade

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1. Introduction

AlGaN/GaN-based high electron mobility transistors (HEMTs) are very promising for high power and high-frequency applications due to their wide bandgap, large critical electric field, and high saturation velocity [1–4]. Recently, AlGaN/GaN metal-insulator-semiconductor field-effect transistors with fin structures (MIS-FinFETs) have been widely investigated to achieve better gate controllability and higher device linearity, compared with conventional planar HEMTs, which results in a great reduction of off-state leakage current (I_{OFF}), suppression of drain induced barrier lowering (DIBL), and improvement of subthreshold swing (SS) [5–10]. It is worth noting that the threshold voltage (V_{TH}) of the MIS-FinFET increases as the fin width (W_{fin}) decreases due to the lateral depletion of 2-dimensional electron gas (2DEG) channel by sidewall gate and eventually the device can show a normally-off operation when the W_{fin} is reduced to a few tenths of a nanometer [11,12], without adapting additional process methods, such as recessed gate, P-GaN gate, thin AlGaN barrier layer, and cascode structure, usually applied to conventional planar HEMTs [13–16].

Our previous work demonstrated that AlGaN/GaN MIS-FinFETs with W_{fin} of around 30 nm can show not only normally-off operation, but also extremely low I_{OFF} as well as small SS (smaller than theoretical Boltzmann limit of < 60 mV/decade) [17]. These excellent performances of the AlGaN/GaN MIS-FinFETs suggest that the GaN-based materials, combined with novel nano-structure such as fin or nanowire, can offer an opportunity for a new possible low power logic device application [18–20], in addition to conventional efficient power switching device application which requires a relatively large positive V_{TH} to ensure safe device operation as well as low standby power consumption. For low-power logic applications, however, it is better to keep the V_{TH} of the device low as long as the off-state leakage current (I_{OFF}; at gate voltage, V_G = 0 V) is low, which can be achieved with very steep SS.

In this work, two different AlGaN/GaN MIS-FinFETs with either 20 nm-thick SiO_2 or 10 nm-thick Al_2O_3 dielectric layers were characterized to investigate the effects of the fixed oxide charge and the surface trap at the GaN/dielectric interface on the device performances with varying the W_{fin}. In addition, the MIS-FinFETs with different sidewall planes, either steep m-plane or sloped plane (12° off-angle to m-plane), were also characterized for the same purpose.

2. Device Fabrication

Epitaxial layers of 2 µm-thick highly resistive undoped GaN, 50 nm-thick GaN channel layer and 25 nm-thick $Al_{0.25}Ga_{0.75}N$ barriers were sequentially grown on the sapphire substrate by using metal-organic chemical vapor deposition (MOCVD). The 2DEG density of 8.83×10^{12} cm^{-2} and the electron mobility of 1800 cm$^{2}\cdot$V$^{-1}\cdot$s^{-1} were estimated by Hall measurement. Figure 1a shows the schematic image of AlGaN/GaN MIS-FinFET. The fabrication processes of the FinFETs were similar to our previous work [17]. Figure 1b,c exhibit the cross-sectional TEM images for the fin with sloped and steep sidewall surface, respectively. It was found that the formation of fin shape depends on the etching time in anisotropic lateral etching tetramethylammonium hydroxide (TMAH: 25% solution at 85 °C) solution. It was also found the slope of the dry-etched fin, prior to the TMAH wet etching, is important in determining the fin shape. However, the exact etching mechanism for the fin shape still remains unclear and further study is required. It is worth noting that, as shown Figure 1b, the sloped sidewall surface has ~12° off-angle to the m-plane, while the top AlGaN layer has a negatively sloped shape with almost the same off-angle as shown in both Figure 1b,c. This negative slope might be due to the existence of stress induced by lattice mismatch between AlGaN and GaN layers, which increases the etch rate at the interface during TAMH wet etching.

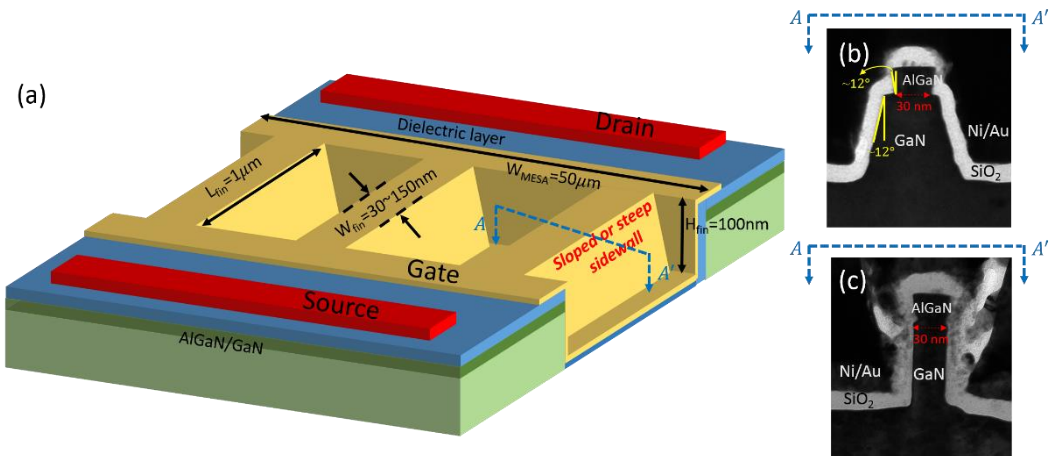


Figure 1. (**a**) Schematic image of AlGaN/GaN-based FinFET with either sloped sidewall surface or steep sidewall surface; (**b**) Cross-sectional TEM image of fin with sloped sidewall surface; (**c**) Cross-sectional TEM image of fin with steep sidewall surface.

The dielectrics, 20 nm-thick plasma enhanced chemical vapor deposited (PECVD) SiO_2 layer and 10 nm-thick atomic layer deposited (ALD) Al_2O_3 layer, were used to investigate the influence of different dielectric layer on device performance. The gate length (L_G), which corresponds to fin length (L_{fin}), and the mesa width for all devices are 1 and 50 µm, respectively. Both of the gate to drain spacing L_{GD} and the gate to source spacing L_{GS} are 5 µm. The fin height (H_{fin}) is 100 nm and the W_{fin} varies from 30 to 150 nm. All the devices have a fin number (N_{fin}) of 45. Drain current (I_D) and transconductance

(g_m) are normalized by gate width $(W_G) = \left[W_{fin} + width\ of\ GaN\ channel\ (50\ nm) \times 2\right] \times N_{fin}$, and V_{TH} is defined as the V_G when drain current I_D equals to 0.1 μA $\times \frac{W_G}{L_G}$.

3. Results and Discussion

Figure 2a,b show the logarithmic and linear transfer curves, respectively, for the sloped sidewall AlGaN/GaN MIS-FinFETs with 20 nm-thick SiO_2 gate dielectric varying the W_{fin} from 150 to 30 nm. The key parameters such as V_{TH}, SS, g_m peak value, full width at half maximum (FWHM) of g_m, and hysteresis of all the devices are summarized and shown in Table 1. The V_{TH} of the sloped FinFET with W_{fin} is 150 nm is −1.9 V and it shifts to a positive direction as the W_{fin} narrows, showing the V_{TH} of 0.3 V when W_{fin} is reduced to 30 nm. This positive shift of the V_{TH} is due to lateral depletion of the 2DEG channel from the sidewall. The SS values for all devices are smaller than 72 mV/dec, which are relatively low compared to those of conventional AlGaN/GaN-based HEMTs [21–23]. For the wide FinFETs with W_{fin} of 150 and 80 nm, the V_{TH} of the 2DEG channel is much lower than that of the MOS channel at sidewall surface and hence the 2DEG channel current dominates the subthreshold current of the device. In this case, the SS (~ 70 mV/dec) for the device can be mainly determined from the trap capacitance at AlGaN/GaN interface ($C_{it,AlGaN/GaN}$) and the existence of the depletion capacitance (C_{dep}) in wide bottom fin body below the 2DEG channel, which is not completely depleted by the lateral electric field from the sidewall gate. Besides, the V_{TH} difference between the 2DEG channel and MOS channel of these FinFETs with wide W_{fin} are relatively large and the two-channel currents become merged as the gate voltage increases to have the broad g_m curves as shown in Figure 2c, which is important in improving the device linearity [8,24].

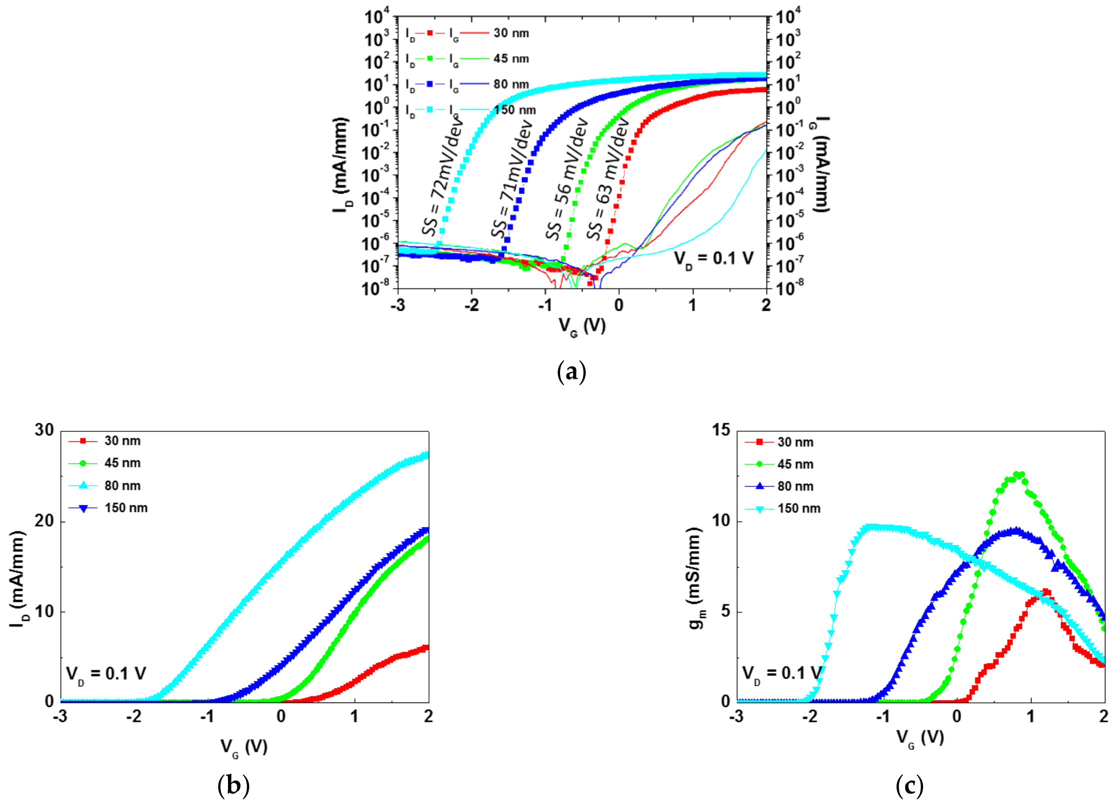


Figure 2. Sloped sidewall MIS-FinFETs with 20 nm-thick SiO_2 gate dielectric varying the W_{fin} from 150 to 30 nm. (**a**) Logarithmic transfer curves; (**b**) Linear transfer curves; (**c**) Transconductance curves.

Table 1. Key parameters for each device exhibited in Figure 2.

W_{fin} (nm)	V_{TH} (V)	SS (mV/dec)	g_m Peak (mS/mm)	FWHM of g_m (V)	Hysteresis (mV)
30	0.3	63	6.1	0.92	400
45	−0.2	54	12.6	1.52	320
80	−0.9	71	9.5	2.40	240
150	−1.9	72	9.8	3.12	120

On the other hand, the narrow FinFET with W_{fin} of 45 nm has a sharper and higher g_m peak as can be seen in Figure 2c, which means that the V_{TH} of the 2DEG channel and MOS channel are almost the same and hence both channels simultaneously turn on/off and the effective channel width of the device can be modulated with the gate voltage, which results in very small SS as low as 56 mV/dec, smaller than the theoretical Boltzmann limit of 60 mV/dec. As discussed in our previous work [17], the 2DEG channel will be generated at the center of the 2DEG channel and laterally spread until occupying the whole 2DEG channel as V_G increases from the V_{TH} of the 2DEG channel to just above it. Then, the MOS channel will instantaneously turn on because there is only a tiny V_{TH} difference between the top 2DEG channel and the sidewall MOS channel. In other words, the channel width first spread laterally within the 2DEG channel and then immediately spread vertically into the MOS channel, which makes the concept of gate-dependent effective channel width modulation reasonable. This sub-60 mV/dec SS can be understood by considering the expression for new $SS_{W(V_G)}$ which includes the gate voltage-dependent channel width modulation [17] as shown below,

$$SS_{W(V_G)} = \frac{1}{\frac{d\left(logI_{D,sub}\right)}{dV_G}} = \frac{1}{A + \frac{1}{SS_{con}}} = \frac{SS_{con}}{A \cdot \frac{1}{SS_{con}} + 1} \quad (1)$$

where $\frac{d\left(logI_{D,sub}\right)}{dV_G} = \frac{d[logW(\varphi_s)]}{dV_G} + \frac{d\left[\int_0^{V_D} Q_{ch}(V,\varphi_s)dV\right]}{dV_G} + \frac{d(log\mu)}{dV_G}$, $I_{D,sub} = \mu\frac{W(\varphi_s)}{L}\int_0^{V_D} Q_{ch}(V,\varphi_s)dV$. In these equations, φ_s and $Q_{ch}(V,\varphi_s)$ are the surface potential and the channel charges in the subthreshold region, respectively. $W_{(\varphi_s)}$ is the surface potential-dependent effective channel width which is constant in conventional devices. $I_{D,sub}$ is the channel current in the subthreshold region and $\frac{d\left(logI_{D,sub}\right)}{dV_G}$ is the differentiation of the logarithmic channel current. The first term $\frac{d[logW(\varphi_s)]}{dV_G}$ in $\frac{d\left(logI_{D,sub}\right)}{dV_G}$ is the channel width modulation and expressed as A in Equation (1). The third term is related to electron mobility and can be neglected. The inverse of the second term is SS_{con} for conventional devices without channel width modulation. SS_{con} can be expressed as,

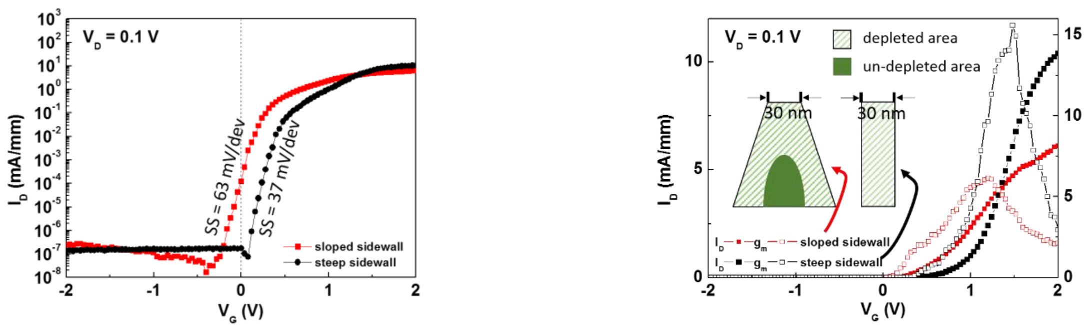
$$SS_{con} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right) \quad (2)$$

where k is the Boltzmann's constant, T is temperature, q is electronic charge, C_{ox} is the capacitance for gate oxide, and C_{it} is the trap capacitance either for the interface of AlGaN/GaN or dielectric/GaN. Normally, SS_{con} is larger than 60 mV/dec and cannot explain the sub-60 mV/dec characteristic observed in this work.

When W_{fin} is further reduced to 30 nm, the SS of the device increases slightly above 60 mV/dec again. This is because the V_{TH} of the 2DEG channel increases and hence the simultaneous turning on of these two channels tends to break to make the channel width modulation less effective. The V_{TH} of the 2DEG channel becomes higher than that of the MOS channel and becomes positive to show normally-off operation with V_{TH} of 0.3 V. In this case, the MOS channel current at sidewall surface dominates the subthreshold characteristics of the device and the SS can be determined mainly from the trap capacitance ($C_{it,\ SiO_2/GaN}$) at SiO_2/GaN interface, which leads to increased SS of 63 mV/dec. As a result, Figure 2c indicates that the g_m of the FinFET with W_{fin} of 30 nm becomes slightly broader and the peak value becomes lower again compared with that of FinFET with W_{fin} of 45 nm. As can be seen in

Figure 2a, SS first decreases below 60 mV/dec when W_{fin} is reduced to 45 nm and then increases again above 60 mV/dec with further decreasing W_{fin}, which depends on whether the 2DEG channel and MOS channel turn on at the same time or not as has already been discussed above. Correspondingly, with decreasing W_{fin}, as shown in Figure 2c, g_m curve becomes sharper as W_{fin} decreases to 45 nm, but becomes broad again when W_{fin} is reduced to 30 nm. Based on the tendency of SS and g_m curves as decreasing W_{fin} as shown in Figure 2a,b, it can be concluded that the g_m peak becomes sharp showing excellent subthreshold characteristics with SS of sub-60 mV/dec, if 2DEG channel and MOS channel of a FinFET are simultaneously turned on/off. However, most of the FinFETs with SiO_2 dielectric layer investigated in this work exhibits normally-on operation, thus they are not adequate to be used as efficient power switching or low power logic application due to large I_{OFF}, even though they exhibited excellent SS. A similar argument can be addressed even for the normally-off FinFET with W_{fin} of 30 nm, because I_{OFF} of the FinFET is still very high due to its low V_{TH}.

Figure 3a shows the comparison of the logarithmic transfer curves obtained from the FinFETs with sloped and steep sidewall surfaces. It is observed that the steep sidewall surface is m-plane and very smooth and uniform and has the lowest surface trap density, while the sloped sidewall has a rather rough and nonuniform surface, as shown in Figure 1b. The key parameters such as V_{TH}, SS, g_m peak value, and FWHM of g_m of all the devices are summarized and shown in Table 2. Both devices, which have the same W_{fin} of 30 nm and 20 nm-thick SiO_2 gate dielectric layer, exhibit normally-off operation, but the sloped sidewall device exhibits much higher I_{OFF} of 100 nA/mm, measured at V_G = 0 V, compared with that of steep sidewall device. The high I_{OFF} of the sloped sidewall device is due to its lower V_{TH} of 0.3 V, compared to V_{TH} of 0.6 V of the steep sidewall device. The lower V_{TH} of the sloped device is probably because the sidewall surface has a higher density of positive effective oxide charge at the GaN/SiO_2 interface as well as higher surface trap density caused by a relatively rough surface, compared to the steep m-plane sidewall surface [25]. This high positive oxide charge density in the sloped device lowers V_{TH} of the sidewall MOS channel to increase I_{OFF}. The SS of steep sidewall device is as low as 37 mV/dec due to the simultaneous turning on of 2DEG channel and MOS channel and the effective channel width modulation as discussed before [17]. On the other hand, the sloped sidewall device exhibits a relatively larger SS of 63 mV/dec, which could be explained by the existence of non-negligible C_{dep} caused by the undepleted part at the wide fin bottom and relatively large $C_{it,\ SiO_2/GaN}$ due to a rough sidewall surface [25], which increases both SS_{con} and $SS_{W(V_G)}$, while the C_{dep} can be ignored for the device with a steep sidewall because the entire fin is narrow and completely depleted from the electric field of the sidewall gate at off-state. The schematic images of both sloped and steep sidewall fin structures with un-depleted/depleted areas are shown in Figure 3b. The steep sidewall device exhibits a sharper and higher g_m peak, as shown in Figure 3b, which indicates that both the 2DEG channel and the MOS channel of the device simultaneously turn on almost at the same time.



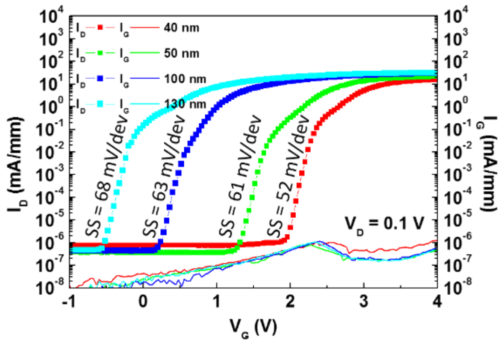
(**a**) (**b**)

Figure 3. (**a**) Logarithmic transfer curves of sloped sidewall FinFETs (red line) in this work and steep sidewall FinFETs (black line) in our previous work; (**b**) Transfer curves of the two devices in (**a**). The schematic images of sloped and steep sidewall fin structures are shown in the insert of (**b**).

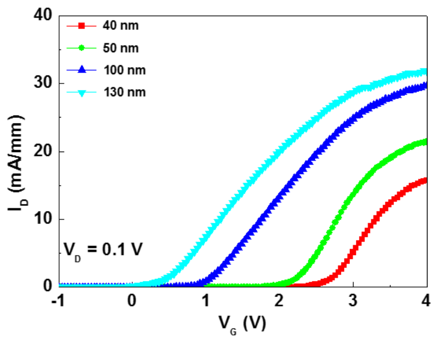
Table 2. Key parameters for each device exhibited in Figure 3.

W_{fin} (nm)	Sidewall Type	V_{TH} (V)	SS (mV/dec)	g_m Peak (mS/mm)	FWHM of g_m (V)
30	sloped	0.3	63	6.1	0.92
30	steep	0.6	37	15.6	0.60

To investigate the effect of the gate dielectric on the device performances, the SiO_2 layer was replaced with 10 nm-thick Al_2O_3 layers on the sloped sidewall FinFETs. All FinFETs with W_{fin} varied from 130 to 40 nm exhibit normally-off operation as shown in Figure 4a,b. The key parameters such as V_{TH}, SS, g_m peak value, FWHM of g_m, and hysteresis of all the devices are summarized and shown in Table 3. Similarly, V_{TH} of the FinFET shifts to a positive direction as W_{fin} decreases, but it increases up to a much higher value of 2.5 V for the FinFET with W_{fin} of 40 nm, which is probably due to the existence of the negative effective oxide charge at the interface between the Al_2O_3 dielectric layer and GaN [5,26,27].



(**a**)



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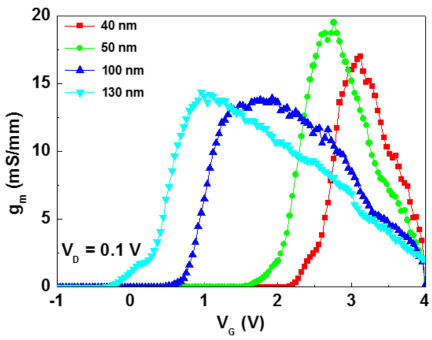

(**c**)

Figure 4. Sloped sidewall MIS-FinFETs with 10 nm-thick Al_2O_3 gate dielectric varying the W_{fin} from 130 to 40 nm. (**a**) Logarithmic transfer curves; (**b**) Linear transfer curves; (**c**) Transconductance curves.

Table 3. Key parameters for each device exhibited in Figure 4.

W_{fin} (nm)	V_{TH} (V)	SS (mV/dec)	g_m Peak (mS/mm)	FWHM of g_m (V)	Hysteresis (mV)
40	2.3	52	17	0.88	400
50	1.8	61	19.5	1.04	480
100	0.8	63	13.9	2.12	400
130	0	68	14.4	2.44	400

It is also observed that the FinFETs show considerably low I_{OFF} of ~0.1 nA/mm, except the FinFET with W_{fin} of 130 nm, which is essential for reducing the standby power consumption. Especially, the FinFET with W_{fin} of 40 nm exhibits excellent SS of 52 mV/dec, also smaller than the theoretically limited value of 60 mV/dec, which can be explained by the concept of effective channel width modulation and the simultaneous turn-on of 2DEG channel and MOS channel as discussed before. This fast switching characteristics of the device with its relatively high V_{TH} of 2.5 V and low off-state leakage current would lead to improvement of efficiency and ensure the safety of power switching devices [28]. The g_m peak becomes sharper as the W_{fin} of the FinFET decreases, as shown in Figure 4b, which is similar to the case of the FinFETs with SiO_2 gate dielectric layer and a similar argument can be also addressed for the reason.

According to the discussion above, it can be seen that it is a possible method to realize relatively high V_{TH}, small SS, and low I_{OFF} in AlGaN/GaN MIS-FinFETs by carefully adjusting W_{fin} as well as choosing the sidewall plane, which corresponds to the controlling of threshold voltages. As W_{fin} varies, the shape of g_m curve becomes sharper as the V_{TH} difference between the 2DEG channel and the MOS channel becomes closer.

4. Conclusions

In this work, AlGaN/GaN MIS-FinFETs were fabricated and characterized using 20 nm-thick SiO_2 and 10 nm-thick Al_2O_3 as dielectric layers, respectively. The effects of the sidewall plane on device performance were also investigated. The sloped sidewall FinFET with 20 nm-thick SiO_2 dielectric layers and W_{fin} of 45 nm shows the lowest SS of 56 mV/dec among the FinFETs which can be explained by the concept of effective channel width modulation and the simultaneous turn-on of 2DEG channel and sidewall MOS channel. The SS is further decreased to 37 mV/dec for the steep sidewall FinFET with W_{fin} of 30 nm. However, the sloped sidewall FinFET with the same W_{fin} of 30 nm, which has a relatively rough sidewall surface, show low V_{TH}, large SS, and high I_{OFF} probably due to the high density of positive effective fixed oxide charges and trap charges at the SiO_2/GaN interface. On the other hand, the sloped sidewall FinFETs with 10 nm-thick Al_2O_3 dielectric layer show normally-off operation with relatively high V_{TH}, small SS, and low I_{OFF}. In our opinion, these performances are probably due to the existence of negative effective fixed oxide charge at the Al_2O_3/GaN interface, even though the FinFETs have sloped sidewalls. The device with W_{fin} of 40 nm exhibits SS of 52 mV/dec with V_{th} of 2.3 V, which might be promising for efficient power switching application.

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