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Implementation of a Wide Input Voltage Resonant Converter with Voltage Doubler Rectifier Topology

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Abstract: A new circuit structure of *LLC* converter is studied and implemented to achieve wide zero-voltage switching range and wide voltage operation such as consumer power units without power factor correction and long hold up time demand, battery chargers, photovoltaic converters and renewable power electronic converters. The dc converter with the different secondary winding turns is adopted and investigated to achieve the wide input voltage operation (50–400 V). To meet wide voltage operation, the full bridge and half bridge dc/dc converters with different secondary turns can be selected in the presented circuit to have three different voltage gains. According to input voltage range, the variable frequency scheme is employed to have the variable voltage gain to overcome the wide input voltage operation. Therefore, the wide soft switching load variation and wide voltage operation range are achieved in the presented resonant circuit. The prototype circuit is built and tested and the experiments are demonstrated to investigate the circuit performance.

Keywords: frequency modulation; dc/dc converters; wide voltage variation; soft switching operation

1. Introduction

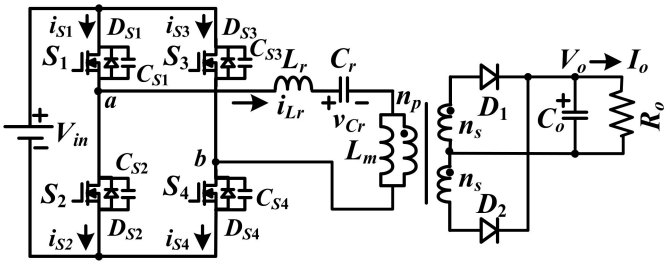
Power electronics are more and more important for the energy conversion systems such as renewable power conversion, electric vehicle systems, traction vehicles, light rail vehicles, dc nano- or micro-grid systems, battery-based storage systems, personal computer power units and industry power units. Power semiconductors such as insulated gate bipolar transistors (IGBTs), Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), Gallium Nitride (GaN) FET and Silicon Carbide (SiC) devices are widely used power switches in power electronic circuits. However, IGBT devices have low switching frequency problem. GaN and SiC devices have the advantages of low switching loss and high frequency operation. However, the cost of GaN and SiC is much more expensive than the IGBT and MOSFET devices. Compared to IGBT, GaN and SiC devices, MOSFET elements have low cost and medium frequency operation for modern power converters. Pulse-width modulation (PWM) power electronic circuits have been widely studied and developed in power electronics to lessen reduce global warming and air pollution problems. The dc-dc or dc-ac power converters are the most attractive interface circuits between the photovoltaic (PV) cells (or fuel cells) and the utility dc or ac voltage. However, the output voltage of PV cells, fuel cells and dc wind turbine power generators is not constant and related to solar intensity or wind speed. Conventional duty cycle control converters [1–4] and frequency control converters [5–7] cannot be operated well under wide voltage variation condition due to the limit voltage gain of power converters. Multi-stage dc converters with parallel or series structure [8–11] have been researched to overcome wide voltage variation problem and used for renewable energy conversion and battery charger applications. However, the disadvantages of multi stage dc-dc converters have low reliability and more active and passive power components. Two full bridge circuits structure was presented in [12] to overcome limit voltage range

problem of conventional resonant converters. However, sixteen power semiconductors are used in this circuit structure. The conventional *LLC* converter with two sets of secondary windings was studied in [13] to have wide hold-up time operation for PC power units. The main drawbacks of this circuit structure are four secondary windings and large copper losses. The resonant converter with interleaved duty cycle control was achieved in [14] to overcome wide voltage variation problem and achieve low current ripple input. However, the circuit topology is still the multi stage converter.

The new resonant converter with voltage doubler configuration and two sets of secondary windings is presented in this paper to accomplish soft switching operation and overcome wide voltage input variation (V_{in} = 50–400 V). According to the input voltage range, the present *LLC* converter can be operated under full bridge resonant structure or half bridge resonant structure with different secondary turns. Therefore, the proposed converter has much wide range of input voltage operation. When V_{in} = 50–100 V (low voltage region), the full bridge type *LLC* circuit with more secondary turns is operated to have high voltage gain. If V_{in} = 100–200 V (medium voltage input region), the full bridge type *LLC* circuit with fewer secondary turns is adopted to have less dc voltage gain. If V_{in} = 200–400 V (high voltage input region), the half bridge structure is used to obtain the lowest voltage gain on the presented circuit. With the proposed control strategy, the wide voltage operation (V_{in} = 50–400 V) is accomplished in the presented circuit structure. Since the proposed resonant circuit is controlled under the variable switching frequency with input inductive impedance operation, the active switches have soft switching turn-on characteristic. The voltage doubler rectification structure can reduce the voltage rating of diodes compared to the center-tapped rectifier topology. Thus, the diode conduction loss can be reduced. The proposed *LLC* converter has less circuit components compared to the wide voltage resonant converter presented in [8–14]. Finally, the experimental verifications are provided to demonstrate the performance of the studied *LLC* resonant circuit.

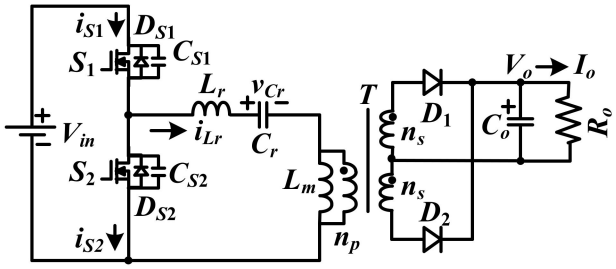
2. Circuit Configuration and Principles of Operation

The conventional resonant converters with half bridge or full bridge structure are provided in Figure 1. The fundamental root-mean-square (rms) input voltage of full bridge structure is two times of the fundamental rms input voltage of half bridge structure. Therefore, the full bridge resonant converter has more power capability than the half bridge resonant converter. Owing to the center-tapped rectification structure, the diodes D_1 and D_2 has at least $2V_o$ voltage stress. The other disadvantage of the center-tapped rectifier is two winding sets are needed on the secondary side of transformer T. For high load current applications, there are more copper losses on the secondary windings.



(**a**)

Figure 1. *Cont.*



(**b**)

Figure 1. Structures of the conventional *LLC* converters: (**a**) full bridge *LLC* structure; (**b**) half bridge *LLC* structure.

The proposed *LLC* hybrid converter is provided in Figure 2a to overcome the disadvantage of narrow voltage range in conventional *LLC* converter. The adopted circuit comprises a full bridge resonant circuit and a voltage double rectifier with variable winding turns to have wide voltage operation capability (50–400 V) and wide soft switching operation. L_r is the series resonant inductance, L_m is the magnetizing inductance and C_r is the series resonant capacitance. According to the switching status of S_1–S_4, the converter can operate as the full bridge circuit structure (Figure 2b,c) or half bridge circuit structure (Figure 2d). The *LLC* resonant tank with C_r, L_r and L_m is operated with variable frequency to have inductive input impedance and zero-voltage turn-on switching for all devices S_1–S_4. The variable secondary turns are controlled by S_{ac} to achieve different voltage gains. S_{ac} is realized with two back-to-back MOSFETs. According to the adopted circuit configuration, the converter has three operation sub-circuits under three different input voltage regions. Figure 2b–d give the equivalent circuits for low, medium and high input voltage conditions respectively. If 50 V < V_{in} < 100 V (low voltage region $V_{in,L}$), then switches S_1–S_4 are controlled by frequency modulation and S_{ac} is in the on-state. Figure 2b gives the circuit diagram for low input voltage operation. The voltage v_{ab} has voltage level V_{in} or $-V_{in}$. The $2n_s$ winding turns and diodes D_1 and D_2 are connected to output load. The voltage gain under low input voltage region is obtained as $V_o/V_{in,L} = G_{ac}(f_{sw})(4n_s)/n_p$, where $G_{ac}(f)$ is the voltage transfer function of resonant tank. From the conduction states of the power semiconductors, the circuit in Figure 2b has six or four states in one switching period under the f_r (series resonant frequency) > or < f_{sw} (switching frequency). If 100 V < V_{in} < 200 V (medium voltage region $V_{in,M}$), S_{ac} turns off and Figure 2c gives the equivalent circuit configuration. It is clear to observe that D_2 and D_1 are off. The n_s winding turns and diodes D_3 and D_4 are connected to load.

The voltage gain in Figure 2c is $V_o/V_{in,M} = G_{ac}(f_{sw})(2n_s)/n_p$. If 200 V < V_{in} < 400 V (high voltage region $V_{in,H}$), the active switches S_3 and S_{ac} are turned off and S_4 is always in the on-state. Figure 2d illustrates the circuit diagram operated at high voltage region. The leg voltage v_{ab} has voltage level V_{in} or 0. Only n_s winding turns and diodes D_3 and D_4 are connected to load. The voltage gain in Figure 2d is $V_o/V_{in,H} = G_{ac}(f_{sw})n_s/n_p$. From the three voltage gains in previous discussion, it can observe that $V_o/V_{in,L} = G_{ac}(f_{sw})(4n_s)/n_p = 2V_o/V_{in,M} = 4V_o/V_{in,H}$. Thus, one can conclude that $V_{in,H} = 2V_{in,M} = 4V_{in,L}$. Therefore, the proposed *LLC* converter has the highest voltage gain at low voltage region $V_{in,L}$ and the lowest voltage gain at high voltage region $V_{in,H}$.

2.1. Low Voltage Region ($V_{in,L}$: 50–100 V)

When S_{ac} is in the on-state, the *LLC* converter has less transformer turns-ratio $n_p/(2n_s)$ and large voltage gain. Under this condition, the rectifier diodes D_3 and D_4 are always off. The voltage gain of the converter is obtained as $V_o/V_{in,L} = G_{ac}(f_{sw})(4n_s)/n_p$. From the gating signals of S_1–S_4 and the on/off state of D_1 and D_2, six equivalent operating states per switching periods are provided in Figure 3.

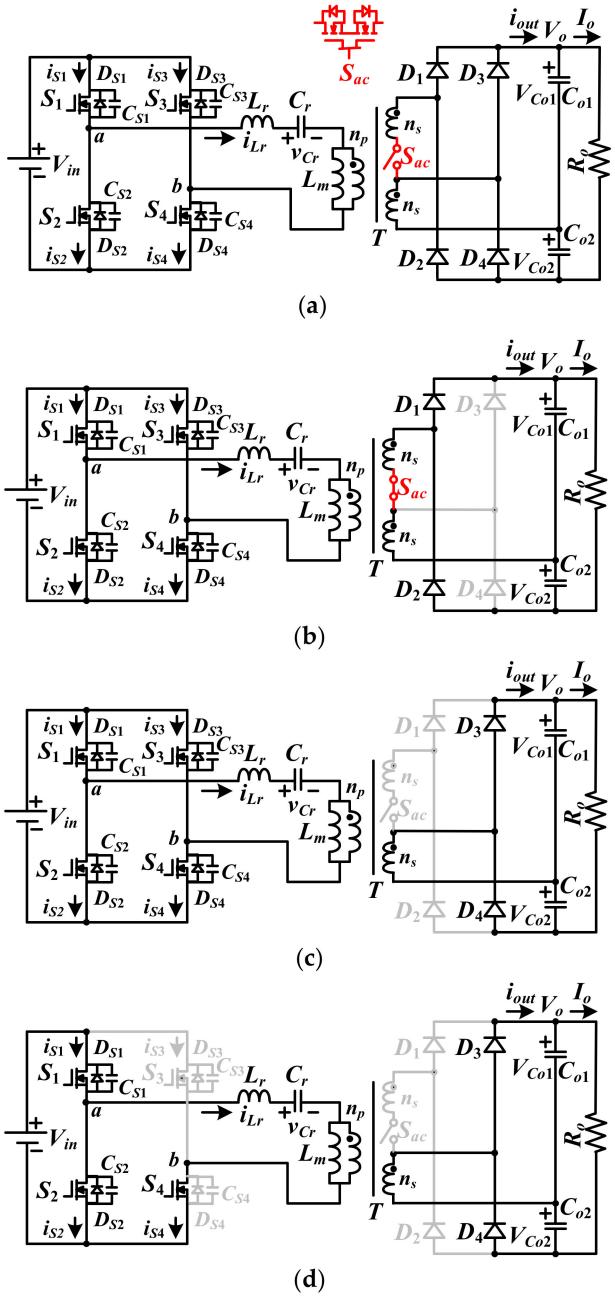


Figure 2. Proposed converter: (**a**) circuit diagram; (**b**) low input voltage region; (**c**) medium input voltage region; (**d**) high input voltage region.

State 1 [t_0–t_1]: When $t = t_0$, $v_{CS1} = v_{CS4} = 0$ V. Power devices S_4 and S_1 turn on at this moment to realize soft switching operation due to $i_{Lr}(t_0) < 0$. Since $i_{Lr} > i_{Lm}$, D_1 conducts in this state. In state 1, $v_{ab} = V_{in,L}$, $v_{Lm} = (V_{Co1}n_p)/(2n_s) \approx (V_o n_p)/(4n_s)$ and i_{Lm} increases. The resonant frequency of the *LLC* converter in this state is $f_{r,1} = 1/[2\pi\sqrt{L_r C_r}]$. If $f_{r,1} >$ or $< f_{sw}$, then the circuit operation will go to state 2 or 3.

State 2 [t_1–t_2]: When $i_{D1} = 0$ at t_1, D_1 is turned off with zero-current switching. The resonant frequency in state 2 is $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r + L_m)}]$. It is obvious that $f_{r,1} > f_{r,2}$. The current variation on L_m approximates $\Delta i_{Lm} \approx \left(n_p V_o\right)/\left(8 n_s L_m f_{sw}\right)$ and the magnetizing current i_{Lm} at t_2 is $i_{Lm}(t_2) = \Delta i_{Lm}/2 \approx (n_p V_o)/(16 n_s L_m f_{sw})$.

State 3 [t_2–t_3]: Power devices S_1 and S_4 are off at time t_2. Since $i_{Lr}(t_2)$ is positive, v_{CS3} and v_{CS2} are decreased. Due to $i_{Lm}(t_2) > i_{Lr}(t_2)$, D_2 is conducting. To ensure the soft switching turn-on

of S_3 and S_2, the current $i_{Lm}(t_2)$ must be greater than $V_{in,L}\sqrt{C_{oss}/(L_m+L_r)}$ where $C_{oss} = C_{S1} = \ldots = C_{S4}$. The other necessary condition for zero-voltage switching is that the dead time t_d between S_2 and S_1 is greater than time interval in state 3. To accomplish this condition, one can obtain $L_{m,\max} = (t_d V_o n_p)/(32 C_{oss} n_s f_{sw} V_{in,L})$.

State 4 [t_3–t_4]: At time t_3, $v_{CS2} = v_{CS3} = 0$ V. At this moment, power devices S_3 and S_2 are turned on under zero voltage. Owing to $i_{Lm}(t_3) > i_{Lr}(t_3)$, D_2 conducts. In state 2, $v_{ab} = -V_{in,L}$, $v_{Lm} = -(V_{Co2} n_p)/(2n_s) \approx -(V_o n_p)/(4n_s)$, i_{Lm} decreases and C_{o1} (C_{o2}) is discharged (charged). If $f_{r,1} >$ or $< f_{sw}$, then the circuit operation will go to state 4 or 6.

State 5 [t_4–t_5]: If $f_{r,1} > f_{sw}$, one obtains i_{D2} equals 0 at t_4. Then, D_2 turns off. The resonant frequency in state 4 is $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r+L_m)}]$. The magnetizing current i_{Lm} at t_5 approximates $i_{Lm}(t_5) \approx -(n_p V_o)/(16 n_s L_m f_{sw})$.

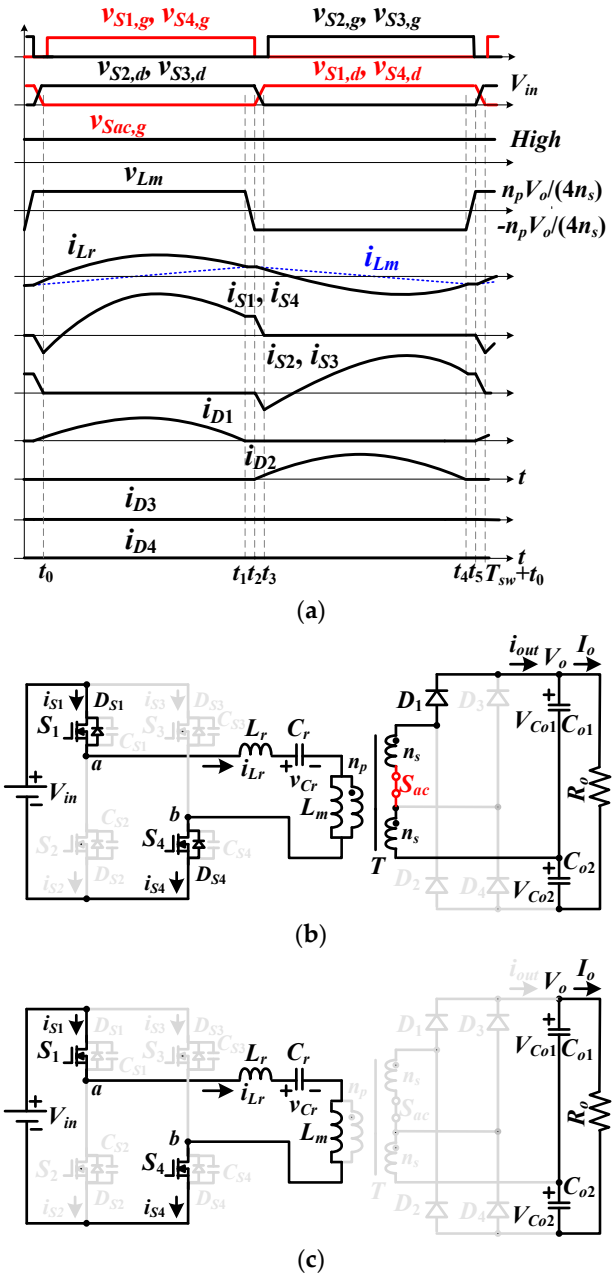


Figure 3. *Cont.*

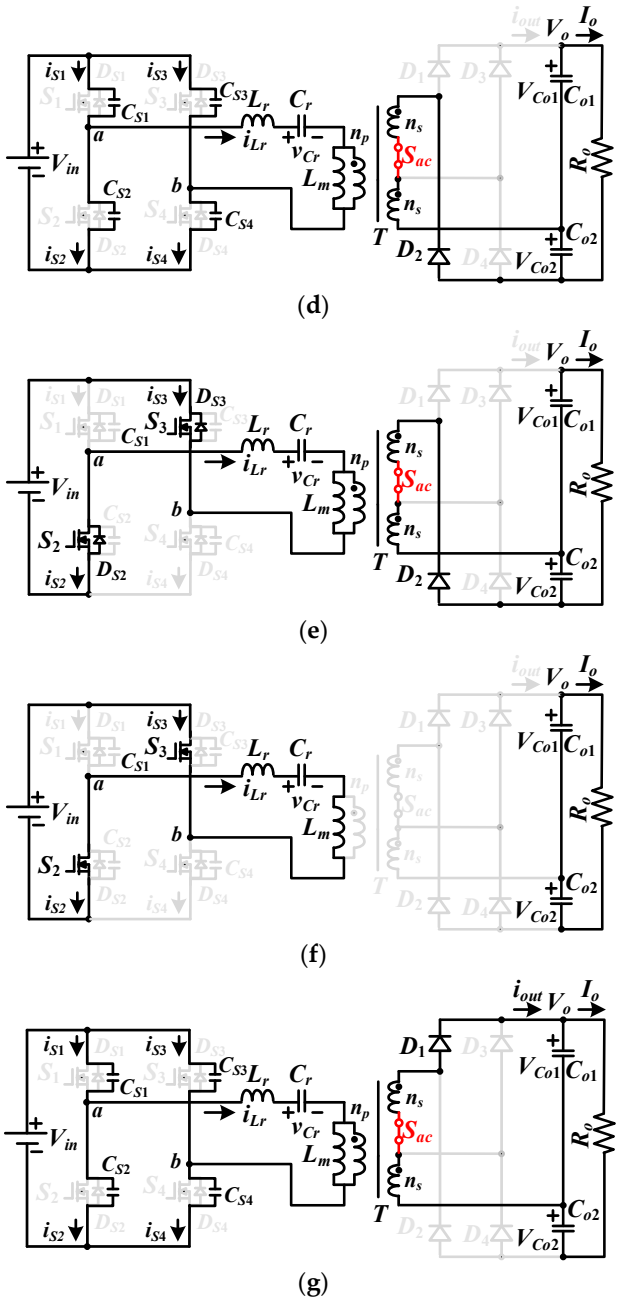


Figure 3. *LLC* converter at low input voltage region: (**a**) key PWM waveforms; (**b**) state 1 equivalent circuit; (**c**) state 2 equivalent circuit; (**d**) state 3 equivalent circuit; (**e**) state 4 equivalent circuit; (**f**) state 5 equivalent circuit; (**g**) state 6 equivalent circuit.

State 6 [t_5–T_{sw} + t_0]: S_3 and S_2 turn off at t_5. C_{S1} and C_{S4} are discharged owing to $i_{Lr}(t_5) < 0$. Since $i_{Lr}(t_5) > i_{Lm}(t_5)$, the rectifier diode D_1 conducts. To achieve soft switching turn-on of S_4 and S_1, the magnetizing inductor current i_{Lm} at t_5 is obtained and expressed as $|i_{Lm}(t_5)| \geq V_{in,L}\sqrt{C_{oss}/(L_m + L_r)}$.

2.2. Medium Voltage Region ($V_{in,M}$: 100–200 V)

If V_{in} is in the medium voltage region between 100 V and 200 V, the switch S_{ac} is tuned off. The converter has low transformer turns-ratio n_p/n_s and less voltage gain. The circuit diagram is shown in Figure 2c. The voltage gain at medium voltage operation is equal to $V_o/V_{in,M} = G_{ac}(f_{sw})(2n_s)/n_p$. Figure 4 shows the key PWM waveforms and state circuits for medium voltage operation (100–200 V).

State 1 [t_0–t_1]: The drain-to-source voltages of S_1 and S_4 are decreased and equal to zero at t_0. Due to $i_{Lr}(t_0) < 0$, the primary-side current i_{Lr} flows through the anti-parallel diodes D_{S4} and D_{S1}. Power devices S_4 and S_1 turn on at this moment to accomplish soft switching turn-on. Since $i_{Lr} > i_{Lm}$, D_3 conducts. From Figure 4b, it can obtain that $v_{ab} = V_{in}$, $v_{Lm} \approx (V_o n_p)/(2n_s)$, i_{Lm} increases and the resonant frequency $f_{r,1} = 1/[2\pi\sqrt{L_r C_r}]$. In this state, C_{o1} is charged and C_{o2} is discharged.

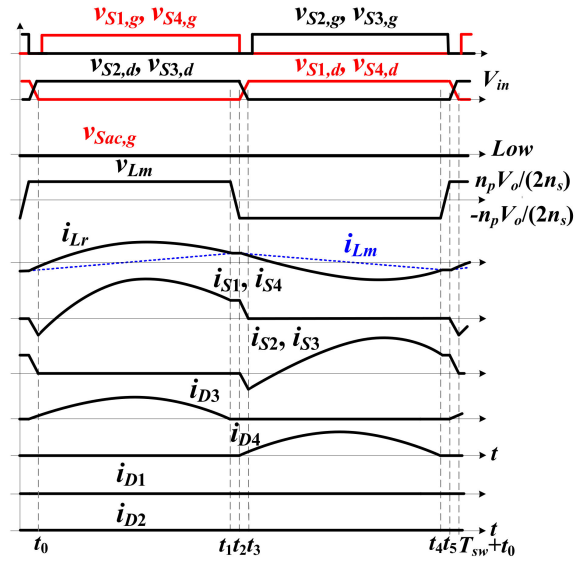
State 2 [t_1–t_2]: If $f_{r,1} > f_{sw}$, then i_{D3} is decreased to zero ampere at time t_1 and D_3 turns off at zero-current switching. Then, the resonant frequency in state 2 is $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r + L_m)}]$. The magnetizing current i_{Lm} at the end of this state is $i_{Lm}(t_2) \approx (n_p V_o)/(8n_s L_m f_{sw})$.

State 3 [t_2–t_3]: Power devices S_4 and S_1 are turned off in state 3. The positive primary current $i_{Lr}(t_2)$ will discharge C_{S2} and C_{S3}. Owing to $i_{Lm}(t_2) > i_{Lr}(t_2)$, D_4 on the output-side is conducting. The soft switching turn-on condition of S_3 and S_2 is $i_{Lm}(t_2) \geq V_{in,M}\sqrt{C_{oss}/(L_m + L_r)}$. To ensure $v_{CS2} = v_{CS3} = 0$ at t_3, the maximum magnetizing inductance $L_{m,max}$ is obtained as $L_{m,\max} = (t_d V_o n_p)/(16 C_{oss} n_s f_{sw} V_{in,M})$.

State 4 [t_3–t_4]: The v_{CS3} and v_{CS2} are decreased to zero at t_3. The primary-side current $i_{Lr}(t_3)$ is positive and flows through the body diodes D_{S2} and D_{s3}. At this moment, power devices S_3 and S_2 turn on to realize zero-voltage switching. Since $i_{Lm}(t_3) > i_{Lr}(t_3)$, D_4 conducts. From Figure 4e, it can obtain that $v_{ab} = -V_{in}$, $v_{Lm} \approx -(V_o n_p)/(2n_s)$ and i_{Lm} decreases. The output capacitors C_{o1} and C_{o2} are discharged and charged.

State 5 [t_4–t_5]: i_{D4} is decreased and equal to zero at t_4. Then, D_4 turns off. The resonant frequency in state 5 is $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r + L_m)}]$. The magnetizing current i_{Lm} at t_5 approximates $i_{Lm}(t_5) \approx -(n_p V_o)/(8n_s L_m f_{sw})$.

State 6 [t_5–$T_{sw} + t_0$]: Power devices S_3 and S_2 turn off in this state. $i_{Lr}(t_5)$ is negative and discharges C_{S1} and C_{S4}. Since $i_{Lr}(t_5) > i_{Lm}(t_6)$, D_3 is conducting. The soft switching turn-on condition of S_4 and S_1 is obtained as $|i_{Lm}(t_5)| \geq V_{in,M}\sqrt{C_{oss}/(L_m + L_r)}$.



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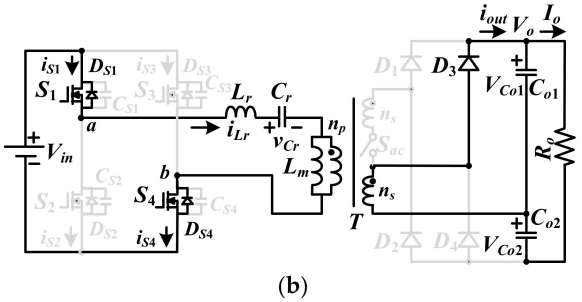

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Figure 4. *Cont.*

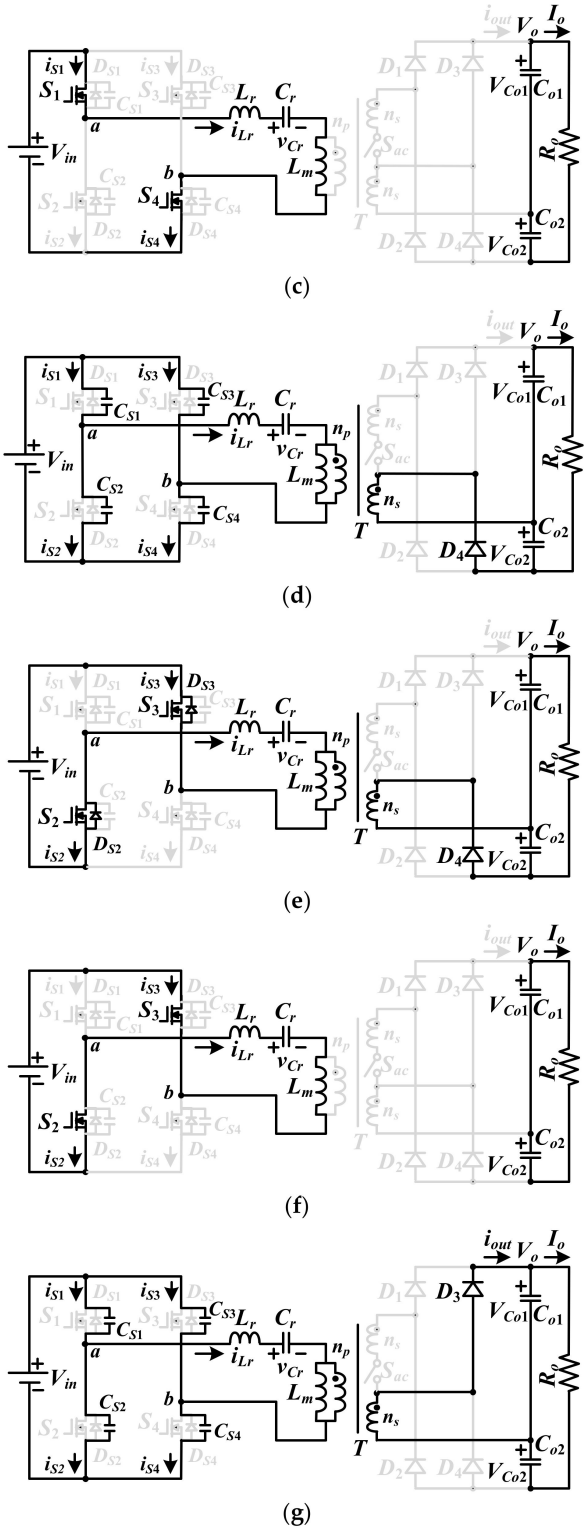


Figure 4. *LLC* converter at medium input voltage region: (**a**) key PWM waveforms; (**b**) state 1 equivalent circuit; (**c**) state 2 equivalent circuit; (**d**) state 3 equivalent circuit; (**e**) state 4 equivalent circuit; (**f**) state 5 equivalent circuit; (**g**) state 6 equivalent circuit.

2.3. High Voltage Region ($V_{in,H}$: 200–400 V)

When V_{in} is increased from 200 V to 400 V, the presented circuit is controlled under high input voltage region. Power devices S_3 and S_{ac} turn off and S_4 turns on. Only power semiconductors S_2 and

S_1 are controlled with frequency modulation so that the half bridge *LLC* resonant circuit (S_1, S_2, S_4, L_r, C_r and T) is operated on the input-side. The voltage gain of the converter at high voltage region is $V_o/V_{in,H} = G_{ac}(f_{sw})n_s/n_p$. From the on/off state of D_3, D_4, S_1 and S_2, six equivalent operating states per switching periods can be observed in Figure 5 for high input voltage range (200–400 V).

State 1 [t_0–t_1]: The capacitor voltage $v_{CS1} = 0$ at time t_0. The primary-side current $i_{Lr}(t_0)$ is negative so that the body diode D_{S1} conducts and the leg voltage $v_{ab} = V_{in}$. Due to $i_{Lr} > i_{Lm}$, D_3 is forward biased. The inductor voltage $v_{Lm} \approx (V_o n_p)/(2n_s)$. The resonant frequency $f_{r,1} = 1/[2\pi\sqrt{L_r C_r}]$ and C_{o1} is charged in this state.

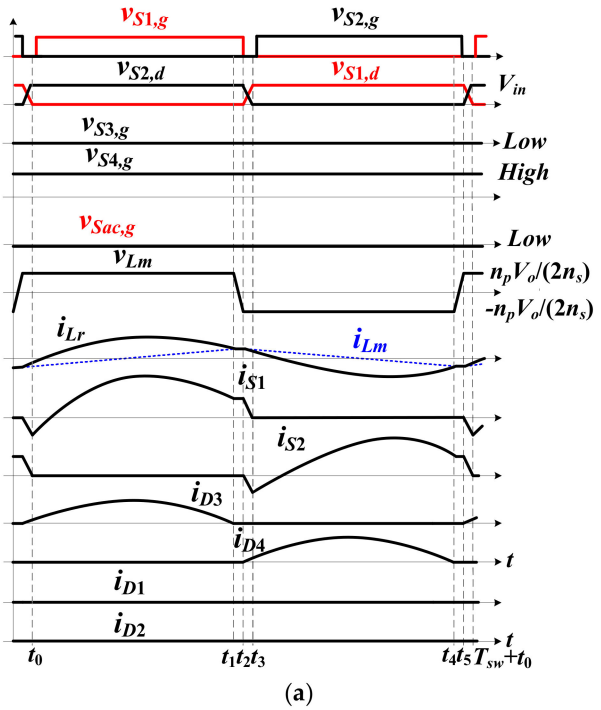
State 2 [t_1–t_2]: If $f_{r,1} > f_{sw}$, $i_{D3} = 0$ at time t_1. Then D_3 is turned off at zero-current switching. The resonant frequency in state 2 is expressed as $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r + L_m)}]$. At time t_2, $i_{Lm}(t_2) \approx (n_p V_o)/(8n_s L_m f_{sw})$ and S_1 turns off.

State 3 [t_2–t_3]: Power device S_1 is turned off in this state. The primary current $i_{Lr}(t_2)$ is positive and discharges C_{S2}. To ensure the soft switching turn-on of S_2, the inductor current $i_{Lm}(t_2)$ must greater than $V_{in,H}\sqrt{2C_{oss}/(L_m + L_r)}$. The other necessary condition for zero-voltage switching is that the dead time t_d between S_2 and S_1 is greater than time interval in state 3. To achieve this condition, the magnetizing inductance can obtain $L_{m,\max} = (t_d V_o n_p)/(16C_{oss} n_s f_{sw} V_{in,H})$.

State 4 [t_3–t_4]: The drain-to-source voltage $v_{CS2} = 0$ at t_3. The primary current $i_{Lr}(t_3) > 0$ and i_{Lr} flows through the body diode D_{S2}. At this moment, S_2 turns on to have zero-voltage switching operation. Since $i_{Lr}(t_3) < i_{Lm}(t_3)$, D_4 is conducting. From Figure 5e, it is clear that $v_{ab} = 0$, $v_{Lm} \approx -(V_o n_p)/(2n_s)$ and i_{Lm} decreases.

State 5 [t_4–t_5]: i_{D4} is decreased to zero at time t_4 and D_4 turns off at zero-current switching. The resonant frequency in state 5 is $f_{r,2} = 1/[2\pi\sqrt{C_r(L_r + L_m)}]$. S_2 is turned off at the end of this state and $i_{Lm}(t_5)$ is expressed as $i_{Lm}(t_5) \approx -(n_p V_o)/(8n_s L_m f_{sw})$.

State 6 [t_5–$T_{sw} + t_0$]: Owing to $i_{Lr}(t_5) < 0$, i_{Lr} discharge C_{S1}. The soft switching turn-on of S_1 is $|i_{Lm}(t_5)| \geq V_{in,H}\sqrt{2C_{oss}/(L_m + L_r)}$. The capacitor C_{S1} is discharged to zero voltage at time $t_0 + T_{sw}$.



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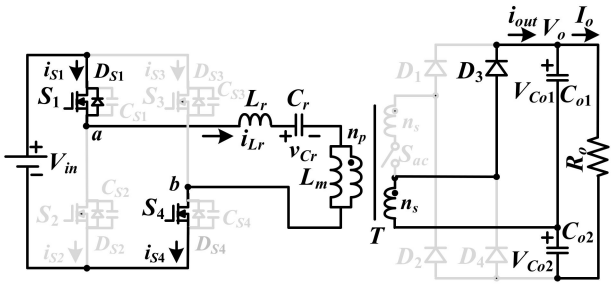

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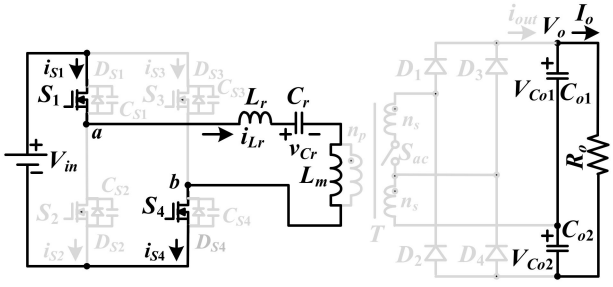
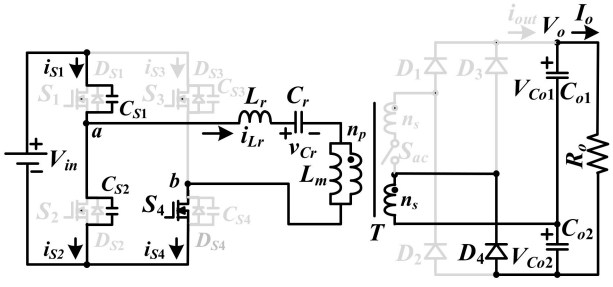


(**c**)



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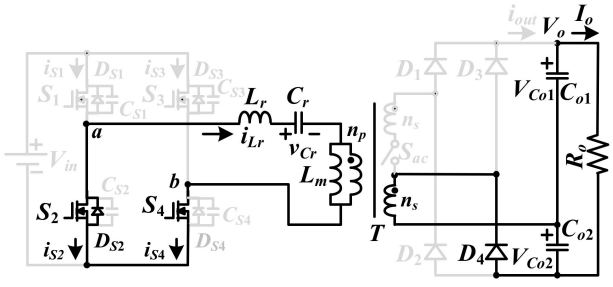

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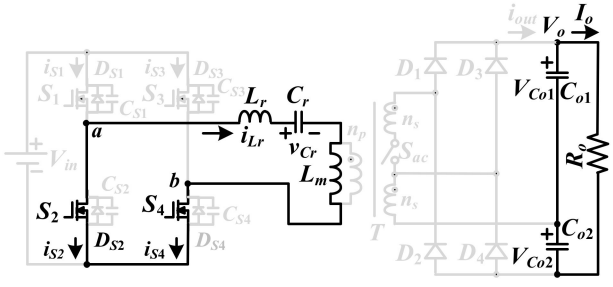

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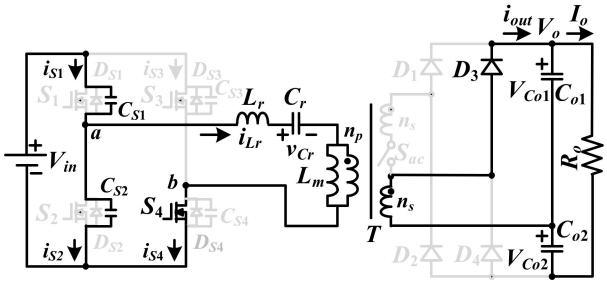


(g)

Figure 5. *LLC* converter at low high voltage region: (**a**) key PWM waveforms; (**b**) state 1 equivalent circuit; (**c**) state 2 equivalent circuit; (**d**) state 3 equivalent circuit; (**e**) state 4 equivalent circuit; (**f**) state 5 equivalent circuit; (**g**) state 6 equivalent circuit.

3. Circuit Characteristics and Design Example

The proposed *LLC* resonant converter is operated by variable frequency control. The square voltage waveform is generated on the leg voltage v_{ab} with voltage values $\pm V_{in}$ in Figure 2b,c or V_{in} and 0 in Figure 2d. The circuit characteristics of the converter are based on the fundamental frequency analysis. Figure 6 gives the equivalent resonant circuit on the input-side. $R_{e,ac}$ is the primary-side resistance of transformer T and $v_{ab,rms}$ is the input fundamental voltage. From the leg voltage v_{ab} in Figure 2, the fundamental root mean square (*rms*) voltage $v_{ab,rms}$ can be expressed in Equation (1).

$$v_{ab,rms} = \begin{cases} \frac{2\sqrt{2}V_{in}}{\pi}, & \text{in low and medium input voltage regions} \\ \frac{\sqrt{2}V_{in}}{\pi}, & \text{in high input voltage region} \end{cases} \tag{1}$$

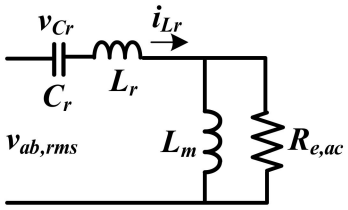


Figure 6. The equivalent resonant circuit on the primary-side.

In low input voltage operation, S_{ac} is always in the on-state. The equivalent turns-ratio of transformer T in Figure 2b is $n_p/(2n_s)$ and the *rms* value of the magnetizing voltage $v_{Lm,rms} = V_o n_p / \left(\sqrt{2}\pi n_s\right)$. In medium and high input voltage ranges (Figure 2c,d), S_{ac} is always in the off-state. The equivalent turns-ratio of transformer T is n_p/n_s. Thus, the *rms* value of the magnetizing voltage $v_{Lm,rms} = \sqrt{2}V_o n_p/(\pi n_s)$. The primary-side equivalent resistance $R_{e,ac}$ is obtained as $R_{e,ac} = \left(n_p/n_s\right)^2 R_o/\left(2\pi^2\right)$ in low input voltage operation or $R_{e,ac} = 2\left(n_p/n_s\right)^2 R_o/\pi^2$ in medium and high input voltage operation. From the resonant circuit in Figure 6, the output/input transfer function is expressed in Equation (2).

$$\left|G_{ac}(f_{sw})\right| = 1/\sqrt{\frac{\frac{L_r}{C_r}}{R_{e,ac}^2}\left[\left(\frac{f_{sw}}{f_r}\right)^2 - 1\right]^2}{\left(\frac{f_{sw}}{f_r}\right)^2} + \left[1 + \frac{\left(\frac{f_{sw}}{f_r}\right)^2 - 1}{\frac{L_m}{L_r}\left(\frac{f_{sw}}{f_r}\right)^2}\right]^2} = \begin{cases} \frac{V_o n_p}{4V_{in,L} n_s}, & \text{in low voltage region} \\ \frac{V_o n_p}{2V_{in,M} n_s}, & \text{in medium voltage region} \\ \frac{V_o n_p}{V_{in,H} n_s}, & \text{in high voltage region} \end{cases} \tag{2}$$

The output voltage V_o can be expressed in Equations (3)–(5) for low, medium and high input voltage regions.

$$V_o = 4V_{in,L}n_s/(n_p \sqrt{\frac{\frac{L_r}{C_r}\left[\left(\frac{f_{sw}}{f_r}\right)^2 - 1\right]^2}{\left(\frac{f_{sw}}{f_r}\right)^2} + \left[1 + \frac{\left(\frac{f_{sw}}{f_r}\right)^2 - 1}{\frac{L_m}{L_r}\left(\frac{f_{sw}}{f_r}\right)^2}\right]^2}) \quad (3)$$

$$V_o = 2V_{in,M}n_s/(n_p \sqrt{\frac{\frac{L_r}{C_r}\left[\left(\frac{f_{sw}}{f_r}\right)^2 - 1\right]^2}{\left(\frac{f_{sw}}{f_r}\right)^2} + \left[1 + \frac{\left(\frac{f_{sw}}{f_r}\right)^2 - 1}{\frac{L_m}{L_r}\left(\frac{f_{sw}}{f_r}\right)^2}\right]^2}) \quad (4)$$

$$V_o = V_{in,H}n_s/(n_p \sqrt{\frac{\frac{L_r}{C_r}\left[\left(\frac{f_{sw}}{f_r}\right)^2 - 1\right]^2}{\left(\frac{f_{sw}}{f_r}\right)^2} + \left[1 + \frac{\left(\frac{f_{sw}}{f_r}\right)^2 - 1}{\frac{L_m}{L_r}\left(\frac{f_{sw}}{f_r}\right)^2}\right]^2}) \quad (5)$$

In the proposed circuit, the electric specifications are V_{in} = 50–400 V, V_o = 48 V and P_o = 500 W. The design resonant frequency f_r = 100 kHz. The assumed inductance ratio L_m/L_r is 6. Since the resonant tank is identical for the operation in low, medium and high voltage ranges as shown in Figure 6, the following design procedures are based on the high input voltage condition ($V_{in,H}$ = 200–400 V). The assume voltage gain of resonant converter is 0.95 at V_{in} = 400 V case. Thus, the primary-secondary turn n_p/n_s can be calculated as.

$$n_p/n_s = G_{ac}(f_{sw})V_{in}/V_o = 0.95 \times 400/48 = 7.916 \quad (6)$$

The transformer T is implemented by using the magnetic core TDK EE-55 with primary turns n_p = 16 and secondary turns n_s = 2. Therefore, the actual voltage gains at 200 V and 400 V input cases are rewritten as.

$$G_{ac,max} = n_pV_o/n_sV_{in} = 1.92 \quad (7)$$

$$G_{ac,min} = n_pV_o/n_sV_{in} = 0.96 \quad (8)$$

According to the winding turns and the load resistor at full load, $R_{e,ac}$ is calculated in Equation (9).

$$R_{e,ac} = 2(n_p/n_s)^2R/\pi^2 \approx 60\ \Omega \quad (9)$$

It is assumed the quality factor $x = \sqrt{L_r/C_r}/R_{ac} = 0.1$. Then, L_r can be derived in Equation (10).

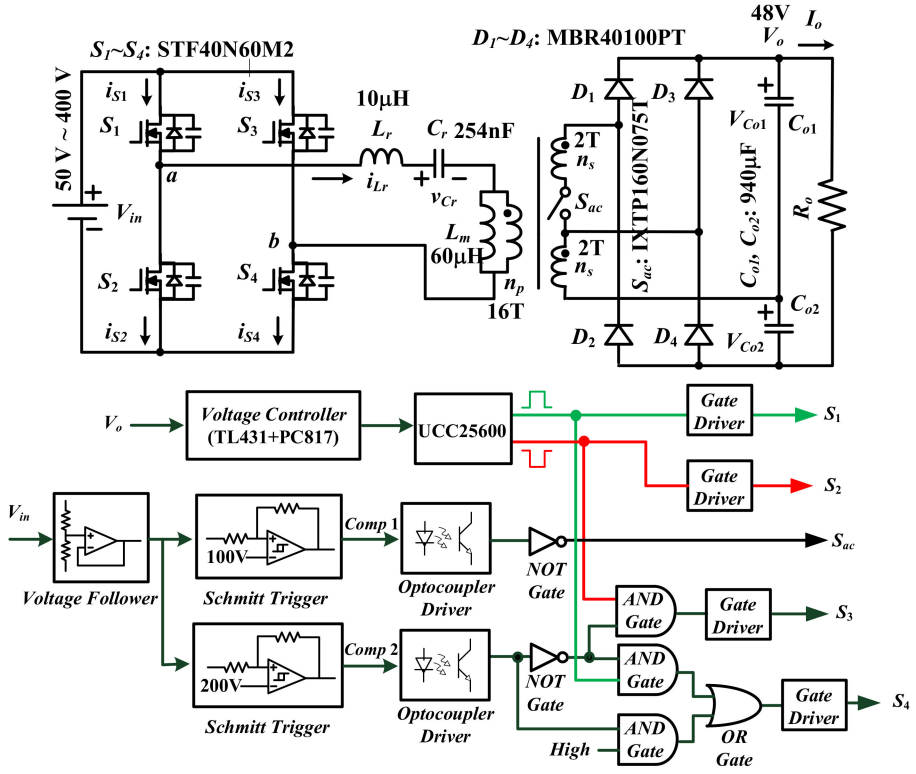
$$L_r = xR_{e,ac}/(2\pi f_r) \approx 10\ \mu\text{H} \quad (10)$$

From the given inductance ratio $L_m/L_r = 6$, L_m is calculated as $L_m = 6 \times L_r = 60\ \mu$H. The series resonant capacitance C_r is expressed in Equation (11).

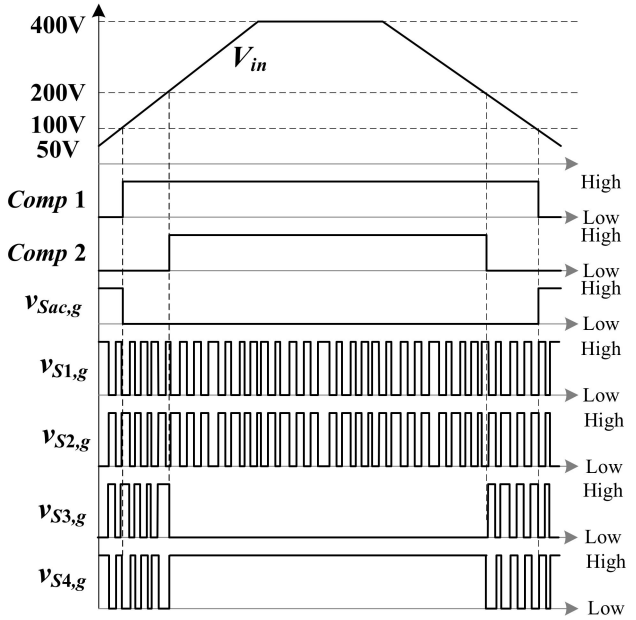
$$C_r = 1/(4\pi^2L_rf_r^2) \approx 254\ \text{nF} \quad (11)$$

The maximum voltage rating of S_1–S_4 equals $V_{in,max}$ (= 400 V). The voltage rating of D_1–D_4 is equal to V_o (= 48 V). Power switches STF40N60M2 (650 V/22 A) are used for S_1–S_4 and switch IXTP160N075T (75 V/160 A) is used for S_{ac} in the prototype circuit. Power diodes MBR40100PT (100 V/40 A) are adopted in the prototype for the rectifier diodes D_1–D_4. The selected capacitances C_{o1} and C_{o2} are 940 μF with 100 V voltage rating. The control block of a laboratory prototype is shown in Figure 7a. Two Schmitt voltage comparators (comp 1 and comp 2) with reference voltages at 100 V and 200 V are used to select three input voltage regions. The control unit of the converter is using the integrated

circuit UCC25600. The logic gates such as AND and OR gates are used to generate the control PWM signals of S_{ac}, S_3 and S_4. The relationship between the PWM signals of power switches and the input voltage is provided. It can observe that S_{ac} is always ON and S_1–S_4 are active if 50 V < V_{in} < 100 V. If 200 V > V_{in} > 100 V, S_{ac} is always OFF and S_1–S_4 are active. When V_{in} > 200 V, S_{ac} and S_3 are always OFF, S_4 is always ON, and S_1 and S_2 are active.



(**a**)



(**b**)

Figure 7. Laboratory prototype: (**a**) circuit diagram and control block; (**b**) control signal and input voltage.

4. Experimental Results

The experimental waveforms are provided to confirm the effectiveness of the presented resonant converter. Figures 8–10 gives the experimental results of PWM signals of S_1–S_4 for low, medium and high input voltage regions, respectively. For low voltage region operation, S_{ac} always turns on, the $2n_s$ secondary turns are connected to load and diodes D_3 and D_4 are the reverse biased. The gating signals $v_{S1,g}$–$v_{S4,g}$ under 50 V and 90 V input conditions are provided in Figure 8a,b. The converter operated at V_{in} = 50 V condition has the low switching frequency compared to 90 V input condition. Figure 8c,d provide the test waveforms of S_1 at 20% and 100% output power under 50 V input condition. Similarly, the test waveforms of S_1 at 20% and 100% output power under 90 V input condition are provided in Figure 8e,f. One can observe the switch S_1 is tuned on at zero voltage switching for both 50 V and 90 V input conditions from 20% output power. Power switches S_2–S_4 have the similar switching characteristics as switch S_1. Thus, the soft switching turn-on of S_1–S_4 can be achieved under low voltage input region. In the same manner, the measured results of S_1–S_4 for medium and high voltage input regions are shown in Figures 9 and 10, respectively. For high voltage input region, the half bridge *LLC* resonant converter is activated and controlled. Thus, S_3 and S_4 are always turn-off and turn-on as shown in Figure 10a,b, respectively. Figure 11 gives the test waveforms v_{ab}, v_{Cr} and i_{Lr} at V_{in} = 50 V, 110 V, 190 V and 400 V conditions. In the same manner, the experimental results of the rectifier diode currents, load voltage and load current at V_{in} = 50 V, 110 V, 190 V and 400 V conditions are shown in Figure 12. For 50 V input case, the studied converter is controlled at low voltage input region and S_{ac} is turned on. The turns-ratio of transformer T is $n_p/2n_s$. Diodes D_3 and D_4 are off. Since the studied circuit has much more voltage gain at V_{in} = 50 V than V_{in} = 100 V, the circuit operated at V_{in} = 50 V has less switching frequency. It can observe that D_1 and D_2 turn off without the reverse recovery current loss shown in Figure 12a. For V_{in} = 110 V (Figure 12b) and 190 V (Figure 12c) conditions, the circuit is operation in medium input voltage range. S_{ac} is in the off-state and the transformer turns-ratio is n_p/n_s. Diodes D_1 and D_2 are inactive. The voltage gain of the converter operated at V_{in} = 110 V is greater than V_{in} = 190 V condition. Therefore, the switching frequency at 110 V input (Figure 11b is less than 190 V input condition (Figure 11c). Since f_{sw} (switching frequency) at 110 V input is lower than f_r (resonant frequency), D_3 and D_4 are turned off under zero-current switching shown in Figure 12b. For V_{in} = 400 V input, the resonant converter is operation at high voltage input region. S_3 and S_{ac} are always turn-off and switch S_4 is always in the on-state. One can observe there is a dc voltage value ($V_{in}/2$ = 200 V) on voltage v_{Cr} shown in Figure 11d. Owing to $f_{sw} > f_r$ at 400 V input, D_3 and D_4 are turned off with hard switching shown in Figure 12d. The experimental results of V_{in}, $V_{Co}1$, $V_{Co}2$ and I_o for different input voltage conditions are provided in Figure 13. It observes that $V_{Co}1$ and $V_{Co}2$ are balanced well each other under different input voltage conditions. Figure 14a gives the measured input voltage V_{in}, the gating voltage $v_{Sac,g}$ and output voltage V_o between 50 V (low voltage region)–130 V (medium voltage region) input. When V_{in} is lower or greater than 100 V, S_{ac} turns on (low input voltage range) or off (medium input voltage range). Figure 14b gives test waveforms of V_{in}, $v_{S3,g}$ and $v_{S4,g}$ between V_{in} = 0 V and 250 V. If V_{in} is lower (or greater) than 200 V, S_3 is active (or always turn-off) and S_4 is active (or always turn-on). The test PWM signals of S_3, S_4 and S_{ac} and input voltage V_{in} shown in Figure 14 are agreed with the theoretical waveforms shown in Figure 7.

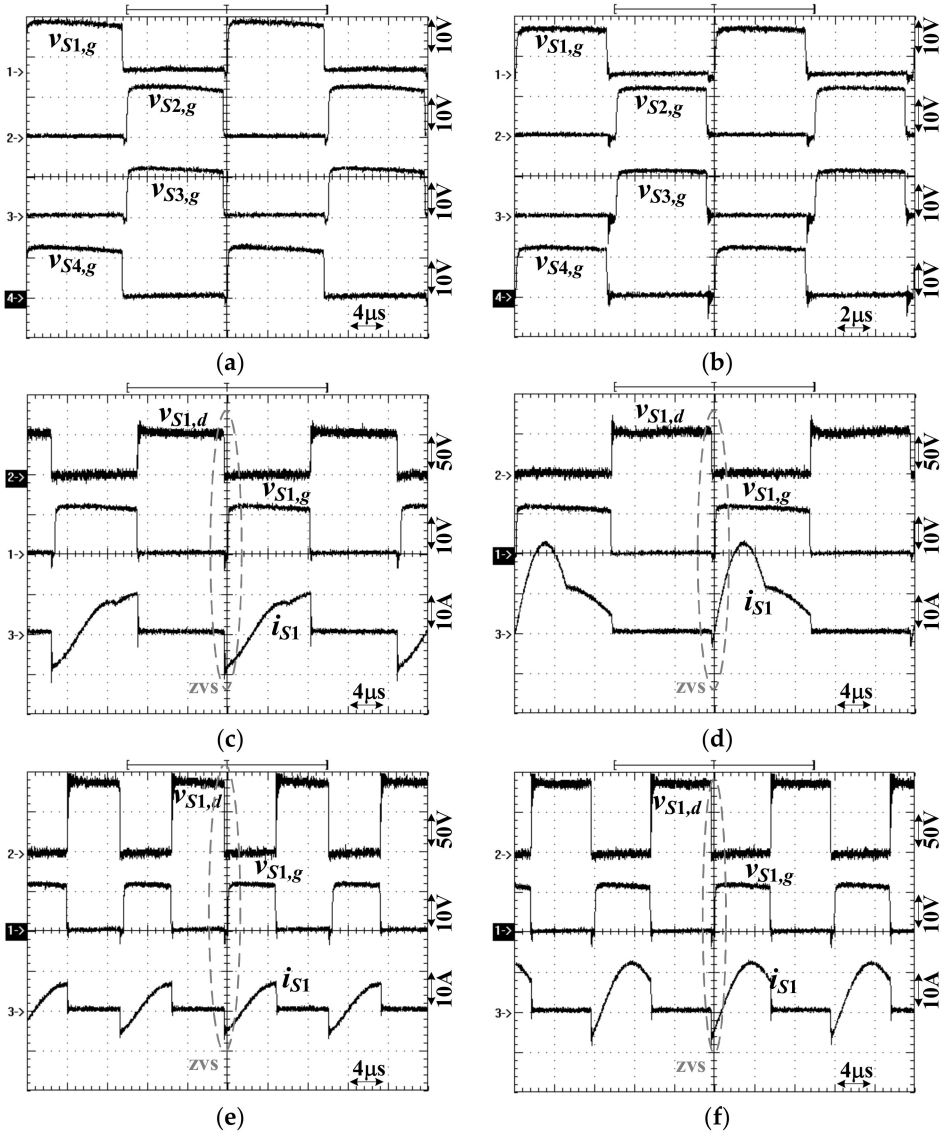


Figure 8. Experimental results of PWM signals for low input voltage region: (**a**) S_1–S_4 at 50 V input and 100% power; (**b**) S_1–S_4 at 90 V input and 100% power; (**c**) S_1 voltage and current at 50 V input and 20% power; (d) S_1 voltage and current at V_{in} = 50 V input and 100% power; (**e**) S_1 voltage and current at 90 V input and 20% power; (**f**) S_1 voltage and current at 90 V input and 100% power.

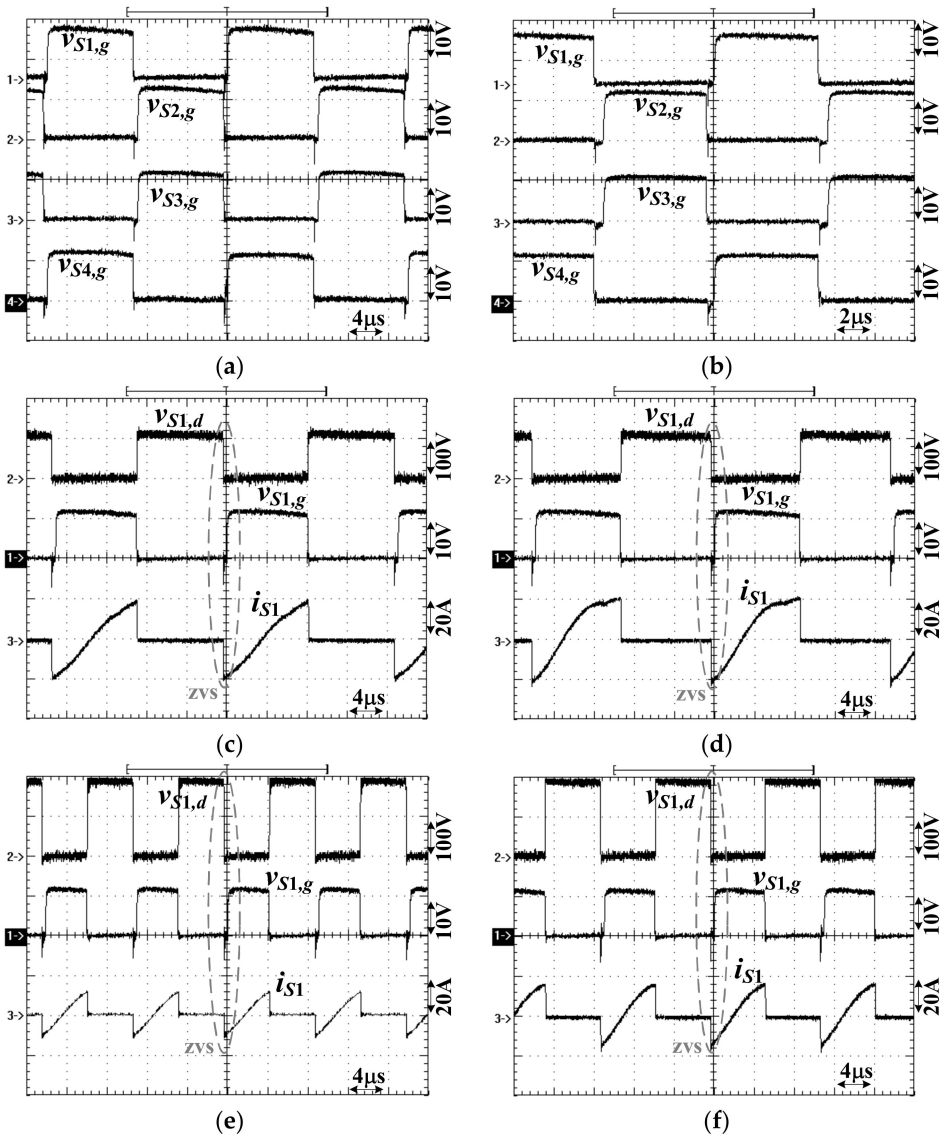


Figure 9. Experimental results of PWM signals for medium input voltage region: (**a**) S_1–S_4 at 110 V input and 100% power; (**b**) S_1–S_4 at 190 V input and 100% power; (**c**) S_1 voltage and current at 110 V input and 20% power; (**d**) S_1 voltage and current at V_{in} = 110 V input and 100% power; (**e**) S_1 voltage and current at 190 V input and 20% power; (**f**) S_1 voltage and current at 190 V input and 100% power.

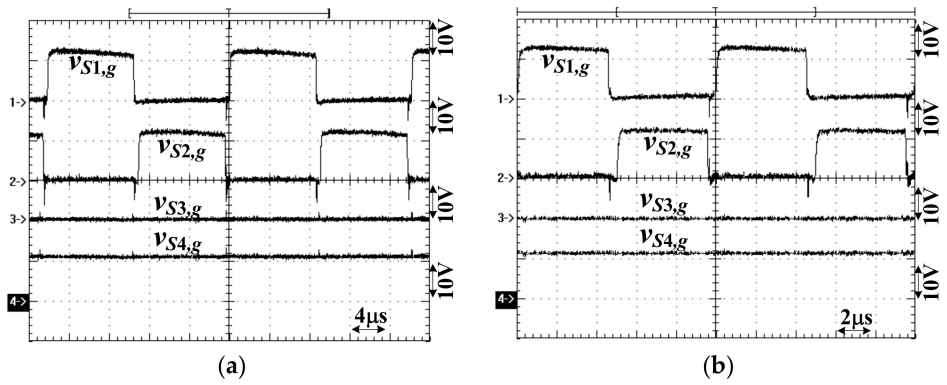


Figure 10. *Cont*.

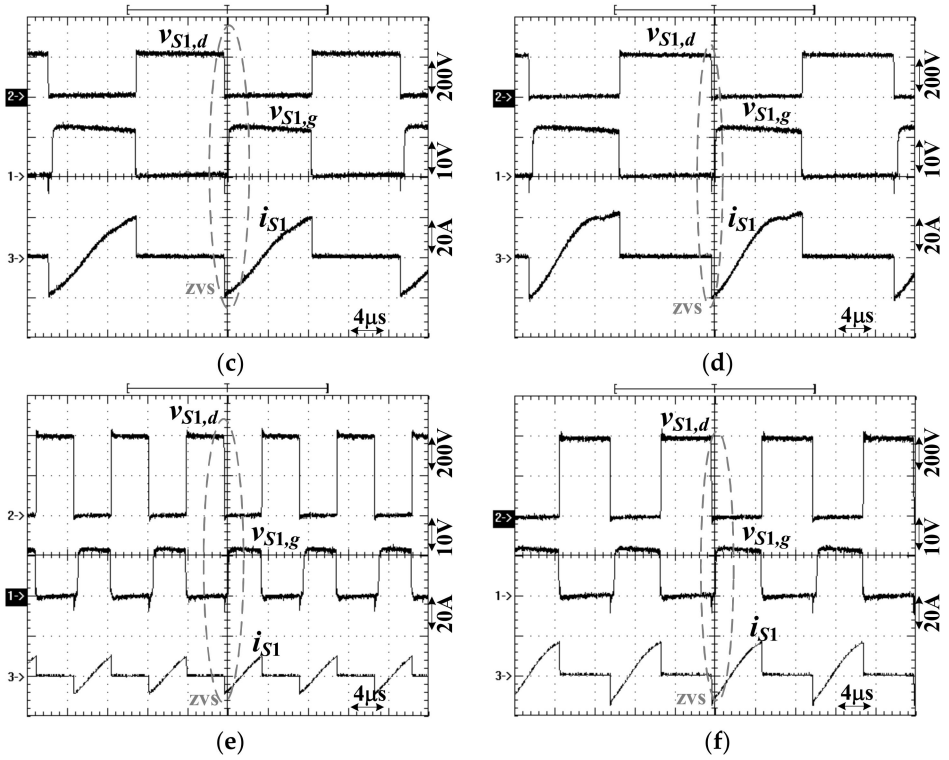


Figure 10. Experimental results of PWM signals for high input voltage region: (**a**) S_1–S_4 at 210 V input and 100% power; (**b**) S_1–S_4 at 400 V input and 100% power; (**c**) S_1 voltage and current at 210 V input and 20% power; (**d**) S_1 voltage and current at V_{in} = 210 V input and 100% power; (**e**) S_1 voltage and current at 400 V input and 20% power; (**f**) S_1 voltage and current at 400 V input and 100% power.

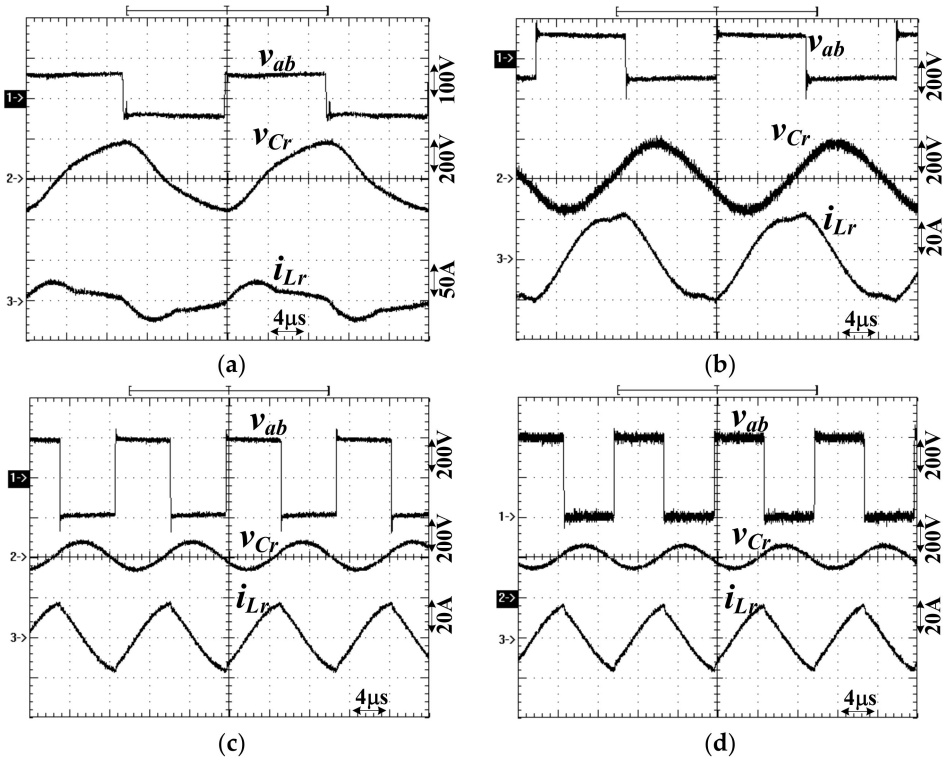


Figure 11. Measured primary-side voltage and current waveforms at 100% load: (**a**) 50 V input (low voltage range); (**b**) 110 V input (medium voltage range); (**c**) 190 V input (medium voltage range); (**d**) 400 V input (high voltage range).

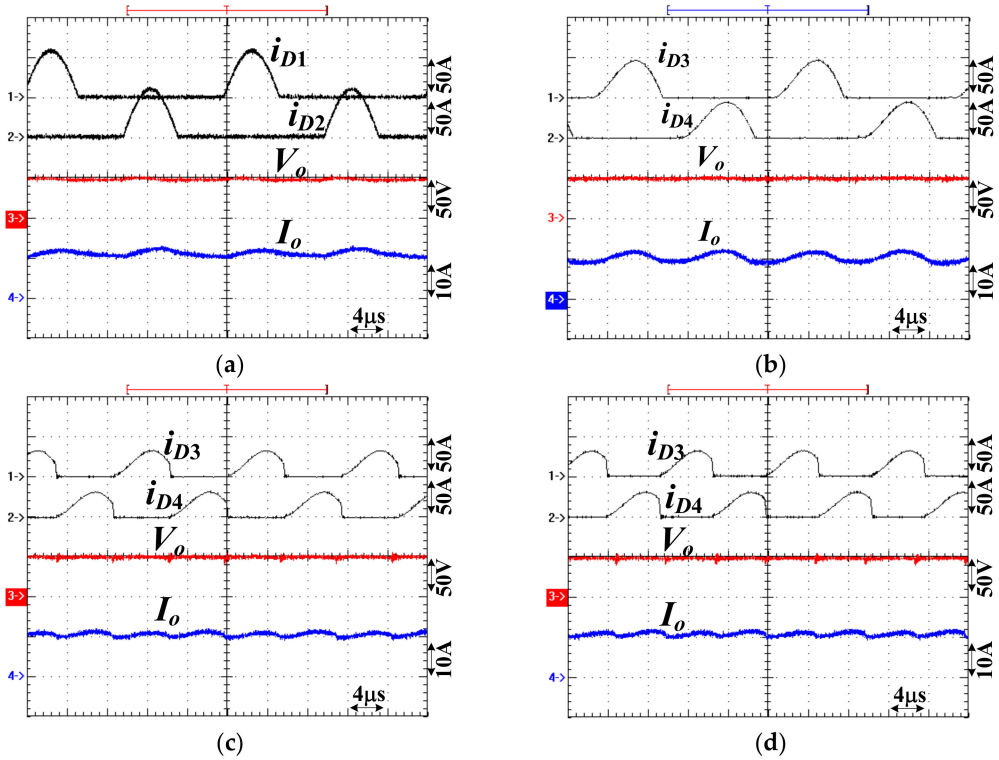


Figure 12. Experimental results of the secondary-side currents and load voltage at 100% load; (**a**) 50 V input (low voltage range); (**b**) 110 V input (medium voltage range); (**c**) 190 V input (medium voltage range); (**d**) 400 V input (high voltage range).

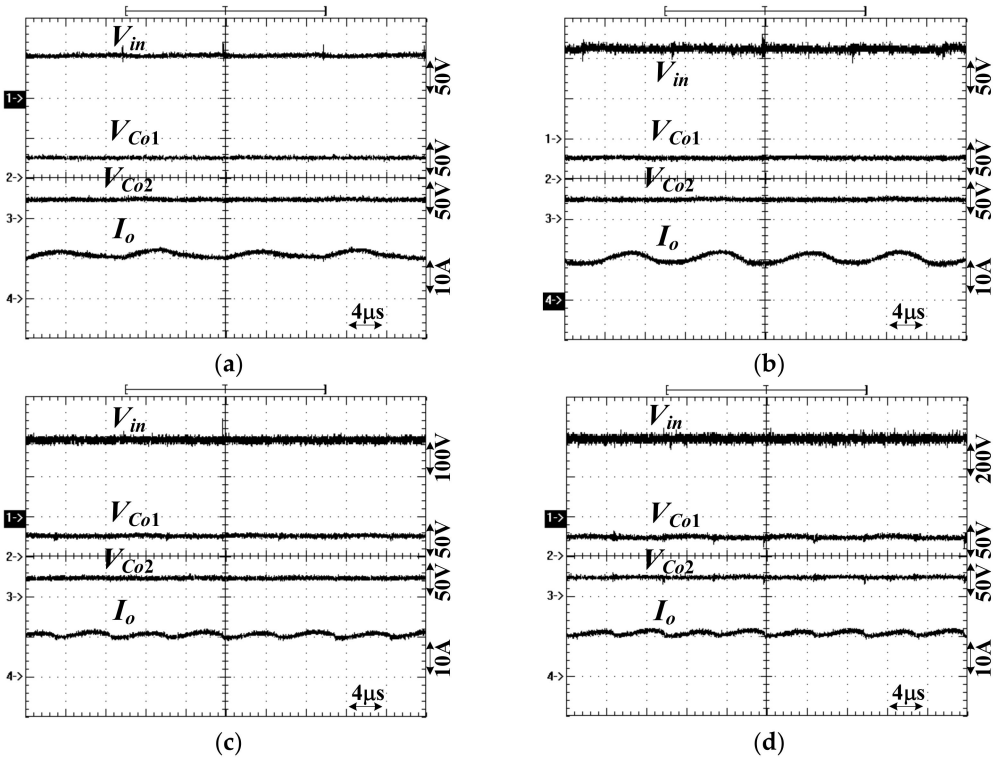


Figure 13. Measured results of V_{in}, V_{Co1}, V_{Co2} and I_o at 100% load: (**a**) 50 V input (low voltage range); (**b**) 110 V input (medium voltage range); (**c**) 190 V input (medium voltage range); (**d**) 400 V input (high voltage range).

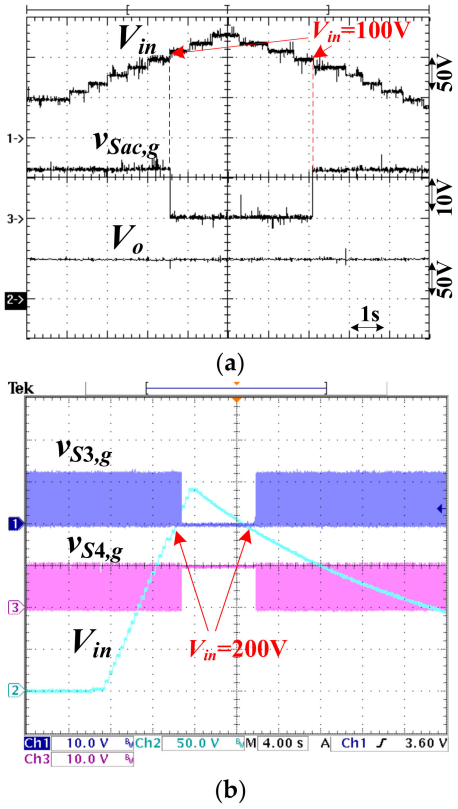


Figure 14. Measured waveforms: (**a**) V_{in}, v_{Sac} and V_o; (**b**) V_{in}, $v_{S3,g}$ and $v_{S4,g}$.

5. Conclusions

The hybrid *LLC* converter with three equivalent sub-circuit topologies is proposed and discussed to realize wide soft switching turn-on and wide voltage input operation. According to the switching status of power devices, the full bridge and half bridge *LLC* circuit with variable transformer turn-ratio are operated to accomplish wide voltage operation (V_{in} = 50–400 V). Owing to the *LLC* circuit tank, power switches have soft switching characteristic at turn-on instant. The presented resonant converter can be applied to dc-dc converters with wide voltage variation capability such as power units in PV power converters, power servers with large hold-up times and battery chargers and dischargers. The experimental results are demonstrated and provided to confirm the effectiveness of the adopted circuit topology.

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