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Numerical Simulation Analysis of Switching Characteristics in the Source-Trench MOSFET's

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Abstract: In this paper, we compare the static and switching characteristics of the 4H-SiC conventional UMOSFET (C-UMOSFET), double trench MOSFET (DT-MOSFET) and source trench MOSFET (ST-MOSFET) through TCAD simulation. In particular, the effect of the trenched source region and the gate trench bottom P+ shielding region on the capacitance is analyzed, and the dynamic characteristics of the three structures are compared. The input capacitance is almost identical in all three structures. On the other hand, the reverse transfer capacitance of DT-MOSFET and ST-MOSFET is reduced by 44% and 24%, respectively, compared to C-UMOSFET. Since the reverse transfer capacitance of DT-MOSFET and ST-MOSFET is superior to that of C-UMOSFET, it improves high frequency figure of merit (HF-FOM: $R_{ON\text{-}SP} \times Q_{GD}$). The HF-FOM of DT-MOSFET and ST-MOSFET is 289 mΩ·nC, 224 mΩ·nC, respectively, which is improved by 26% and 42% compared to C-UMOSFET. The switching speed of DT-MOSFET and ST-MOSFET are maintained at the same level as the C-UMOSFET. The switching energy loss and power loss of the DT-MOSFET and ST-MOSFET are slightly improved compared to C-UMOSFET.

Keywords: 4H-SiC; double trench; energy loss; reverse transfer capacitance; source trench; switching

1. Introduction

4H-SiC MOSFETs are widely considered to be the leading next-generation power semiconductor devices due to their superior material properties, such as high critical electric field, high thermal conductivity, and ability to operate at high temperatures [1,2]. Of the various SiC MOSFET structures, gate-trench MOSFETs (UMOSFETs) typically have lower on-state resistance compared to planar MOSFETs (VDMOSFETs). In addition, UMOSFETs have higher channel density and mobility than VDMOSFETs due to their ability to form vertical channels on the trench sidewalls and their ability to reduce cell pitch [3–7]. However, there are two main drawbacks to UMOSFETs. First, they have a relatively large reverse transfer capacitance (C_{rss}). For high-frequency applications, devices must have a small Miller plateau (Q_{GD}) and C_{rss} [8]. Since Q_{GD} and C_{rss} are determined by the overlap between the gate and the drain, the gate-trench structure has a relatively large C_{rss}. As such, it is necessary to reduce the device C_{rss} to ensure high power efficiency and low energy loss in high frequency operations. The second problem with UMOSFETs is the appearance of gate oxide reliability issues that arise from the gate oxide at the bottom of the trench when UMOSFET operates in the off-state. Because SiC, a wide bandgap material, has a small offset between the conduction band and the valance band with respect to the SiC and the gate oxide, Fowler Nordheim tunneling (FN tunneling) will occur in the electric field (generally over 3 MV/cm) smaller than Si (~6 MV/cm). This FN tunneling current leads to oxide degradation [9–11]. Therefore, in the case of SiC UMOSFETs, it is very important to suppress electric field crowding at the gate oxide edge. To address this problem, a structure which includes a gate trench bottom P+ shielding region (BPR) has been proposed [12–15]. Various other structures have been proposed additionally to reduce the electric field of the gate oxide [16–19]. Infineon's CoolSiC

and Rohm's Double Trench structure were also commercialized at a 1.2 kV class [20–22]. Among them, the double trench structures have been most actively studied in recent years with regard to their dynamic properties and reliability [23–25]. In the case of the double trench structure, the source region and gate are both trenched. As a result, the electric field is not concentrated in the gate trench region. As a variant of the double trench, a source trench structure for distributing the electric field through thermally grown oxide has been proposed [26]. However, the dynamic characteristics of the 1700 V source trench MOSFET structure have not been actively discussed. In this study, we researched the switching characteristics of the 1700 V UMOSFET, Double Trench MOSFET (DT-MOSFET), and Source Trench MOSFET (ST-MOSFET) structures.

2. Device Structures

Figure 1 shows the three structures considered in this paper. Figure 1a is the conventional UMOSFET (C-UMOSFET), and Figure 1b,c are DT-MOS and ST-MOS, respectively. The device parameters of each structure have been optimized for static characteristics while the BPR is grounded. In addition, a depletion stopping layer (DSL) [27], also known as a current spreading layer (CSL) [28,29], is added. The DSL improves the on-state characteristics by suppressing the expansion of the depletion region in the JFET region. The cell pitch of each structure is 5.55 µm, and the total thickness of the epi-layer is 18 µm. The thickness of the BPR is 0.3 µm, and the gate trench width and depth are 1.55 µm and 1.5 µm, respectively. In the case of DT-MOS, the source trench width is 0.5 um, the depth is 1.5 µm, and the thickness of the P+ shielding region of the source trench is 0.3 µm. In the case of ST-MOS, the source trench width is 0.5 µm, the depth is 2.4 µm, and the source oxide thickness is 0.1 µm. In addition, the concentration of the epi layer of each structure is 3×10^{15} cm^{-3}, 5×10^{15} cm^{-3}, and 5×10^{15} cm^{-3} for C-UMOS, DT-MOS, and ST-MOS, respectively. Additional device parameters are listed in Table 1.

In the next section, the characteristics of each structure are described. Static characteristics were simulated using Synopsys TCAD, and dynamic characteristics were analyzed through mixed mode simulation [30]. Electron/hole continuity equations and Poisson equation are solved with Shockley–Read–Hall recombination and Auger recombination model. The doping dependency, high field velocity saturation and mobility degradation are included in the mobility model. In particular, the Lombardi model was considered for the interface that affects the channel mobility [31]. Bandgap narrowing, anisotropic material properties, and incomplete ionization effects of each structure were considered [32,33].

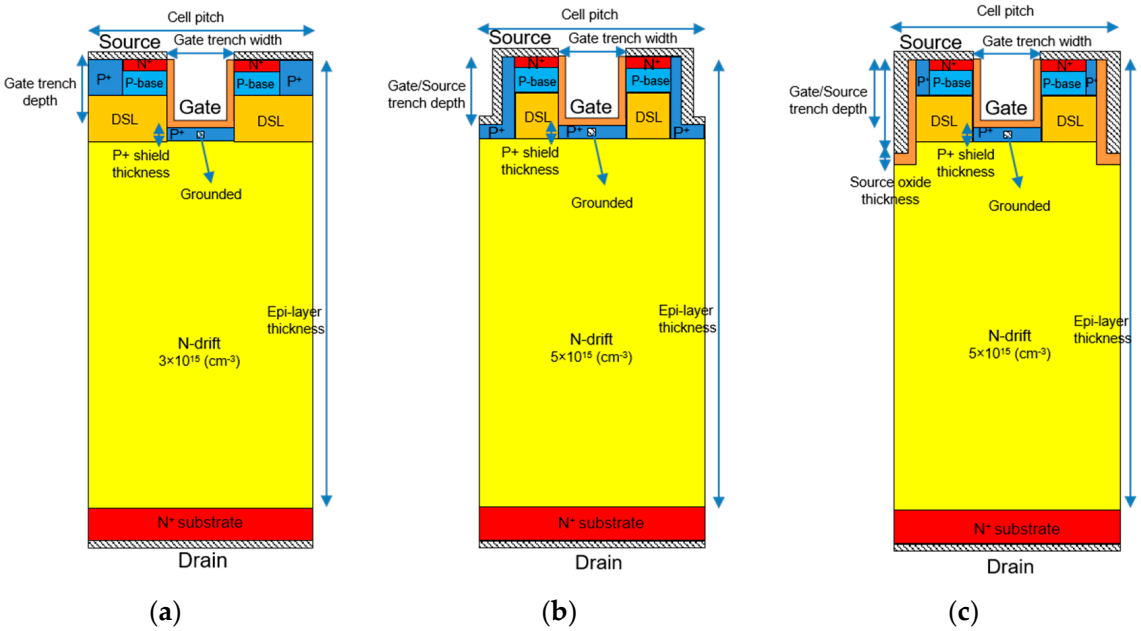

Figure 1. Schematic cross-sectional view of (**a**) C-UMOSFET, (**b**) DT-MOSFET, and (**c**) ST-MOSFET.

Table 1. Device parameter of each structure.

Parameter	C-	DT-	ST-
Cell pitch (μm)	5.55	5.55	5.55
Gate-trench width (μm)	1.55	1.55	1.55
Gate-trench depth (μm)	1.5	1.5	1.5
P-base width (μm)	2	2	2
P+ shield width (μm)	1.55	1.55	1.55
Channel length (μm)	0.5	0.5	0.5
Gate oxide thickness (μm)	0.05	0.05	0.05
Epi-layer thickness (μm)	18	18	18
P+ shield thickness (μm)	0.3	0.3	0.3
N-sub thickness (μm)	1	1	1
Source-trench width (μm)	-	0.5	0.5
Source-trench depth (μm)	-	1.5	2.4
Source oxide thickness (μm)	-	-	0.1
Source doping concentration (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
P-base doping concentration (cm^{-3})	1×10^{17}	1×10^{17}	1×10^{17}
P+ shield doping concentration (cm^{-3})	5×10^{18}	5×10^{18}	5×10^{18}
Epi-layer doping concentration (cm^{-3})	3×10^{15}	5×10^{15}	5×10^{15}
N-sub doping concentration (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}
DSL doping concentration (cm^{-3})	1×10^{16}	1×10^{16}	1×10^{16}

3. Results and Discussion

3.1. Static Characteristics

First, in order to facilitate normalization, the active area was assumed to be 1 cm^2, and simulation of static characteristics was performed. Figure 2 shows the off-state characteristic curves of the three structures. The breakdown voltages are 1699 V, 1706 V, and 1724 V for each C-UMOSFET, DT-MOSFET and ST-MOSFET, respectively. Figure 3 shows the breakdown voltage when the doping concentration of the epi-layer of each structure is varied. Each structure is designed to have the breakdown voltage close to 1700 V by controlling the doping concentration of the epi-layer. Figure 4 shows the on-state characteristic curves of the three structures when the gate voltage is 15 V. Figure 4a is the on-state characteristic curves of the linear region with the drain voltage range of 0–25 V, and b is the overall on-state characteristic curves with the drain voltage range of 0–800 V. In Figure 4a, the specific on-resistance at a low V_D of the C-UMOSFET, DT-MOSFET, and ST-MOSFET are 3.37 mΩ·cm^2, 3.57 mΩ·cm^2, and 2.52 mΩ·cm^2 (at V_G = 15 V and I_D = 20 A), respectively. From Figure 4b, the quasi-saturation current [34] was highest for C-UMOSFET and lowest for DT-MOSFET. Due to the trenched source region, the width of the JFET region of the DT-MOSFET and ST-MOSFET is smaller than that of the C-UMOSFET. Since the current path decreases in proportion to the JFET width, the quasi-saturation current of DT-MOSFET and ST-MOSFET is reduced compared to the C-UMOSFET. The FOM ($BV^2/R_{on\text{-}sp}$) [35], which represents the trade-off relationship of static characteristics, was calculated as 856.6 MW/cm^2, 815.2 MW/cm^2, and 1179.4 MW/cm^2 for the three structures, C-UMOSFET, DT-MOSFET, and ST-MOSFET, respectively.

Figure 5 shows the off-state gate oxide electric field distributions of each structure when V_G = 0 V and V_D = 1200 V. The maximum gate oxide electric field ($E_{ox\text{-}max}$) is 1.1 MV/cm for the C-UMOSFET, 0.6 MV/cm for the DT-MOSFET, and 0.7 MV/cm for the ST-MOSFET. The grounded BPR applied to all three structures effectively blocks the electric field at gate oxide, reducing the $E_{ox\text{-}max}$. In the case of the DT-MOSFET and ST-MOSFET, not only the BPR but also the trenched source region disperses the electric field applied to the gate oxide, further reducing the $E_{ox\text{-}max}$. Figure 6 shows the transfer characteristic curves of the three structures at V_D = 20 V. As shown, at the same given gate voltage, the current handling capability varies with the JFET width. The wider the JFET width, the larger the drain current at the same gate voltage. Furthermore, the threshold voltages (Vth) calculated at V_D = 20 V and I_D = 1 A are 5.74 V, 5.75 V, and 5.75 V for each structure. Since the doping concentration and depth of the P-base were kept constant, there was little Vth shift. The overall static performance of the three structure is

summarized in Table 2. Figure 7a shows the change in the threshold voltage of each structure as the temperature varies, and the threshold voltage shows the negative temperature coefficient [36]. As the lattice temperature increases from 300 K to 500 K, the threshold voltage decreases due to the increase in intrinsic carrier concentration [37]. In all three structures, the threshold voltage at 500 K decreases by nearly 24% compared to the value at 300 K. Figure 7b shows the specific on-resistance versus temperature. As seen in Figure 7b, the DT-MOSFET is the least temperature dependent, increasing by approximately 140% at 500 K, with respect to its on-resistance at 300 K. For the ST-MOSFET and C-UMOSFET, the on-resistance at 500 K increases by 160% and 180%, respectively, compared to the on-resistance at 300 K.

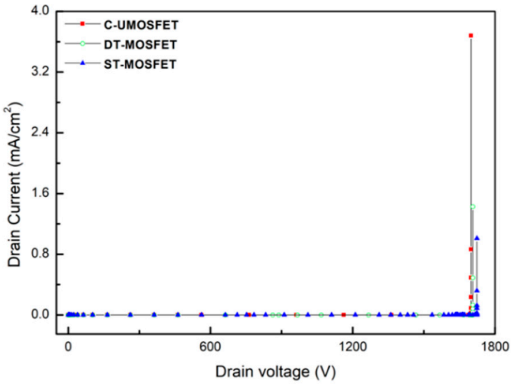

Figure 2. Off-state breakdown characteristic cures of each structure.

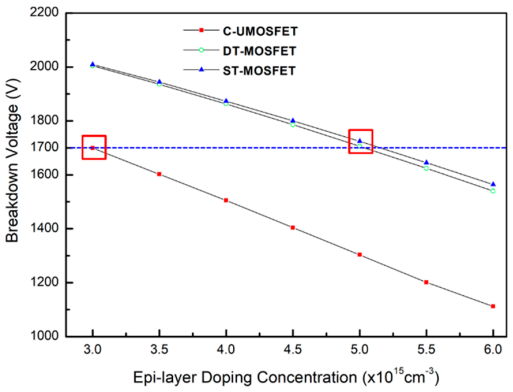

Figure 3. Variation of breakdown voltage of each structure with epi-layer doping concentration.

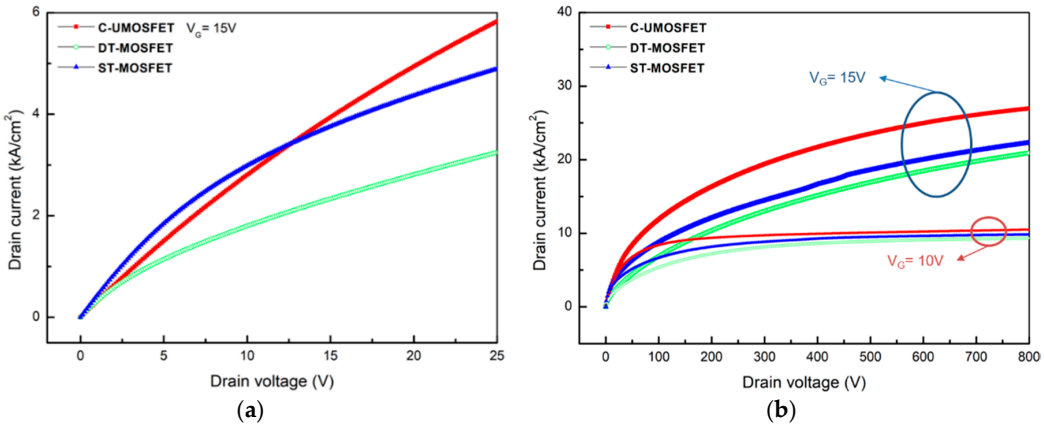

Figure 4. (**a**) On-state output characteristic curves in the linear region of each structure with the drain voltage range of 0–25 V and (**b**) Overall on-state output characteristic curves of each structure with the drain voltage range of 0–800 V.

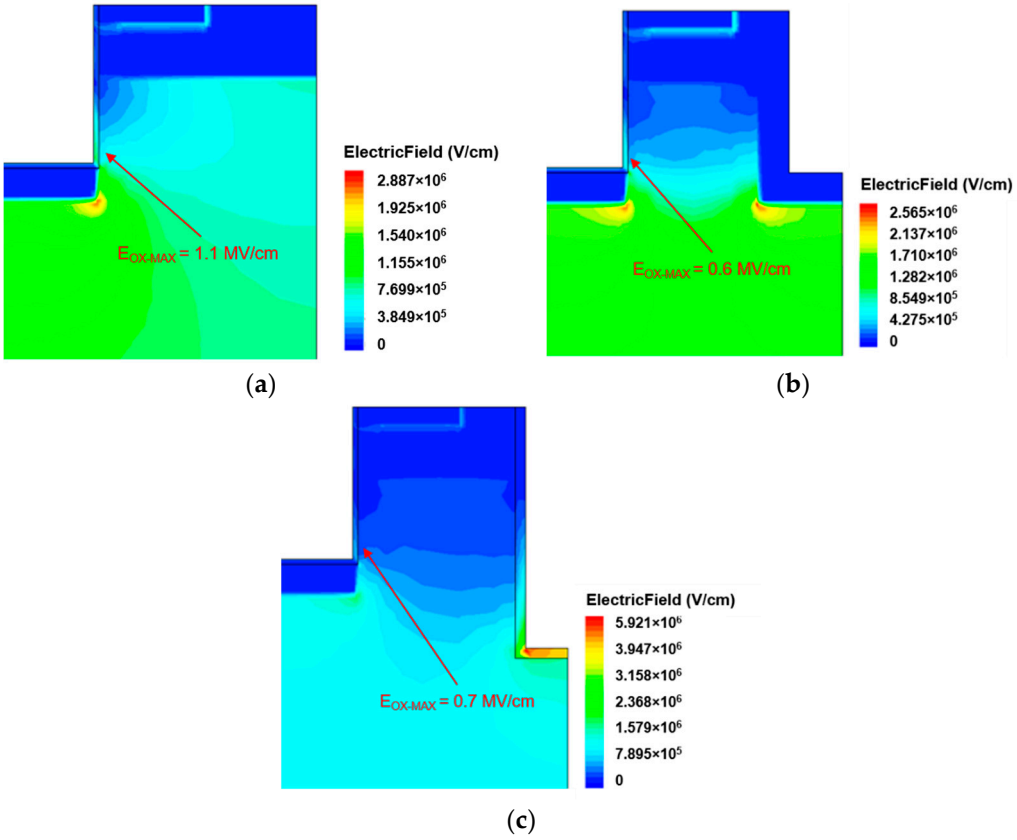

Figure 5. Off-state gate oxide electric field distribution of (**a**) C-UMOSFET, (**b**) DT-MOSFET, and (**c**) ST-MOSFET at V_D = 1200 V.

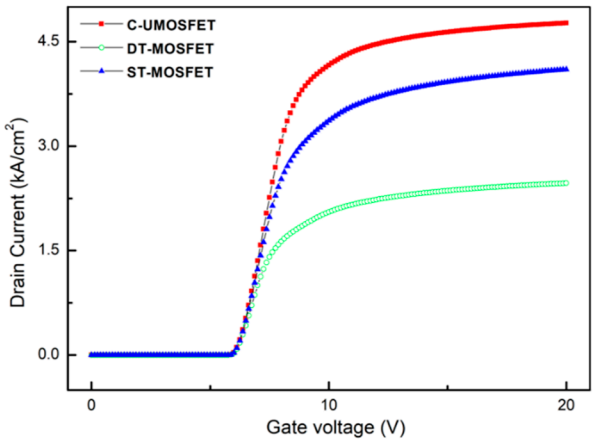

Figure 6. Transfer characteristics of each structure at V_D = 20 V.

Table 2. Static performance of each structure.

Parameter	C-	DT-	ST-
Breakdown voltage [V]	1699	1706	1724
$R_{ON\text{-}SP}$ [mΩ·cm^2]	3.37	3.57	2.52
$E_{OX\text{-}MAX}$ (@VG = 0 V, VD = 1200 V) [MV/cm]	1.11	0.62	0.72
V_{TH} [V]	5.74	5.75	5.75
DC-FOM (BV^2/$R_{ON\text{-}SP}$) [MW/cm^2]	857	815	1179

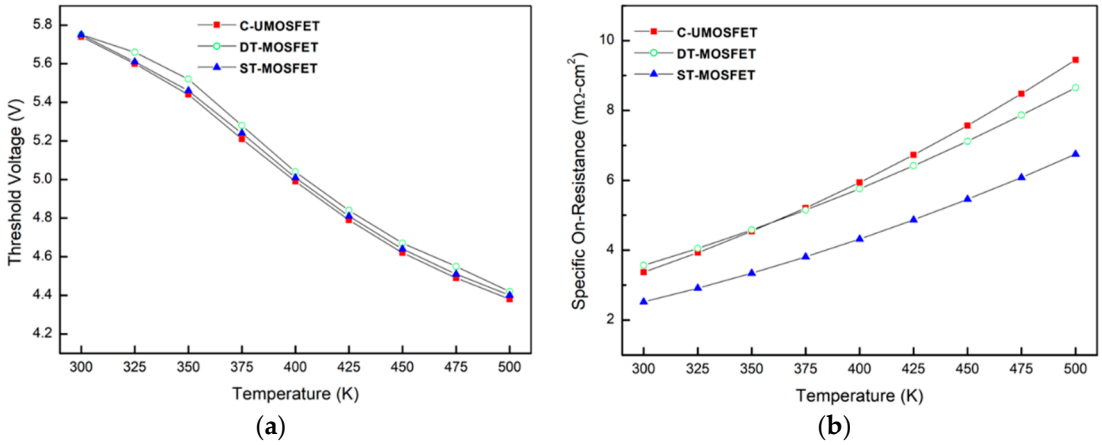

Figure 7. (**a**) Threshold voltage versus temperature of each structure taken at V_D = 20 V and I_D = 1 A; (**b**) Specific on-resistance versus temperature of each structure taken at V_G = 15 V and I_D = 20 A.

3.2. Terminal Capacitance Characteristics

In this section, the simulation conditions for capacitance extraction are set such that the active area is 1 cm^2, the ac small signal is 1 MHz, the gate voltage is fixed at 0 V, and the drain voltage sweeps from 0–600 V. Before analyzing the terminal capacitance of the three structures, the effect of BPR on the capacitance was analyzed. Figure 8 shows the capacitance for both ground and floating BPR and for DSL in the C-UMOSFET. The grounded BPR in contact with the source increases the overlapping area between the gate and the source. Thus, in the case of the grounded BPR, the input capacitance (C_{iss}:C_{iss} = C_{GS} + C_{GD}) is higher than that when no BPR is used or when a floating BPR is applied. However, the floating BPR causes dynamic degradation due to its charge storage mechanism [38], and when no BPR is applied to the C-UMOSFET, there is increased degradation of the dynamic characteristics due to hot hole injections that arise from the high electric field in the gate oxide [24]. On the other hand, in the case of grounded BPR, C_{rss}, which plays the most important role in switching energy loss, is effectively reduced. The grounded BPR blocks the electric field between the bottom gate and the drain and screens the charge coupling [38]. Therefore, only the capacitance between the side gate oxide and the drain contributes to the C_{rss} [12]. When the DSL is added, the C_{rss} is nearly identical as when the ground BPR is applied, excluding a slight increase at low drain voltages.

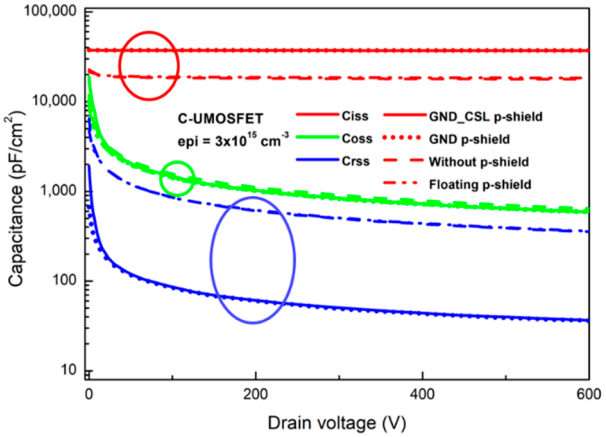

Figure 8. Terminal capacitance of C-UMOSFET. The effect of BPR and DSL on the capacitance is observed.

In the UMOSFET structure, the gate-drain capacitance (C_{GD} or C_{rss}) is the series connection between the gate oxide capacitance and the depletion capacitance. According to a previous study on the modeling of gate-drain capacitance in UMOSFET structures, the equation for C_{GD} is as follows [39,40]:

$$C_{GD} = \left(\frac{t_W + 2t'_D}{t_{cell}}\right)\left[\frac{C_{GOX}C_D}{C_{GOX} + C_D}\right] \quad (1)$$

where t'_D is the trench depth not overlapping the p-base region, t_W is the trench width, t_{cell} is the cell pitch, C_{ox} is the gate oxide capacitance, and C_D is the depletion capacitance. However, in the case of a structure in which the source region is trenched, such as DT-MOSFETs and ST-MOSFETs, it is difficult to intuitively analyze the C_{GD} due to the geometric complexity of the structure. Recently, X. Luo et al. [40] illustrated that the C_{GD} operates as a serial connection between the gate-source capacitance and the drain-source capacitance. The gate-drain capacitance equation in Double Trench MOSFET Structure (without BPR) claimed in his paper are:

$$C_{GD} = \left({C_{GS}}^{-1} + {C_{DS}}^{-1}\right)^{-1} + C_{GD,bottom} \quad (2)$$

where C_{GS} is the gate-source capacitance, C_{DS} is the drain-source capacitance and $C_{GD,bottom}$ is the gate bottom-drain capacitance. In DT-MOSFET with BPR, $C_{GD,bottom}$ is negligible, so $C_{GD} = ({C_{GS}}^{-1} + {C_{DS}}^{-1})^{-1}$. However, this mechanism may contradict the results shown in Figure 9. Figure 9 plots the C_{GD} as function of the trench depth of the source region in the DT-MOSFET. In Figure 9, C_{GD} decreases as L (source trench depth) increases. When L increases, the overlapping area between the gate and the source increases. As such, C_{GS} increases and at the same time, the distance between the drain and the source decreases, leading to an increase in C_{DS}. So, according to (2), as L increases, C_{GD} should increase. This contradicts the simulation results in Figure 9, where C_{GD} decreases as L increases.

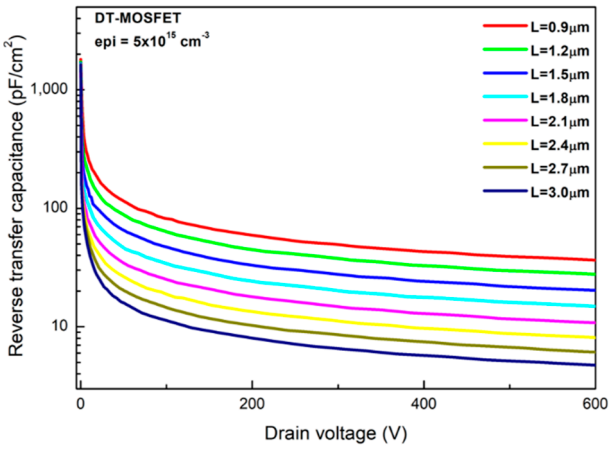

Figure 9. Reverse transfer capacitance of DT-MOSFET varying in source trench depth.

Figure 10 shows the capacitance distribution of the three structures. Depletion capacitance is considered to be the serial connection of the JFET capacitance (C_{JFET}) and the Drift capacitance (C_{Drift}). The modified gate-drain capacitance equation is given follows:

$$C_{GD} = \left({C_{OX}}^{-1} + {C_{JFET}}^{-1} + {C_{Drift}}^{-1}\right)^{-1} \quad (3)$$

Using this model, the capacitance of the trench MOSFET can be analyzed intuitively. First, the gate oxide thickness of the three structures is the same, so C_{ox} is the same. Before the depletion region is fully extended to the drift region, at a low drain voltage, the depletion regions of the DT-MOSFET and ST-MOSFET extend further than that of the C-UMOSFET due to their trenched source regions. Therefore, the C_{Drift} of DT-MOSFET and ST-MOSFET is smaller than that of C-UMOSFET. Indeed,

the DT-MOSFET has the smallest C_{Drift} of the three structures because its depletion region is wider than that of the ST-MOSFET due to the P-shielding region below the source region. In the case of the C_{JFET}, it is proportional to the JFET width. The charge in the JFET region is proportional to the JFET width, and the C_{JFET} is proportional to the charge in the JFET region. Therefore, C_{JFET} is smallest in DT-MOSFET and largest in C-UMOSFET. In addition, at a high drain voltage, the drift region is fully depleted and the C_{Drift} of the three structure is nearly the same. Thus, C_{GD} is determined by the C_{JFET}.

Figure 11 plots the terminal capacitance of the three structures. In Figure 11a, the C_{iss} of the three structures are almost the same. In the DT-MOSFET and ST-MOSFET, the trenched source region for improving the static characteristics increases the overlapping area between the gate and the source. However, as shown in Figure 12, the capacitance between the bottom gate and the BPR is the largest of all C_{GS} components, and BPR is applied to all three structures, so the C_{iss} of the three structures is not significantly different. The output capacitance (C_{oss}:C_{oss}= C_{DS} + C_{GD}), which depends on the distance between the drain and source, is also not significantly different, though the C-UMOSFET has the smallest C_{OSS}. In the case of C_{rss}, according to the previous analysis, the C_{rss} of the DT-MOSFET is the smallest, and the C_{rss} of the C-UMOSFET is the largest. At V_D = 600 V, the C_{rss} of DT-MOSFET and ST-MOSFET decreases by 44% and 24%, respectively, compared to the value of C-UMOSFET. The capacitance simulation results for each structure are shown in Table 3.

Table 3. Dynamic performance of each structure.

Parameter	C-	DT-	ST-
C_{ISS} (@V_D = 600 V, f = 1 MHz) [nF/cm^2]	37	37.3	36.2
C_{OSS} (@V_D = 600 V, f = 1 MHz) [pF/cm^2]	590	763	765
C_{RSS} (@V_D = 600 V, f = 1 MHz) [pF/cm^2]	36.5	20.3	27.7
Q_G [nC/cm^2]	839	805	813
Q_{GD} [nC/cm^2]	115	81	89
HF-FOM < $R_{ON\text{-}SP}$ × Q_G > [mΩ·nC]	2827	2874	2049
HF-FOM < $R_{ON\text{-}SP}$ × Q_{GD} > [mΩ·nC]	388	289	224

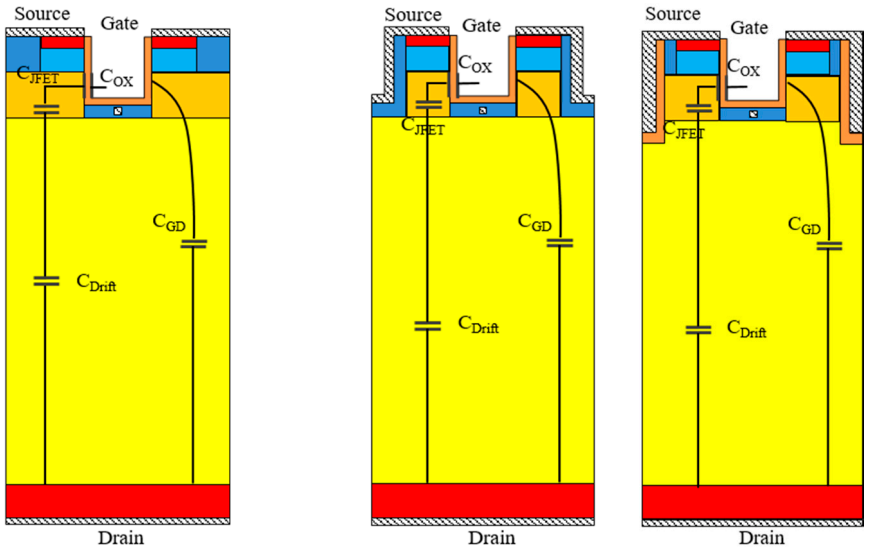

Figure 10. Capacitance distribution for (**a**) C-UMOSFET, (**b**) DT-MOSFET, and (**c**) ST-MOSFET.

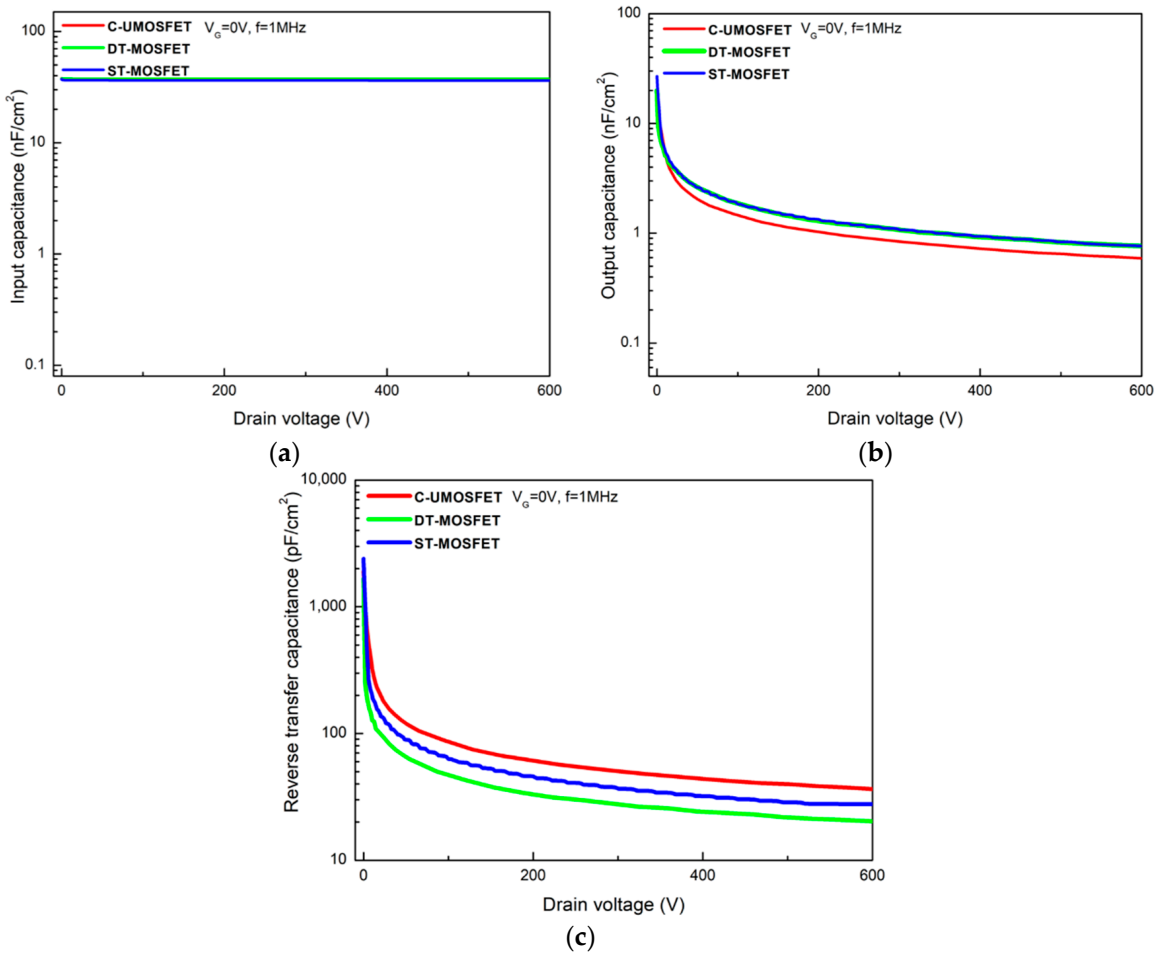

Figure 11. (**a**) Input capacitance, (**b**) output capacitance, and (**c**) reverse transfer capacitance of each structure.

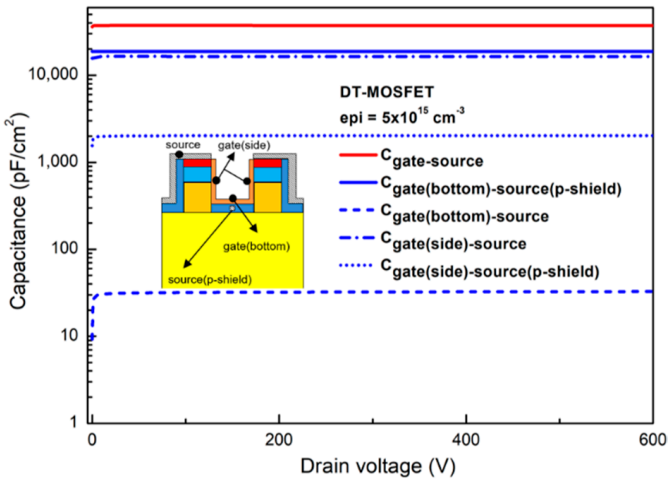

Figure 12. Gate-source capacitance distribution of DT-MOSFET.

3.3. Dynamic Charateristics

Figure 13a shows the gate charge curves of the three structures. The test circuit is shown in Figure 13b and a constant current of 100 mA is used to charge the gate. The active area of the device under test (DUT) for gate charge simulation was set to 1 cm^2. In addition, test conditions were set so that the supplying voltage (V_{DD}) was 1200 V and the load current (I_D) was 20 A. The gate-drain charge (Q_{GD} or Miller plateau) is one of the key parameters that can determine the switching speed of the device and is dependent

on C_{GD}. The extracted Q_{GD} values are 114.8 nC/cm^2, 80.6 nC/cm^2, 89.2 nC/cm^2 for C-UMOSFET, DT-MOSFET, and ST-MOSFET, respectively. In addition, the extracted total gate charge (Q_G) values are 839 nC/cm^2, 805.1 nC/cm^2, 812.7 nC/cm^2 for C-UMOSFET, DT-UMOSFET, and ST-UMOSFET. This result is proportional to the extracted results of C_{GD}. The HF-FOM ($R_{ON\text{-}SP} \times Q_{GD}$) of DT-MOSFET and ST-MOSFET is 289 mΩ·nC, 224 mΩ·nC, respectively, which is improved by 26% and 42% compared to C-UMOSFET.

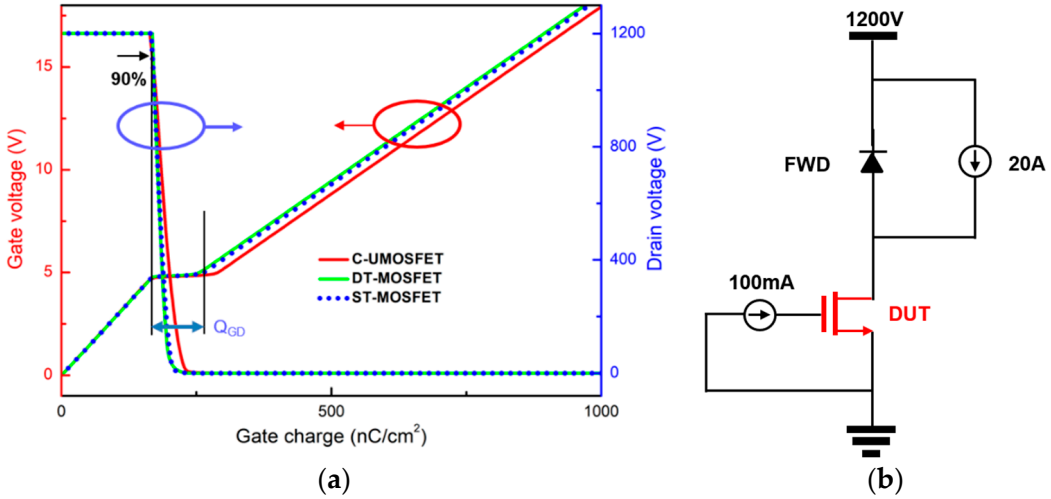

Figure 13. (**a**) Gate charge characteristics of each structure; (**b**) Test circuit.

Table 3 summarizes the results including the values for terminal capacitance, gate charge, and HF-FOMs, which are significant parameters for high frequency performance [8,37,41].

Finally, the switching performance parameter of the device was extracted through a double-pulse test (DPT). The active areas of all the DUT were set to 0.3 cm^2 [42], which is similar to that of commercial devices [43]. Figure 14a plots the full waveform of the ST-MOSFET. Figure 14b shows the test circuit in the three structures. The gate resistance is set to 10 Ω, and the gate voltage switched between 15 V and −3 V for the on- and off-states. The stray inductance was assumed to be 10 nH. The load inductance was set to 300 μH, and the first gate voltage pulse lasted 5 μs so that the load current flow was 20 A. The body diode of the same device as the DUT was used as a freewheeling diode, and the supply voltage was 1200 V.

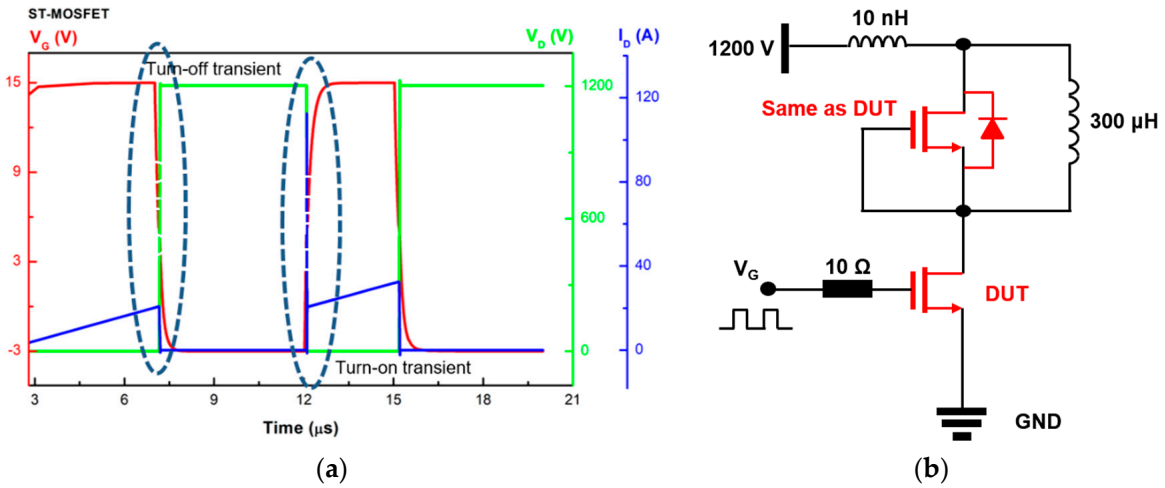

Figure 14. (**a**) Full DPT waveform of ST-MOSFET; (**b**) Test circuit.

In this paper, turn-on time (T_{ON}) and turn-off time (T_{OFF}) are defined as follows [43–45].

$$T_{ON} = T_{D-ON} + T_R \tag{4}$$

$$T_{OFF} = T_{D-OFF} + T_F \tag{5}$$

where $T_{D\text{-}ON}$ is the turn-on delay time (from 10% of V_G to 90% of V_D at the rising edge), T_R is the rise time at the turn-on transient (from 90% of V_D to 10% of V_D at the rising edge), $T_{D\text{-}OFF}$ is the turn-off delay time (from 90% of V_G to 10% of V_D at the falling edge) and fall time at the turn-off transient (from 10% of V_D to 90% of V_D at the falling edge). Figure 15 shows the switching waveforms of each structure, and Table 4 summarizes the detailed switching performance data. The switching speed (T_{ON} and T_{OFF}) of the device is most affected by C_{iss}, and T_R and T_F are most dependent on C_{GD} [37,41]. In hard switching, V_D and I_D are swept during T_R and T_F, so energy loss is dependent upon T_R and T_F. In the previous section, we observed that the C_{iss} of DT-MOSFET and ST-MOSFET is almost the same as the value of C-UMOSFET. Therefore, the switching speed of DT-MOSFET and ST-MOSFET is maintained at the same level as C-UMOSFET. In addition, the C_{GD} of DT-MOSFET and ST-MOSFET is superior to that of C-UMOSFET, which improves the switching energy loss. The switching energy loss of C-UMOSFET, DT-MOSFET, and ST-MOSFET are 827.1 µJ, 771.2 µJ, and 806 µJ, respectively. In addition, since the drain voltage sweeps from low to high at the falling edge of the turn-off transient, T_{OFF} is relatively slower than T_{ON}. Moreover, since the body diode of each device was used as FWD, E_{ON} includes the diode reverse recovery. Therefore, E_{ON} is relatively larger than E_{OFF}.

Table 4. Switching performance of each structure.

Parameter	C-	DT-	ST-
$T_{D\text{-}ON}$ [ns]	56.87	57.68	56.70
T_R [ns]	13.18	10.48	10.73
T_{ON} [ns]	70.05	68.16	67.43
$T_{D\text{-}OFF}$ [ns]	135.1	137.4	132.7
T_F [ns]	23.75	20.48	23.53
T_{OFF} [ns]	158.8	157.8	156.3
E_{ON} [µJ]	655.3	610.7	637.5
E_{OFF} [µJ]	171.8	160.6	168.5
E_{SW} [µJ]	827.1	771.2	806.0

The total power losses P_t of the device consist of conduction losses and switching losses and are calculated as follows [19,37,40]:

$$P_t = dR_{on-sp}{I_d}^2 + f(E_{ON} + E_{OFF}) \tag{6}$$

where d is the duty cycle and f is the switching frequency. Figure 16 shows the power losses which vary with the switching frequency when the duty cycle is 0.5. As the switching frequency increases, the ratio of switching losses of total power losses increases. The power losses of C-UMOSFET, DT-MOSFET, and ST-MOSFET when operating at 200 kHz are 552.1 W/cm^2, 514.9 W/cm^2 and 537.8 W/cm^2, respectively.

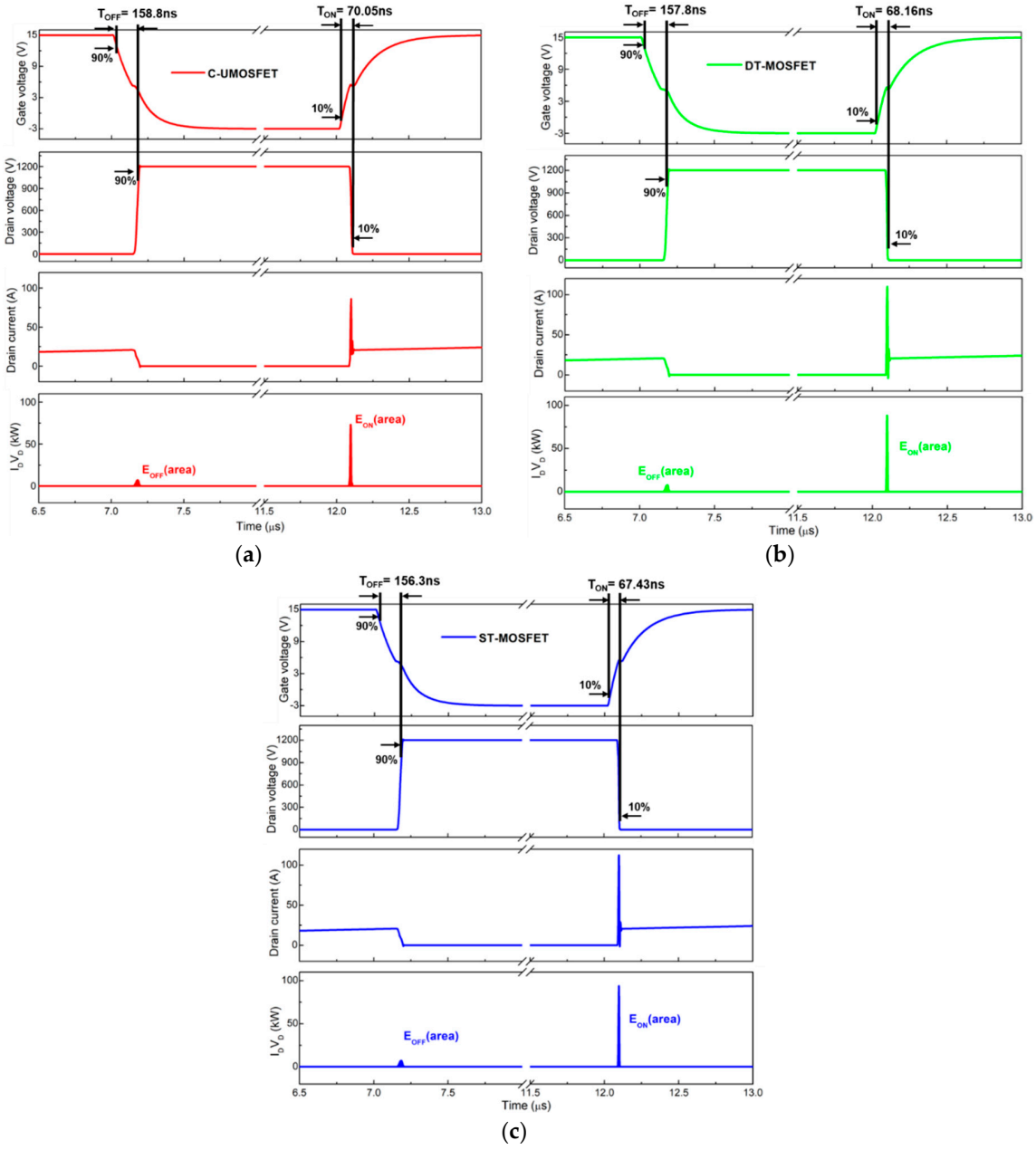

Figure 15. Switching waveform of (**a**) C-UMOSFET, (**b**) DT-MOSFET, and (**c**) ST-MOSFET.

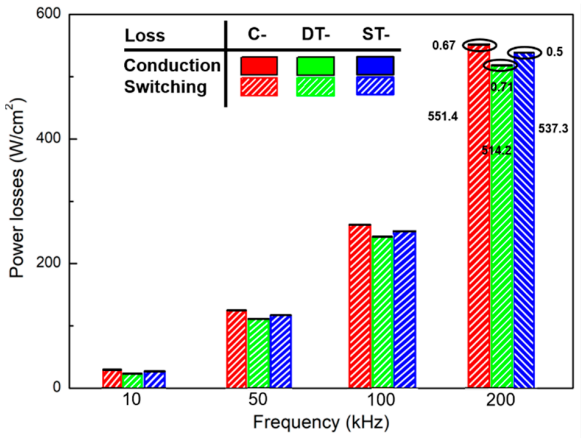

Figure 16. Comparison of power losses depending on switching frequency.

4. Conclusions

In this paper, the static and dynamic performance of the 4H-SiC C-UMOSFET, DT-MOSFET and ST-MOSFET were compared through TCAD simulation. In static characteristics, the $R_{ON\text{-}SP}$ of the ST-MOSFET is 2.52 mΩ·cm^2, which is 25% lower than that of C-UMOSFET. Furthermore, the DC-FOM of the ST-MOSFET is 1179 MW/cm^2, which is 37% higher than that of the C-UMOSFET. At V_D = 1200 V, the Eox-max of the DT-MOSFET is 0.6 MV/cm, which was 44% lower than that of the C-UMOSFET. To improve the static characteristics, both the DT-MOSFET and ST-MOSFET are trenched in the source region. For the same reason, the BPR is introduced in the three structures. The effect of the trenched source region and BPR on the capacitance was analyzed, and the dynamic characteristics of the three structures were compared. Due to the trenched source region, the overlapping area between the gate and source increases. Nevertheless, the capacitance between the gate and the BPR is largest of C_{GS} components, so the C_{iss} is almost identical in all three structure. On the other hand, the C_{GD} of DT-MOSFET and ST-MOSFET is reduced by 44% and 24%, respectively, compared to C-UMOSFET. This is because the depletion region is expanded by the trenched source region. Since the C_{GD} of DT-MOSFET and ST-MOSFET is superior to that of C-UMOSFET, it improves HF-FOM ($R_{ON\text{-}SP} \times C_{GD}$). The HF-FOM ($R_{ON\text{-}SP} \times Q_{GD}$) of DT-MOSFET and ST-MOSFET is 289 mΩ·nC, 224 mΩ·nC, respectively, which is improved by 26% and 42% compared to C-UMOSFET. The switching speed of DT-MOSFET and ST-MOSFET are maintained at the same level as the C-UMOSFET. The switching energy loss and power loss of the DT-MOSFET and ST-MOSFET are slightly improved compared to C-UMOSFET.

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