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Calculation of Semiconductor Power Losses of a Three-Phase Quasi-Z-Source Inverter

Ivan Grgić *, Dinko Vukadinović, Mateo Bašić and Matija Bubalo

Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture, University of Split, 21000 Split, Croatia; dvukad@fesb.hr (D.V.); mabasic@fesb.hr (M.B.); mbubalo@fesb.hr (M.B.)

* Correspondence: igrgic00@fesb.hr

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Abstract: This paper presents two novel algorithms for the calculation of semiconductor losses of a three-phase quasi-Z-source inverter (qZSI). The conduction and switching losses are calculated based on the output current-voltage characteristics and switching characteristics, respectively, which are provided by the semiconductor device manufacturer. The considered inverter has been operated in a stand-alone operation mode, whereby the sinusoidal pulse width modulation (SPWM) with injected 3rd harmonic has been implemented. The proposed algorithms calculate the losses of the insulated gate bipolar transistors (IGBTs) and the free-wheeling diodes in the inverter bridge, as well as the losses of the impedance network diode. The first considered algorithm requires the mean value of the inverter input voltage, the mean value of the impedance network inductor current, the peak value of the phase current, the modulation index, the duty cycle, and the phase angle between the fundamental output phase current and voltage. Its implementation is feasible only for the Z-source-related topologies with the SPWM. The second considered algorithm requires the instantaneous values of the inverter input voltage, the impedance network diode current, the impedance network inductor current, the phase current, and the duty cycle. However, it does not impose any limitations regarding the inverter topology or switching modulation strategy. The semiconductor losses calculated by the proposed algorithms were compared with the experimentally determined losses. Based on the comparison, the correction factor for the IGBT switching energies was determined so the errors of both the algorithms were reduced to less than 12%.

Keywords: loss-calculation algorithm; power inverter losses; quasi-Z-source inverter; semiconductor losses

1. Introduction

The growing production of the electrical energy from renewable sources requires new solutions in the field of power inverters. Conventional voltage-source inverters (VSIs) in applications with photovoltaic modules or fuel cells usually require an additional dc-dc boost converter. The main task of this converter is to boost and control the input voltage. One of the possible alternatives is to use single stage buck-boost inverters, such as the Z-source inverter (ZSI) [1,2]. This inverter boosts the input voltage by short circuiting one or more inverter phase legs, thus achieving the so-called shoot-through (ST) state. Many modifications and improvements have been proposed for the ZSI topology [2,3], as well as for the respective switching modulation strategies [4]. The quasi-ZSI (qZSI) topology [5] is probably the most widely used modification of the ZSI topology. The main advantages of the qZSI are continuous input current and reduced voltage rating of one of the capacitors in the impedance network. The main disadvantages of the Z-source-related topologies compared to the combination of the dc-dc boost converter and VSI are the lower efficiency [6] and the electromagnetic interference and safety problems due to the leakage current [7].

Inverter power losses are an important factor in inverter analysis. These losses consist of semiconductor and passive component losses. The calculation of the latter is rather simple, whereas the calculation of the semiconductor losses is much more complex, and many methods have been proposed to deal with it. Methods in [8–10] calculate the semiconductor losses based on the measured voltage and current of the respective semiconductor devices. These methods are prone to measurement errors. In addition, a current sensor should preferably be installed in each leg of an inverter because otherwise an asymmetry in the inverter legs' conductance could occur. On the other hand, methods in [6,11–22] are based on the output current-voltage (I–V) characteristics and switching characteristics provided by the semiconductor device manufacturer. The loss-calculation algorithms proposed in [6,11–19] require the mean and the root mean square (RMS) values of the currents and voltages of an inverter and are applicable only for one [11–13] or few similar topologies [6,14–16] and for a specific switching modulation strategy. The algorithms presented in [20,21] are based on instantaneous values of the currents and voltages of an inverter and are more generally applicable. The accuracy and the implementation of the mentioned algorithms highly depend on the amount of detail provided in the semiconductor device datasheet (i.e., the output I–V characteristics and switching characteristics vs. the junction temperature or the collector-emitter voltage).

The calculation of semiconductor losses of the previously mentioned ZSI and qZSI topologies represents a challenging task. The loss-calculation algorithms designed for the conventional VSI in [11–13] may not be used for the ZSI topologies since in the latter case there are additional losses produced by the ST states. Furthermore, losses of the diode in the ZSI impedance network also have to be accounted for. Algorithms in [6,14,15] calculate both the conduction and switching losses of the ZSI. However, the authors in [6] have considered the relationship between the semiconductor current and switching energies to be linear. More accurate approximation is ensured by utilizing the characteristics provided by the semiconductor device manufacturer [14,15]. As for the qZSI, the semiconductor losses in [10] were calculated according to the measured current and voltage of the respective semiconductor devices. However, these measurements have to be made very accurately, because even low measurement errors, due to the multiplication of the instantaneous voltage and current, could result with high loss calculation errors. The authors in [17] proposed the semiconductor loss-calculation algorithm (LCA) for the current-fed qZSI, whereas in [18,19] the same was done for the voltage-fed qZSI. However, in the three mentioned papers, the relationship between the semiconductor current and switching energies is considered to be linear. Finally, in [6,17–19] the switching losses were calculated without considering the impact of the phase angle between the fundamental output phase current and voltage. This impact was considered in [14,15], but only for the traditional PWM switching states and not for the ST states.

This paper considers the semiconductor power losses of the qZSI with implemented sinusoidal pulse width modulation (SPWM) with injected 3rd harmonic. Two proposed LCAs calculate the losses of the impedance network diode and the losses of the insulated-gate bipolar transistors (IGBTs) and free-wheeling diodes (FWDs) in the inverter bridge. In the case of the IGBTs, the conduction losses and the switching (turn-on and turn-off) losses were calculated, whereas in the case of the diodes, the conduction and reverse recovery losses were calculated. Both the proposed LCAs require the output I-V characteristics and the switching characteristics provided by the semiconductor device manufacturer. The first considered LCA (LCA1) is based on the algorithms presented in [11–13], which were there applied for the conventional VSI. However, unlike the conventional VSI, the qZSI utilizes the additional ST states, whose losses also need to be calculated. The input variables of the LCA1 are the mean value of the qZSI input voltage and current, the peak value of the output phase current, the duty cycle, the modulation index, and the phase angle between the fundamental output phase current and voltage. On the other hand, the second LCA (LCA2) is based on the algorithm presented in [20,21], but here it is adapted for the qZSI in order to account for the ST states. The input variables of the LCA2 are the instantaneous values of the following variables: the inverter input voltage and current, the impedance network diode current, the duty cycle, and the inverter output phase current.

The semiconductor losses calculated by the two proposed LCAs are compared with the experimentally determined losses, obtained for different values of the switching frequency, input voltage, ST duty cycle, and phase current. The semiconductor losses were experimentally determined by subtracting the measured qZSI output power and the calculated losses of the impedance network inductors from the measured qZSI input power, whereas the losses of the impedance network capacitors were neglected.

2. Quasi-Z-Source Inverter Power Losses

The considered stand-alone control system with the qZSI is shown in Figure 1. In this study, a symmetrical impedance network is considered, i.e., $L_1 = L_2 = L$, $C_1 = C_2 = C$, and $R_{L1} = R_{L2} = R_L$. The additional LCL filter, composed of the inductors (L_{f1}, L_{f2}), capacitors (C_f), and damping resistances (R_d), is connected at the inverter output. The considered qZSI supplies the three-phase resistive load (R_{ac}), whereby the control system maintains the required RMS value of the fundamental load phase voltage (V_{ac}) through adjustment of the modulation index (M). The SPWM with injected 3rd harmonic has been implemented. The qZSI utilizes the standard SPWM switching states (also known as the non-ST states) along with the ST states. The latter occur at the beginning of each zero-switching state of the SPWM, i.e., twice within each switching period (T_{sw}), in order to provide the required input voltage boost

$$B = \frac{1}{1-2D} = \frac{1}{1-2\frac{T_0}{T_{sw}}} \tag{1}$$

where D is the ST duty cycle and T_0 is the ST state period.

The peak value of the load phase voltage ($V_{ac,pk}$) and the peak value of the inverter bridge input voltage (V_{pn}) may be defined as follows:

$$\begin{aligned} V_{ac,pk} &= BM\frac{V_{in}}{2} \\ V_{pn} &= BV_{in} = \frac{V_{in}}{1-2D} \end{aligned} \tag{2}$$

where V_{in} represents the qZSI input voltage.

The power losses of the qZSI are defined as the difference between the inverter input and output power. These losses may be divided into the semiconductor losses, the core losses of the impedance network inductors, and the parasitic resistance losses. In this study, the latter losses include only the copper losses of the impedance network inductors, whereas the power losses of the impedance network capacitors are considered negligible due to the low equivalent series resistance (ESR) of the utilized polypropylene capacitors. The parasitic resistance losses of the impedance network inductors were calculated based on the measured inductor current and previously determined parasitic coil resistance, whereas the corresponding core losses were calculated according to the equation proposed by the core manufacturer [23].

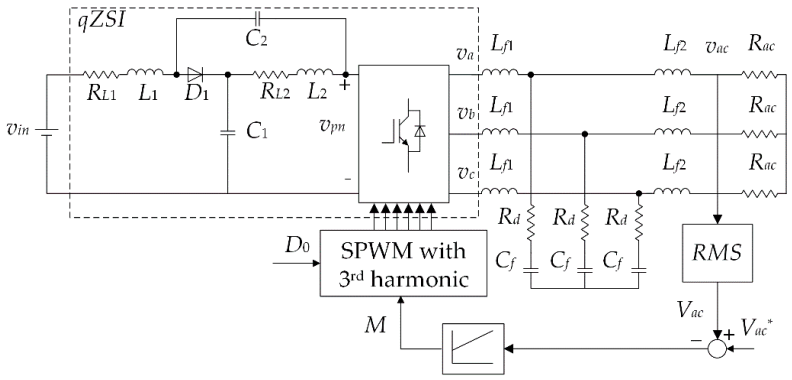


Figure 1. Control system of the qZSI in a stand-alone operation mode.

The semiconductor losses of the qZSI include the losses of the IGBTs, the FWDs, and the impedance network diode. The losses of the IGBTs include the conduction losses, the switching losses, and the

blocking losses. On the other hand, the losses of the diodes include the conduction losses, the reverse recovery losses, and the turn-on losses. The blocking losses of the IGBTs along with the turn-on losses of the diodes may be generally considered negligible. With respect to the above, two novel algorithms for calculation of the qZSI semiconductor losses are proposed in the next section.

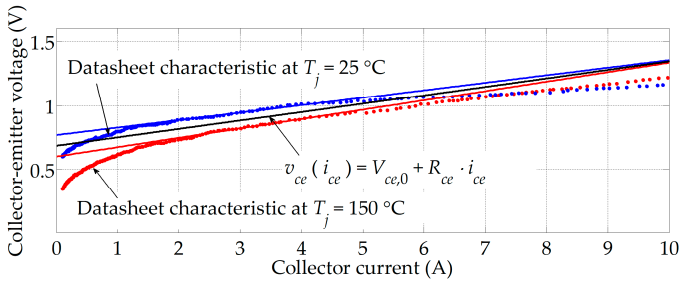
3. Proposed Semiconductor LCAs for the Quasi-Z-Source Inverter

In this section, two novel qZSI semiconductor LCAs are presented. Both the proposed LCAs calculate the losses of the IGBTs and FWDs in the three-phase inverter bridge and the losses of the impedance network diode. As for of the inverter bridge, the losses of a single upper IGBT-FWD pair were calculated and then multiplied by six in order to obtain the total bridge losses. The proposed LCAs require the output I–V characteristics of the IGBTs and diodes for calculation of the respective conduction losses, whereas the turn-on (only for the IGBT) and the turn-off characteristics are required for calculation of the respective switching losses. These characteristics are provided in the datasheet of the switching device manufacturer. Figure 2a shows the output I–V characteristics of the utilized IGBT. These characteristics have been linearized by considering the points taken from the datasheet graphs in the low-current range given the fact that the collector current in this study did not exceed 5 A. The IGBT threshold voltage (V_{ce0}) and the IGBT forward resistance (R_{ce}) were extracted for both provided junction temperatures (T_j = 25 °C and T_j = 150 °C). However, with the assumption that the actual junction temperature during normal operation is somewhere between these two values, final values of $V_{ce,0}$ and R_{ce} were obtained by averaging the values extracted for the two provided temperatures. The I–V characteristics of the FWD and the impedance network diode were approximated in the same way. Finally, the approximated I–V characteristics are defined as follows:

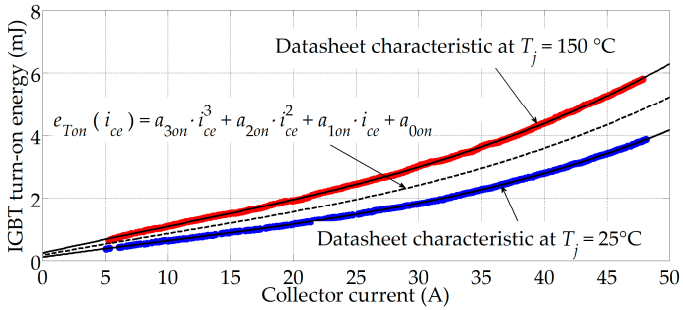
$$v_{ce}(i_{ce}) = V_{ce,0} + R_{ce} i_{ce} \tag{3}$$

$$v_{D/D1}(i_{D/D1}) = V_{D/D1,0} + R_{D/D1} i_{D/D1} \tag{4}$$

where v_{ce} and i_{ce} are the collector-emitter voltage and the collector current, respectively; $v_{D/D1}$, $V_{D/D1,0}$, $R_{D/D1}$, $i_{D/D1}$ are the forward voltage, the threshold voltage, the forward resistance, and the forward current of the FWD (subscript "*D*") and the impedance network diode (subscript "*D*1"), respectively.



(**a**)



(**b**)

Figure 2. I–V characteristics (**a**) and turn-on characteristics (**b**) of the utilized IGBT.

The values of the threshold voltage and the forward resistance for all the considered semiconductor devices are given in Appendix A.

The datasheets of all the semiconductor devices considered in this paper contain switching energy vs. current characteristics for the junction temperatures T_j = 25 °C and T_j = 150 °C. In addition, these characteristics are provided for the specified reference values of the inverter bridge input voltage (noted as V_{ref}) and the gate resistance. As an example, the IGBT turn-on energy (e_{Ton}) vs. the collector current is shown in Figure 2b. The characteristics were extracted for both the provided temperatures and approximated by utilizing the cubic fitting. The coefficients a_{0on}, a_{1on}, a_{2on}, a_{3on} (values given in Appendix A) were obtained by averaging the coefficients determined for the two provided temperatures. In this study, the actual inverter bridge input voltage was different from V_{ref}, so the calculated IGBT turn-on energy was scaled by the ratio $\left(V_{pn}/V_{ref}\right)^{k_T}$, according to the recommendations in [22,24], where k_T is the exponent representing the voltage dependence of the IGBT switching losses. On the other hand, the value of the gate resistance utilized in the experimental setup corresponded to the value given in the datasheet characteristics of interest. Finally, the same principle of the polynomial coefficient extraction has been applied for the IGBT turn-off characteristic and the reverse recovery characteristics of the qZSI diodes. Thus,

$$e_{Ton/off}(i_{ce}) = \left(\frac{V_{pn}}{V_{ref}}\right)^{k_T}\left(a_{3on/off}i_{ce}^3 + a_{2on/off}i_{ce}^2 + a_{1on/off}i_{ce} + a_{0on/off}\right) \tag{5}$$

$$e_{D/D1rr}(i_D) = \left(\frac{V_{pn}}{V_{ref}}\right)^{k_{D/D1}}\left(b_{3D/D1}i_{D/D1}^3 + b_{2D/D1}i_{D/D1}^2 + b_{1D/D1}i_{D/D1} + b_{0D/D1}\right) \tag{6}$$

where e_{Toff} is the turn-off switching energy of the IGBT; $e_{D/D1,rr}$ is the reverse recovery energy of the FWD (subscript "D") and the impedance network diode (subscript "$D1$"); $k_{D/D1}$ is the exponent representing the voltage dependence of the reverse recovery losses.

Values of the polynomial coefficients a_{off} and $b_{D/D1}$ are given in Appendix A, whereas V_{ref} of the considered IGBT and diodes is equal to 600 V. Finally, k_T = 1.4, $k_D = k_{D1}$ = 0.6 are chosen according to [24].

3.1. Loss-Calculation Algorithm 1

The first LCA is based on the methods which were in [11–13] used for the conventional VSI with the SPWM. However, in the considered qZSI configuration, the additional ST states occur, which make the loss calculation more complex.

The conduction losses of a single IGBT are calculated separately for the non-ST state and ST state. In both cases, the conduction losses are calculated based on the conduction energy. The phase current is assumed to be sinusoidal and the current ripple of the impedance network inductor is neglected. The IGBT conduction losses during the non-ST states ($P_{Tcond,nST}$) and the ST states ($P_{Tcond,ST}$) are, respectively, defined as follows (for more details see Appendix B, Equations (A1)–(A9)):

$$P_{Tcond,nST} = V_{ce,0}I_{phM}\left(\frac{1-D}{2\pi} + \frac{M\cos(\varphi)}{8}\right) + R_{ce}I_{phM}^2\left(\frac{1-D}{8} + \frac{M\cos(\varphi)}{3\pi} - \frac{M\cos(3\varphi)}{90\pi}\right) \tag{7}$$

$$P_{Tcond,ST} = D\left[R_{ce}\left(\frac{4}{9}I_L^2 + \frac{1}{8}I_{phM}^2\right) + V_{ce,0}\frac{2}{3}I_L\right] \tag{8}$$

where I_{phM} represents the phase current amplitude, I_L represents the mean value of the impedance network inductor current, φ represents the phase angle between the fundamental output phase current and voltage, and M represents the modulation index ($0 \le M \le 2/\sqrt{3}$).

The overall conduction losses of all the IGBTs in the three-phase inverter bridge are defined as follows:

$$P_{Tcond} = 6\left(P_{Tcond,nST} + P_{Tcond,ST}\right) \tag{9}$$

The conduction losses of the FWD are calculated based on its conduction energy. The overall conduction losses of all the FWDs (P_{Dcond}) in the three-phase inverter bridge are determined as follows (for more details see Appendix B, Equations (A10)–(A12)):

$$P_{Dcond} = 6\left[V_{D,0}I_{phM}\left(\frac{1-D}{2\pi} - \frac{M\cos(\varphi)}{8}\right) + R_D I_{phM}^2\left(\frac{1-D}{8} - \frac{M\cos(\varphi)}{3\pi} + \frac{M\cos(3\varphi)}{90\pi}\right)\right] \quad (10)$$

The impedance network diode conducts only during the non-ST states, whereby the diode current is assumed to be equal to I_L. The corresponding conduction losses are calculated based on the conduction energy. The conduction losses of the impedance network diode are calculated with the assumption that I_L is constant within a single T_{sw}, as follows (for more details see Appendix B, Equation (A13)):

$$P_{D1cond} = (1-D)\left(R_{D1}I_L^2 + V_{D1,0}I_L\right) \quad (11)$$

The switching losses of the IGBT consist of the switching losses of the non-ST states and the ST states. The switching losses of the non-ST states are caused by the switching transitions between the consecutive non-ST states. These losses may be calculated based on the total number of pulses N which occur within T.

$$\begin{aligned} P_{Ton,nST} &= \frac{1}{NT}\sum_n e_{Ton} \\ P_{Toff,nST} &= \frac{1}{NT}\sum_n e_{Toff} \end{aligned} \quad (12)$$

where $P_{Ton,nST}$ and $P_{Toff,nST}$ are the IGBT turn-on and turn-off losses during the switching transitions between the non-ST states, respectively.

The IGBT current is assumed to be sinusoidal during the non-ST states, which implies that the non-ST states switching losses are also sinusoidal. These losses occur only within the positive period of the phase current. By considering the facts mentioned above and switching frequency (f_{sw}), an approximation of Equation (12) can be given as follows:

$$\begin{aligned} P_{Ton,nST} &= \frac{1}{2\pi}\int_0^{\pi} f_{sw}e_{Ton}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = \frac{e_{Ton}\left(I_{phM}\right)}{\pi}f_{sw}\cos(\varphi) \\ P_{Toff,nST} &= \frac{1}{2\pi}\int_0^{\pi} f_{sw}e_{Toff}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = \frac{e_{Toff}\left(I_{phM}\right)}{\pi}f_{sw}\cos(\varphi) \end{aligned} \quad (13)$$

The switching losses of the ST states are caused by the switching transitions between the ST state and the non-ST state. The calculation of these losses is a bit more complex. The switching energies during these transitions are determined by the IGBT current during the ST state, which is equal to sum of 1/2 of the phase current and 2/3 of I_L. Accordingly, the ST state switching losses may be defined as follows:

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi}\int_0^{2\pi}\left[e_{Ton}\left(\tfrac{2}{3}I_L\right) + e_{Ton}\left(\frac{I_{phM}}{2}\right)\sin(\omega t-\varphi)\right]d\omega t \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi}\int_0^{2\pi}\left[e_{Toff}\left(\tfrac{2}{3}I_L\right) + e_{Toff}\left(\frac{I_{phM}}{2}\right)\sin(\omega t-\varphi)\right]d\omega t \end{aligned} \quad (14)$$

where $P_{Ton,ST}$ and $P_{Toff,ST}$ represent the ST states turn-on and turn-off switching losses, respectively.

The ST states switching losses depend on the number of the ST state turn-on and turn-off switching transitions that occur within one T_{sw}. However, during a single fundamental period of the phase current, this number is not constant. It varies depending on the sign of the phase current and the relation between the instantaneous values of the three reference voltages (v_{refA}, v_{refB}, v_{refC}). For example, the single period of the reference voltage (v_{refA}) is divided into five intervals, with each interval having a specific constant number of switching transitions within one T_{sw}. In the intervals where the corresponding phase current (i_{phA}) is negative, the IGBT conducts only during the ST states. Consequently, in these intervals, the ST state turn-on and turn-off switching transitions occur twice

within one T_{sw}. However, in the intervals where $i_{phA} > 0$, the number of the ST states switching transitions depends on the relation between v_{refA}, v_{refB}, and v_{refC}, due to the occurrence of the non-ST switching transitions at the intersection points of v_{refA} and the carrier triangular signal. The borders of these intervals are defined by the time points where v_{refA} intersects the remaining two reference voltages, and also by the time points of i_{phA} zero crossings.

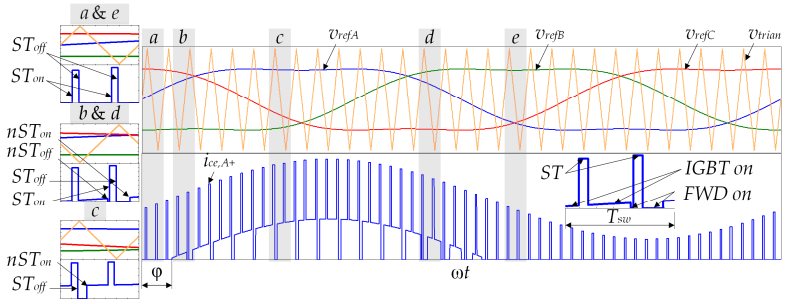
There are two separate set of equations for the calculation of the ST states switching losses. The first set applies for the phase angles between 0 and $\pi/6$ (case 1), whereas the second set applies for the phase angles between $\pi/6$ and $\pi/2$ (case 2). Tables 1 and 2 show the number of switching transitions in the defined intervals for the cases 1 and 2, respectively. The number of switching transitions given in the considered tables is defined based on Figure 3, where the period equal to ωT_{sw} is magnified within each considered phase angle interval. The labels a, b, c, d, e (a', b', c', d', e') represent only the part of the intervals I_1, I_2, I_3, I_4, I_5 (I'_1, I'_2, I'_3, I'_4, I'_5,), respectively, with the length equal to ωT_{sw}.

Table 1. The number of the switching transitions for the phase angle between 0 and $\pi/6$.

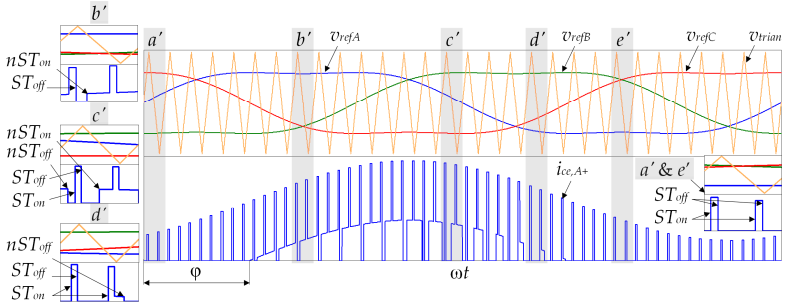
Interval	$N_{nST,on}$	$N_{nST,off}$	$N_{ST,on}$	$N_{ST,off}$
$I_1 = [0, \varphi]$	0	0	2	2
$I_2 = [\varphi, \pi/6]$	1	1	1	1
$I_3 = [\pi/6, 5\pi/6]$	1	0	0	1
$I_4 = [5\pi/6, (\pi + \varphi)]$	1	1	1	1
$I_5 = [(\pi + \varphi), 2\pi]$	0	0	2	2

Table 2. The number of the switching transitions for the phase angle between $\pi/6$ and $\pi/2$.

Interval	$N_{nST,on}$	$N_{nST,off}$	$N_{ST,on}$	$N_{ST,off}$
$I'_1 = [0, \varphi]$	0	0	2	2
$I'_2 = [\varphi, 5\pi/6]$	1	0	0	1
$I'_3 = [5\pi/6, 7\pi/6]$	1	1	1	1
$I'_4 = [7\pi/6, (\pi + \varphi)]$	0	1	2	1
$I'_5 = [(\pi + \varphi), 2\pi]$	0	0	2	2



(**a**)



(**b**)

Figure 3. Waveforms of the reference voltages, the carrier triangular signal, and the IGBT current for the phase angle between 0 and $\pi/6$ (**a**) and the phase angle between $\pi/6$ and $\pi/2$ (**b**).

In the case 1, shown in Figure 3a, the IGBT turns on straight into the ST state ($N_{ST,on}$) and turns off from the ST state ($N_{ST,off}$) twice during each T_{sw} in the intervals I_1 and I_5. In the intervals I_2 and I_4, both the ST switching transitions occur once during each T_{sw}, as well as the IGBT turn-on ($N_{nST,on}$) and turn-off ($N_{nST,off}$) transitions into non-ST states. On the other hand, in the interval I_3, the ST state occurs when the IGBT is already conducting, so there are no switching transitions ($N_{nST,off} = 0$ and $N_{ST,on} = 0$). Since the phase current is positive and the turn-off switching losses between non-ST states are already obtained from Equation (13), their influence has to be eliminated from the switching loss equations defined for the interval I_3. The ST states switching losses for the case 1 are calculated based on the number of switching transitions defined in Table 1 and Equation (14), as follows (for more details see Appendix C, Equation (A14)):

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\tfrac{7}{6}e_{Ton}\left(\tfrac{2}{3}I_L\right) - \tfrac{\sqrt{3}\cos(\varphi)+2}{2\pi}e_{Ton}\left(\tfrac{I_{phM}}{2}\right)\right] \\ P_{Toff,ST} &= f_{sw}\left[\tfrac{3}{2}e_{Toff}\left(\tfrac{2}{3}I_L\right) - \tfrac{1}{\pi}e_{Toff}\left(\tfrac{I_{phM}}{2}\right) - \tfrac{\sqrt{3}\cos(\varphi)}{2\pi}e_{Toff}\left(I_{phM}\right)\right] \end{aligned} \tag{15}$$

In the case 2, when φ is in between π/6 and π/2, the number of the switching transitions defined in Table 2 is determined based on Figure 3b. The ST states switching losses for the case 2 are calculated based on the number of switching transitions defined in Table 2 and Equation (14), as follows (for more details see Appendix C, Equation (A15)):

$$\begin{aligned} P_{Ton,ST} &= f_{sw}\left[\left(1+\tfrac{\varphi}{\pi}\right)e_{Ton}\left(\tfrac{2}{3}I_L\right) - \tfrac{\sqrt{3}\cos(\varphi)+2}{2\pi}e_{Ton}\left(\tfrac{I_{phM}}{2}\right) - e_{Ton}\left(I_{phM}\right)\tfrac{1-\cos(\varphi-\pi/6)}{2\pi}\right] \\ P_{Toff,ST} &= f_{sw}\left[\tfrac{3}{2}e_{Toff}\left(\tfrac{2}{3}I_L\right) - \tfrac{1}{\pi}e_{Toff}\left(\tfrac{I_{phM}}{2}\right) - \tfrac{\cos(\varphi+\pi/6)+1}{2\pi}e_{Toff}\left(I_{phM}\right)\right] \end{aligned} \tag{16}$$

The overall switching losses of the IGBTs in the three-phase inverter bridge are defined as follows:

$$P_{Tsw} = 6\left(P_{Ton,nST} + P_{Toff,nST} + P_{Ton,ST} + P_{Toff,ST}\right) \tag{17}$$

The FWD conducts only the phase current, so the reverse recovery losses of the diode are also sinusoidal. The overall reverse recovery losses of all six FWDs (P_{Drr}) in the three-phase inverter bridge are determined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\int_0^{\pi} e_{Drr}\left(I_{phM}\right)\sin(\omega t-\varphi)d\omega t = 6\frac{f_{sw}}{2\pi}\int_0^{\pi} J d\omega t \tag{18}$$

The number of the reverse recovery switching transitions of the FWD is closely related to the IGBT turn-on switching transitions; namely, every time the IGBT turns on during the positive period of the phase current, the FWD recovers. That means that the total number of the diode reverse recoveries, in fact, equals the sum of the IGBT turn-on switching transitions ($N_{nST,on} + N_{ST,on}$) during the positive period of the phase current. Consequently, the reverse recovery losses of the FWDs have been calculated by considering the cases defined above. In case 1, based on Table 1 and Equation (18), P_{Drr} are defined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\left[2\int_{\varphi}^{\frac{\pi}{6}} J d\omega t + \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} J d\omega t + 2\int_{\frac{5\pi}{6}}^{(\varphi+\pi)} J d\omega t\right] = 6f_{sw}\frac{4-\sqrt{3}\cos(\varphi)}{2\pi}e_{Drr}\left(I_{phM}\right) \tag{19}$$

In the case 2, based on Table 2 and Equation (18), P_{Drr} are defined as follows:

$$P_{Drr} = 6\frac{f_{sw}}{2\pi}\left[\int_{\varphi}^{\frac{5\pi}{6}} J d\omega t + 2\int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} J d\omega t + 2\int_{\frac{7\pi}{6}}^{(\varphi+\pi)} J d\omega t\right] = 6f_{sw}\frac{\sin(\varphi)-\sqrt{3}\cos(\varphi)+6}{4\pi}e_{Drr}\left(I_{phM}\right) \tag{20}$$

It is important to note that for the boundary phase angle of $\pi/6$, Equations (15) and (16) become equal, as well as Equations (19) and (20). Thus, the switching losses are changing continuously with the phase angle.

The impedance network diode recovers every time the ST state occurs, i.e., twice during each T_{sw}. With the reverse recovery current being considered equal to I_L, the reverse recovery losses of the impedance network diode are defined as follows:

$$P_{D1rr} = 2f_{sw}e_{D1rr}(I_L) \tag{21}$$

3.2. Loss-Calculation Algorithm 2

The second LCA is based on the algorithm presented in [20,21], which is for the first time here adapted for the qZSI. The corresponding flow chart is shown in Figure 4. The semiconductor losses are calculated by considering the instantaneous values of the following variables in kth and $(k-1)$st instants: the ST state signal (ST_{signal}), the non-ST state switching pulses of the IGBT (p), the phase current (i_{ph}), the impedance network diode current (i_{D1}), the impedance network inductor current (i_L), and the input voltage of the inverter (v_{in}).

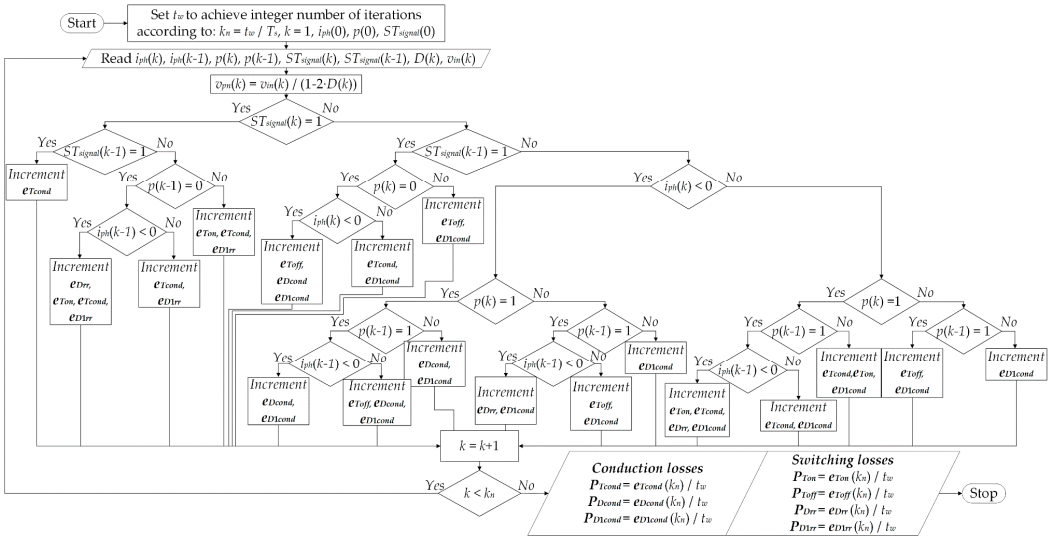


Figure 4. Flow chart of the LCA2.

The calculation of the IGBT conduction energy (e_{Tcond}) requires the value of the collector current. This current is equal to the phase current (i_{ph}) during the non-ST states. However, during the ST states, it is equal to the sum of one half of the phase current and two thirds of the impedance network inductor current. The IGBT conduction energy is calculated as follows:

$$\begin{aligned} e_{Tcond}(k) &= e_{Tcond}(k-1) + v_{ce}(k)\left|i_{ce}(k)\right|[t(k) - t(k-1)] \\ v_{ce}(k) &= V_{ce,0} + R_{ce}\left|i_{ce}(k)\right| \end{aligned} \tag{22}$$

The FWD does not conduct during the ST state, whereas it conducts part of the phase current during the negative half-period. The FWD conduction energy is defined as follows:

$$\begin{aligned} e_{Dcond}(k) &= e_{Dcond}(k-1) + v_D(k)\left|i_{ph}(k)\right|[t(k) - t(k-1)] \\ v_D(k) &= V_{D,0} + R_D\left|i_{ph}(k)\right| \end{aligned} \tag{23}$$

Further, the turn-on (e_{Ton}) and the turn-off (e_{Toff}) switching energies of the IGBT are calculated based on the collector current, whereas the reverse recovery energy (e_{Drr}) of the FWD is calculated based on the phase current as follows:

$$e_{Ton/off}(k) = e_{Ton/off}(k-1) + e_{Ton/off}\left(\left|i_{ce}(k)\right|\right) \tag{24}$$

$$e_{Drr}(k) = e_{Drr}(k-1) + e_{Drr}\left(\left|i_{ph}(k)\right|\right) \tag{25}$$

The conduction energy (e_{D1cond}) and reverse recovery energy (e_{D1rr}) of the impedance network diode are calculated as follows:

$$\begin{aligned} e_{D1cond}(k) &= e_{D1cond}(k-1) + v_{D1}(k)\left|i_{D1}(k)\right|[t(k) - t(k-1)] \\ v_{D1}(k) &= V_{D1,0} + R_{D1}\left|i_{D1}(k)\right| \\ e_{D1rr}(k) &= e_{D1rr}(k-1) + e_{D1rr}\left(\left|i_{D1}(k)\right|\right) \end{aligned} \tag{26}$$

Finally, the calculation of the corresponding power losses requires dividing of the energies accumulated in the time window (t_w), corresponding to the integer number of cycles of the phase current, with the time window duration in seconds.

4. Experimental Testing and Evaluation

The laboratory setup of the system shown in Figure 1 was built in order to test the proposed LCAs. The qZSI was supplied by the dc power supply Chroma 62050H-600S which provides voltages up to 600 V and currents up to 8.2 A. The three-phase inverter bridge is composed of six IGBTs with integrated FWDs IRG8P60N120KD (International Rectifier). The gate drivers SKHI 22B(R) (Semikron) were utilized to drive the IGBTs. The impedance network diode was built as a parallel compound of four FWDs of the IGBT-FWD pair IRG8P25N120KD (International Rectifier) since the impedance network current would be too excessive for a single diode of this type. The parameters of the inductors and capacitors in the impedance network along with the LCL filter parameters are given in Appendix D. The control algorithm was implemented by means of the MicroLabBox (dSpace) microcontroller and executed with the sampling frequency of 10 kHz. The reference RMS value and frequency of the fundamental load phase voltage were set to 230 V and 50 Hz, respectively. The ST signals were injected by a hardware circuit placed in between the digital outputs of the MicroLabBox and the signal inputs of the gate drivers.

4.1. Implementation Requirements of the Proposed Loss-Calculation Algorithms

Implementation requirements represent the important factor in the analysis of the proposed LCAs. They include the computational requirements, the number of required input variables and parameters, and the number of additional current/voltage sensors required to implement the desired LCA. The common input variables of the proposed algorithms are D, i_L, V_{in}, and i_{ph}. The additional input parameters of the LCA1 are M and φ, whereas in the case of the LCA2, the additional input signals are the i_{D1} waveform, the ST state signal, and the non-ST state switching pulses.

The value of the duty cycle required for the implementation of the LCA2 was obtained from the control algorithm. On the other hand, the currents required for the implementation of the LCA2 (i_L, i_{ph}, i_{D1}) were measured by means of the Hall-effect transducers IT 60-S (LEM). The input voltage of the qZSI, also required for the implementation of the LCA 2, has been measured by means of the Hall effect transducers CV 3–500 (LEM).

The waveforms of the three input currents (i_L, i_{ph}, i_{D1}) and the non-ST state switching pulses of the IGBT, required by the LCA2, were recorded by the oscilloscope MDO 3014 (Tektronix), which ensures sampling frequencies (f_{samp}) up to 10 MHz. The waveform of the qZSI input voltage was recorded by the oscilloscope SDS 1104X-E (Siglent), whereas the ST state signal was reconstructed based on the i_{D1} waveform, as shown in Figure 5. During the ST states ($ST_{signal} = 1$), i_{D1} is zero, whereas during the non-ST states ($ST_{signal} = 0$), this current is always positive.

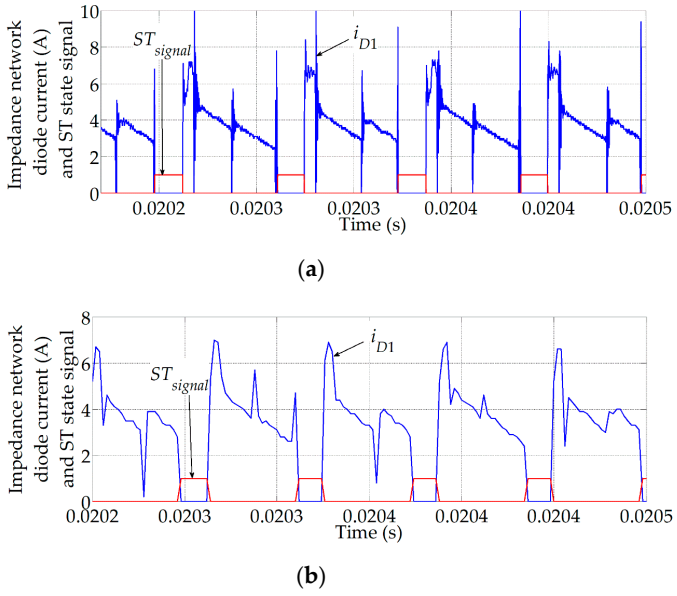


Figure 5. Waveforms of the impedance network diode current and the ST signal for the switching frequency of 8 kHz and sampling frequencies of 10 MHz (**a**) and 500 kHz (**b**).

The signals acquired by the oscilloscope MDO 3014 were originally sampled at 10 MHz and subsequently downsampled to determine the minimum value of f_{samp} that still allows capturing the required information from the recorded waveforms. With regard to this, the waveforms of i_{D1} and ST_{signal} were analyzed for the highest switching frequency considered in this study, which is 8 kHz. The minimum sufficient f_{samp} obtained for this case is also sufficient for switching frequencies lower than 8 kHz because lower f_{sw} implies lower minimum f_{samp}. During the measurement of the waveforms shown in Figure 5, the ST duty cycle was 0.22, which along with f_{sw} = 8 kHz, according to Equation (1), determines the ST state duration $T_0/2$ = 13.75 µs. For f_{samp} = 10 MHz (Figure 5a), the measured duration of each ST state ($T_0/2$) deviated by about ± 0.7 µs from the mentioned calculated value. This deviation is a consequence of an error induced by the hardware circuit that injects the ST signals. The goal was to retain approximately the same deviation of $T_0/2$ value while reducing f_{samp}. The minimum f_{samp} value for which this was achieved was equal to 500 kHz (Figure 5b). For the sampling frequencies lower than 500 kHz, the i_{D1} waveform could not be any more faithfully reconstructed, which led to an error in $T_0/2$ value of up to 3 µs.

The impedance network inductor current waveform shown in Figure 6 was also sampled with the frequency of f_{samp} = 500 kHz, although this signal could be faithfully reconstructed by applying the sampling frequency as low as 100 kHz. However, it is mandatory for the non-ST state switching pulses of the IGBT to be sampled with the same frequency as the waveform of i_{D1} in order to avoid the mismatch between that signal and the reconstructed ST state signal. Finally, the waveforms of the phase current and the qZSI input voltage were sampled with 10 kHz.

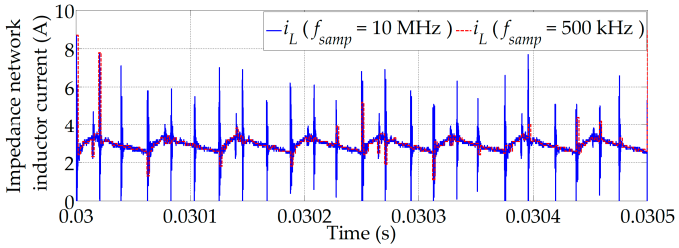


Figure 6. Waveform of the impedance network inductor current for the switching frequency of 8 kHz and sampling frequencies of 10 MHz and 500 kHz.

The LCA1 requires the values of M, D, φ, I_L, V_{in}, and I_{phM} for implementation. The latter three values may be relatively easily determined from the measured waveforms, whereas the values of M and D are obtained from the control algorithm. However, the value of φ has to be either determined from the measured phase current and voltage or known in advance (e.g., for a resistive load, $\varphi = 0$).

It may be concluded that the implementation of the LCA2 is more complex primarily due to an additional current sensor required for i_{D1}. Moreover, all three additional input signals required by the LCA2 have to be sampled with high sampling frequencies (i.e., 500 kHz or higher for the setup used in this study).

4.2. Experimental Results

All the experiments were carried out with the three-phase resistive load ($\varphi = 0$) connected to the inverter output. Figure 7 shows the semiconductor power losses distribution with respect to the switching frequency, RMS value of the phase current, qZSI input voltage, and duty cycle. During the variation of the switching frequency, the other system parameters were $D = 0.22$, $I_{ph} = 1.72$ A, $V_{in} = 450$ V, whereas the variation of I_{ph}, V_{in}, and D was carried out with the switching frequency set to 5 kHz. Different RMS values of the phase current were achieved by varying the load resistance, with $D = 0.22$ and $V_{in} = 450$ V. The variation of the input voltage was carried out with $D = 0.18$ and $I_{ph} = 1.72$ A, whereas the variation of the duty cycle was carried out with $V_{in} = 470$ V and $I_{ph} = 1.72$ A. The selected ranges of V_{in} and D were determined by considering several limitations of the utilized laboratory setup; namely, the combination of high input voltage and high ST duty cycle may result in IGBT collector-emitter voltage higher than the allowed maximum value of 1200 V, which may ultimately destroy the device. On the other hand, too low an input voltage would require a higher than allowed modulation index, whose value, according to the maximum constant boost strategy, must not exceed $2/\sqrt{3}(1-D)$ in order to maintain the six active states of the inverter intact [4]. Finally, high input voltage in combination with high duty cycle may cause the electromagnetic interference, which may disrupt the normal operation of the gate drivers.

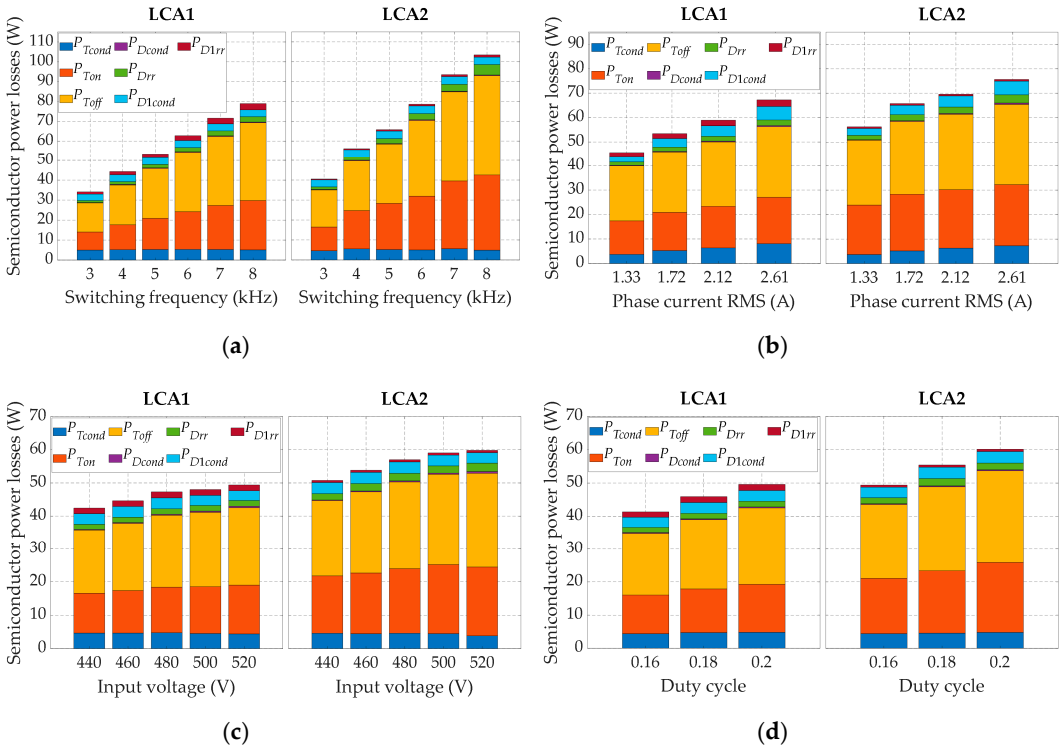


Figure 7. Semiconductor power losses distribution with respect to: switching frequency (**a**), RMS phase current (**b**), input voltage (**c**), and duty cycle (**d**).

The increase of the semiconductor losses with all four varied parameters was noted for both the proposed algorithms. However, arguably the largest increase is noted with the increase of the switching frequency. For example, at f_{sw} = 3 kHz, the total semiconductor losses calculated by the LCA1 and LCA2 amounted to P_{LCA1} = 34 W and P_{LCA2} = 40 W, respectively, whereas at f_{sw} = 8 kHz, these values have more than doubled and amounted to P_{LCA1} = 79 W and P_{LCA2} = 103 W, respectively. On the other hand, a less pronounced change in the semiconductor losses was noted in the considered ranges of the phase current, the input voltage, and the duty cycle.

Both algorithms indicate that the total losses of the IGBTs, considered as the sum of the respective switching and conduction losses, are dominant compared to the total diode losses and account for approximately 87% of the total semiconductor losses. In addition, the IGBT conduction losses account for approximately 10% of the total IGBT losses for both the algorithms. These losses are practically unaffected by the switching frequency and duty cycle since the IGBT current remains the same with the variation of these two parameters. However, the conduction losses increase with the phase current, whereas they decrease with the input voltage due to the decrease of the qZSI input current for the same applied load. The IGBT switching losses, which account for approximately 90% of the total IGBT losses, consist of the turn-on (P_{Ton}) and turn-off (P_{Toff}) switching losses. These losses significantly increase with the switching frequency due to the increase of the number of switching transitions. The same tendency is noted with the increase of the phase current due to the increase of switching energies according to Equation (5). The switching losses of the IGBTs also increase with the duty cycle and the input voltage due to the increase of V_{pn} as per Equation (2). The total losses of the FWDs account for approximately 5% of the total semiconductor losses, where the reverse recovery losses are dominant over the conduction losses. Finally, the remaining 8% of the total semiconductor losses belong to the impedance network diode losses, with the conduction losses being dominant over the reverse recovery losses. The mentioned losses of the qZSI's diodes have similar behavior as the losses of the IGBTs in terms of variation with f_{sw}, i_{ph}, V_{in}, and D.

The semiconductor losses calculated by the two proposed LCAs have been compared with the measured ones. For that purpose, the input and output inverter power along with the power losses of the impedance network inductors (P_L) and capacitors had to be obtained. As in [25], the copper losses of the impedance network inductors were calculated based on the respective current and the parasitic coil resistance. Likewise, the inductors' core losses were calculated according to the equation proposed in the datasheet of the core manufacturer [23]. The same datasheet shows that the losses of this core type are practically unaffected by the core temperature in the case of a continuous operation of up to 10 h, regardless of the values of the switching frequency and the magnetic induction. Since the experiments in this study lasted less than one hour, the temperature impact was neglected. The power losses of the impedance network capacitors were neglected due to the low ESR value. The inverter input power P_{in} was obtained as the mean value of $i_L \cdot v_{in}$, whereas the inverter output power (P_{acinv}) was measured by the high-precision power analyzer Norma 4000 (Fluke). The semiconductor losses were ultimately obtained as $P_{in} - P_{acinv} - P_L$, with the wire parasitic resistance losses considered negligible.

Figure 8 shows the comparison between the measured semiconductor losses ($P_{measured}$) and the calculated semiconductor losses from Figure 7. The absolute errors of both the LCA1 and LCA2 increase significantly with the switching frequency as shown in Table 3. On the other hand, the absolute errors of the proposed algorithms only slightly increase with the phase current RMS value, qZSI input voltage and duty cycle. Overall, the LCA2 provided more accurate results for all the considered values of f_{sw}, i_{ph}, V_{in}, and D. By assuming that the inductor core losses are calculated accurately, that the capacitor losses are negligible, and that both the input and output power of the inverter are accurately measured, the remaining differences between the measured and calculated losses are ascribed to the LCA errors. The errors of both the proposed LCAs significantly increase with the switching frequency. It is suspected that the values of the switching energies in the considered laboratory setup were higher than the values provided in the datasheet of the IGBT manufacturer, which are determined based on the double-pulse test. This is, presumably, due to the shortcomings of the double-pulse test such as

errors in the calculation of switching energies due to inaccuracies in voltage/current measurement or the influence of the parasitic capacitances and additional loop inductance/resistance within the test circuitry on the switching energies, as described in [26].

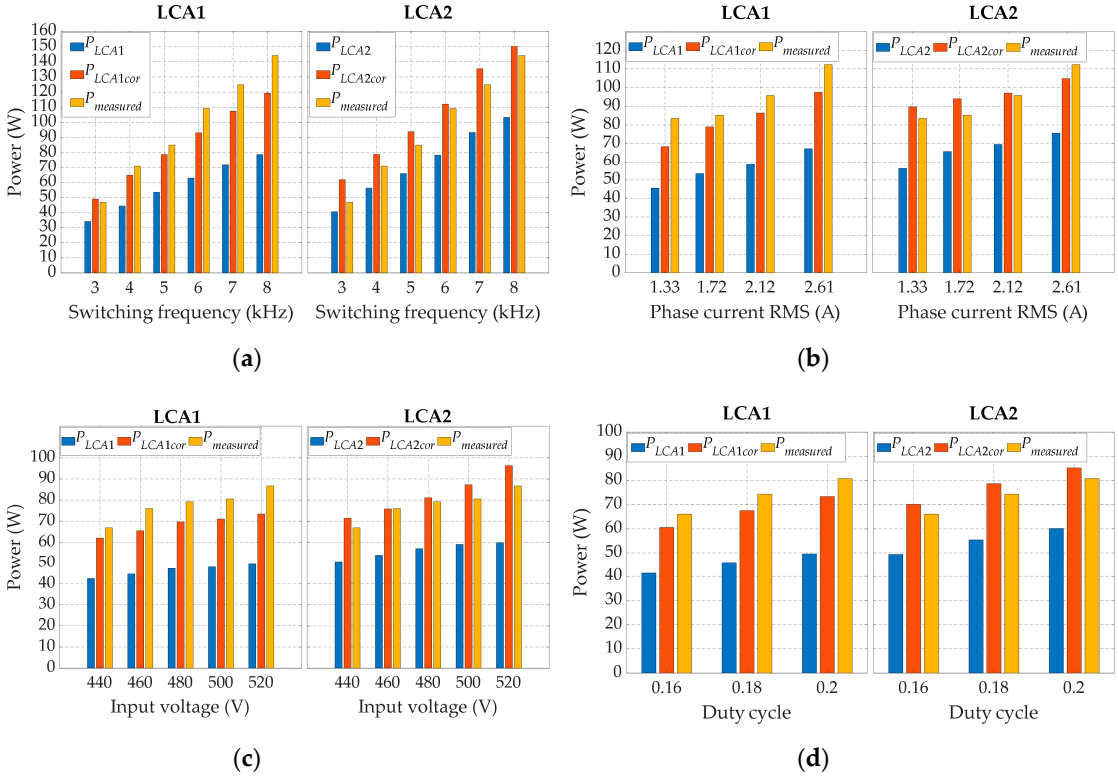


Figure 8. Measured and calculated semiconductor losses with respect to: switching frequency (**a**), RMS phase current (**b**), input voltage (**c**), and duty cycle (**d**).

Table 3. Absolute and relative errors with respect to the measured semiconductor losses of the proposed LCAs.

Switching Frequency	LCA1	LCA1cor	LCA2	LCA2cor
3 kHz	12 W (25%)	−2 W (−4%)	6 W (12%)	−15 W (−31%)
4 kHz	27 W (38%)	6 W (8%)	15 W (21%)	−8 W (−11%)
5 kHz	32 W (37%)	6 W (7%)	19 W (22%)	−9 W (−10%)
6 kHz	46 W (42%)	16 W (14%)	30 W (27%)	−3 W (−3%)
7 kHz	53 W (43%)	17 W (14%)	32 W (25%)	−10 W (−8%)
8 kHz	65 W (45%)	24 W (16%)	40 W (27%)	−6 W (−4%)

The influence of the switching frequency on the switching losses may be shown by considering the temperature of the semiconductor device. For that purpose, the IGBT-FWD case temperature was measured in steady state by means of the thermal camera Testo 865 (Testo) for all the considered switching frequencies. Figure 9 shows that, for the frequency increase from 3 kHz to 7 kHz, the IGBT-PWD case temperature increased by a total of 11 °C. However, when the switching frequency was increased from 7 kHz to 8 kHz, the temperature increased for 12 °C. These results confirm that the IGBT-FWD switching losses significantly increase with the switching frequency since the conduction losses are not affected by the switching frequency. The temperature increase is presumably caused by the increase of the IGBT switching losses, since both the proposed algorithms indicate that they are dominant over the FWD switching losses.

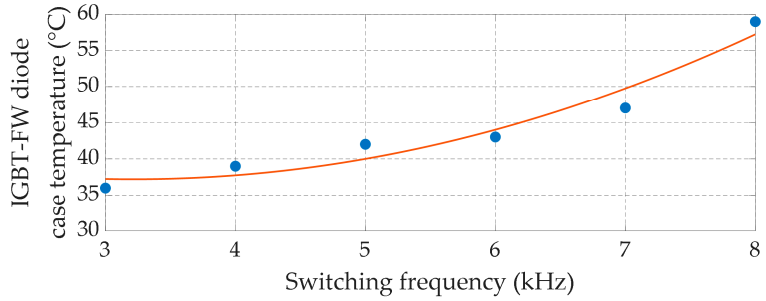


Figure 9. Measured temperature of the IGBT-FWD case at different switching frequencies.

4.2.1. Correction of the IGBT Switching Losses Calculation

As a way of simple correction of the calculated IGBT switching losses, the IGBT turn-on and turn-off switching energies defined in Equation (5) were multiplied by the same factor greater than 1 with the aim of reducing the LCA2 error to zero. The LCA2 was chosen for the correction because it involves far less simplifications compared to the LCA1 so it, expectedly, provided more accurate results prior to the correction. The final value of the multiplication factor was determined by averaging the values obtained for several measurement points. For that purpose, four points with the I_{ph} values of 1.33 A, 1.72 A, 2.12 A, and 2.61 A were chosen. For all the considered points, the switching frequency was set to 5 kHz and V_{pn} amounted to 800 V, thus maintaining the constant V_{pn}/V_{ref} ratio. Hence, the influence of k_T was the same for all the considered measurement points. The value of the average multiplication factor obtained in this manner is 1.53, which implies 53% higher IGBT switching energies. Note that by applying the multiplication factor in the described manner, all the other remaining errors, such as the input/output power measurement errors, are ascribed as the calculation error of the IGBT switching losses. Ultimately, the same value of the corrective multiplication factor was applied for both the LCAs.

Figure 8 shows the comparison between the proposed LCAs-prior and after the correction of the IGBT switching energies- and the measured semiconductor losses. In Table 3, the absolute and relative errors are given with respect to the measured semiconductor losses for all the considered f_{sw} values. The accuracy of the LCAs notably increased after the correction of the IGBT switching energies. The same tendency is noted with regard to the qZSI input voltage, the phase current, and the duty cycle.

4.2.2. Efficiency and Semiconductor Losses Share of the qZSI

Figure 10 shows the qZSI efficiency and the share of the measured semiconductor losses in the total inverter losses with respect to the switching frequency. The inverter efficiency decreases approximately linearly in the considered frequency interval, whereas the share of the measured semiconductor losses increases rapidly from about 50% at f_{sw} = 3 kHz to almost 85% at f_{sw} = 8 kHz.

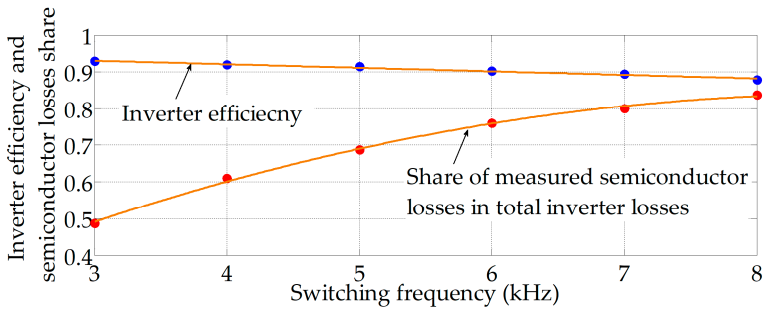


Figure 10. Inverter efficiency and share of measured semiconductor losses in total inverter losses with respect to switching frequency.

5. Conclusions

This paper presents two novel semiconductor LCAs for the three-phase qZSI. The proposed LCAs were successfully applied for the considered inverter in the stand-alone operation mode. However, the proposed algorithms are also applicable for different control systems as well as for grid-tied applications. Both the proposed LCAs indicate that the losses of the transistors are dominant and account for approximately 87% of all the semiconductor losses. Of all transistor losses, the switching losses are dominant with the percentage of 90%. The differences noted between the measured and calculated semiconductor losses are, presumably, due to the differences between the actual switching energies and those provided in the datasheet of the transistor manufacturer. Therefore, the transistor datasheet switching energies, which were used as the input data for the LCAs, were multiplied by the experimentally determined factor of 1.53, which resulted in the mean absolute percentage errors of 11.2% and 7.9% for the LCA1 and LCA2, respectively. Alternatively, instead of relying on the manufacturers characteristics, more accurate IGBT switching characteristics may be obtained prior to LCAs implementation (e.g., determined experimentally from the measurements taken in the normal operating conditions of the considered qZSI) and then used as the input data for the LCAs, and even scaled with respect to the actual measured IGBT case temperature. The experimental results indicate that the qZSI semiconductor losses significantly drop with the switching frequency, resulting in better inverter efficiency. On the other hand, the total harmonic distortion value of the phase currents increases at lower switching frequencies, thus making filter design a more demanding task.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Polynomial coefficients in Equations (3)–(6)

$R_{ce} = 0.066105\ \Omega$, $V_{ce,0} = 0.6823$ V
$R_D = 0.0862\ \Omega$, $V_{D,0} = 0.774$ V
$R_{D1} = 0.1225\ \Omega$, $V_{D1,0} = 0.999$ V
$a_{0on} = 0.18$, $a_{1on} = 0.074$, $a_{2on} = -7.2 \times 10^{-4}$, $a_{3on} = 2.537 \times 10^{-5}$
$a_{0off} = 0.258$, $a_{1off} = 0.081$, $a_{2off} = -1.41 \times 10^{-4}$, $a_{3off} = 0$
$b_{0D} = 0.036$, $b_{1D} = 0.04$, $b_{2D} = -3.76 \times 10^{-4}$, $b_{3D} = 9.9 \times 10^{-7}$
$b_{0D1} = 0.0145$, $b_{1D1} = 0.052$, $b_{2D1} = -0.0012$, $b_{3D1} = 5.34 \times 10^{-6}$

Appendix B

The conduction energy of the IGBT during the non-ST states within one T_{sw} are given by

$$E_{Tcond,nST} = v_{ce} i_{ce,nST} d_{T,nST} T_{sw} \tag{A1}$$

where $i_{ce,nST} = I_{phM} \sin(\omega t)$, $d_{T,nST}$ represents the IGBT duty cycle during the non-ST states, which is, in turn, defined as follows:

$$d_{T,nST} = \frac{1}{2}\left\{1 + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2} \tag{A2}$$

The first term in Equation (A2) represents the duty cycle in the case when the traditional SPWM with the injected 3rd harmonic is implemented. The factor –D/2 appears in Equation (A2) in order to

eliminate the impact of the corresponding ST state (Figure 3a, lower right corner). By substituting Equations (3) and (A2) in Equation (A1), it becomes

$$E_{Tcond,nST} = \left(R_{ce}I_{phM}\sin(\omega t) + V_{ce0}\right)I_{phM}\sin(\omega t)\left\{\frac{1}{2}\left\{1 + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2}\right\}T_{sw} \quad \text{(A3)}$$

Based on the differential form of Equation (A3) ($T_{sw} = dt = T/2\pi\, d\omega t$), the IGBT conduction losses that occur during the non-ST states are defined as follows:

$$P_{Tcond,nST} = \frac{1}{T}\int_0^{T/2} dE_{Tcond,nST} = \frac{1}{2\pi}\int_0^{\pi} E_{Tcond,nST}\, d\omega t \quad \text{(A4)}$$

By substituting Equation (A3) into Equation (A4), $P_{Tcond,nST}$ are defined as follows:

$$P_{Tcond,nST} = \frac{I_{phM}}{4\pi}\int_0^{\pi}\left(R_{ce}I_{phM}\sin(\omega t) + V_{ce,0}\right)\sin(\omega t)\left\{1 - D + M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} d\omega t \quad \text{(A5)}$$

The final expression of $P_{Tcond,nST}$ is obtained by solving the integral on the right-hand side of Equation (A5).

The conduction energy of the IGBT during the ST states within one T_{sw} is given by

$$E_{Tcond,ST} = v_{ce}i_{ce,ST}DT_{sw} \quad \text{(A6)}$$

The IGBT current during the ST state may be approximated as follows [14]:

$$i_{ce,ST} = \frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t) \quad \text{(A7)}$$

By substituting Equations (3) and (A7) in Equation (A6), it becomes

$$E_{Tcond,ST} = \left[R_{ce}\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right) + V_{ce,0}\right]\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right)DT_{sw} \quad \text{(A8)}$$

Based on the differential form of Equation (A8) ($T_{sw} = dt = T/2\pi\, d\omega t$), the IGBT conduction losses that occur during the ST states are defined as follows:

$$P_{Tcond,ST} = \frac{1}{2\pi}\int_0^{2\pi}\left[R_{ce}\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right) + V_{ce,0}\right]\left(\frac{2}{3}I_L + \frac{1}{2}I_{phM}\sin(\omega t)\right)Dd\omega t \quad \text{(A9)}$$

The final expression of $P_{Tcond,ST}$ is obtained by solving the integral on the right-hand side of Equation (A9).

The conduction energy of the FWD within one T_{sw} is defined as follows:

$$E_{Dcond} = i_{ce,nST}v_D(1 - d_{T,nST} - D)T_{sw} = v_D d_D T_{sw} i_{ce,nST} \quad \text{(A10)}$$

where the FWD current is assumed to be sinusoidal, whereas the diode duty cycle (d_D) is defined according to the $d_{T,nST}$ and D, as follows:

$$d_D = \frac{1}{2}\left\{1 - M\left[\sin(\omega t + \varphi) + \frac{1}{6}\sin[3(\omega t + \varphi)]\right]\right\} - \frac{D}{2} \quad \text{(A11)}$$

By substituting Equations (4) and (A11) into Equation (A10), it becomes

$$E_{Dcond} = \left(R_D I_{phM} \sin(\omega t) + V_{D,0}\right) I_{phM} \sin(\omega t) \left\{ \frac{1}{2} \left\{ 1 - M \left[\sin(\omega t + \varphi) + \frac{1}{6} \sin[3(\omega t + \varphi)] \right] \right\} - \frac{D}{2} \right\} T_{sw} \quad \text{(A12)}$$

The FWD conduction losses (P_{Dcond}) were calculated as the integral of the differential form of Equation (A12), similarly as the IGBT conduction losses.

The impedance network diode conduction energy within one T_{sw} is defined as follows:

$$E_{D1cond} = (R_{D1} I_L + V_{D1,0}) I_L (1 - D) T_{sw} \quad \text{(A13)}$$

Appendix C

Calculation of the switching losses in LCA1 for $0 < \varphi < \pi/6$

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} K d\omega t + \int_{\varphi}^{\frac{\pi}{6}} K d\omega t + \int_{\frac{5\pi}{6}}^{(\pi+\varphi)} K d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} K d\omega t \right] \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} I d\omega t + \int_{\varphi}^{\frac{\pi}{6}} I d\omega t + \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} I d\omega t + \int_{\frac{5\pi}{6}}^{(\pi+\varphi)} I d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} I d\omega t - \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} e_{off}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \end{aligned} \quad \text{(A14)}$$

Calculation of the switching losses in LCA1 for $\pi/6 < \varphi < \pi/2$

$$\begin{aligned} P_{Ton,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} K d\omega t + \int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} K d\omega t + 2 \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} K d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} K d\omega t - \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} e_{Ton}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \\ P_{Toff,ST} &= \frac{f_{sw}}{2\pi} \left[2 \int_0^{\varphi} I d\omega t + \int_{\varphi}^{\frac{5\pi}{6}} I d\omega t + \int_{\frac{5\pi}{6}}^{\frac{7\pi}{6}} I d\omega t + \int_{\frac{7\pi}{6}}^{(\pi+\varphi)} I d\omega t + 2 \int_{(\pi+\varphi)}^{2\pi} I d\omega t - \int_{\varphi}^{\frac{5\pi}{6}} e_{Toff}\left(I_{phM}\right) \sin(\omega t - \varphi) d\omega t \right] \end{aligned} \quad \text{(A15)}$$

where $K = e_{Ton}\,(2/3I_L) + e_{Ton}\,(I_{phM}/2)\,\sin(\omega t - \varphi)$, $I = e_{Toff}\,(2/3I_L) + e_{Toff}\,(I_{phM}/2)\,\sin(\omega t - \varphi)$

Appendix D

Parameters of the impedance network inductors:
T520-26 powder cores (Micrometals), L = 20.2 mH (unsaturated), and R_L = 0.5 Ω (at 25 °C).
Parameters of the impedance network capacitors:
MKSPI35-50U/1000 polypropylene capacitors (Miflex), C = 50 µF, and ESR = 7.8 mΩ.
Parameters of the output LCL filter:
L_{f1} = 8.64 mH, L_{f2} = 4.32 mH, C_f = 4 µF, and R_d = 10 Ω.

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