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An Impedance Source Multi-Level Three Phase Inverter with Common Mode Voltage Elimination and Dead Time Compensation

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Abstract: Currently, most electro-mechanical drive systems that require speed control use pulse-width modulated (PWM) variable frequency drives known as adjustable speed drives (ASD). The high switching speeds of the electronics switches are essential for proper operation of the ASD. Common mode voltage (CMV) has its origin in the PWM switching. The CMV increases the stress on the coils and windings, reduces the life of the bearing and, therefore, has a significant impact on motor life cycle. In this paper, a variant of a PWM-based space vector modulation (SVPWM) switching algorithm is proposed to control both the shoot-through intervals and the dead time of the power switches that could be compensated. The proposed algorithm is implemented on a platform consisting of an impedance source network in the DC side of the topology with the purpose of mitigating the CMV and capability of voltage boosting. Since similar methods have achieved a CMV reduction of 1/6 of the DC link voltage so far, in this paper, while surpassing the disturbing current harmonics, the high efficiency is fully accessible. The presented experimental results verify the effectiveness of the proposed approach by slightly increasing the total harmonic distortion (THD) and reducing the converter losses.

Keywords: common-mode voltage (CMV); adjustable speed drive (ASD); three-level NPC inverter

1. Introduction

The three-phase voltage-source inverter is the power conversion basis for modern industrial motor drive systems due to its high flexibility to perform speed and torque control in the whole range of AC motors. Inside of a motor speed drive, PWM control signals are crucial to perform the control requirement, being a control interface standard among industrial inverters. PWM control techniques are really popular because can be easily implemented in modern digital signal controller-based software [1–3].

On the other hand, PWM speed inverters are prone to generate high frequency noise that is conducted and radiated if not properly designed. The PWM-based three-phase waveforms generation technique is also a source of issues because the vector sum of the three-phase voltage is never null. Consequently, it appears as CMV in the motor [4,5]. The consequences of CMV due to PWM inverters are well known: a voltage induction in the rotor shaft allows a significant current to flow through the

rotor support bearings and the grounding system. This is one of causes for motor failures. In addition, high CMV may led to motor electrical insulation disruption, which prevents its operation.

Since a new generation of nitride (GaN) and silicon carbide (SiC) power switches with much higher switching frequency capability will take the preference of power converter designers, including ASD manufacturers, an intensification of CMV issues and additional challenges to comply with electromagnetic compatibility (EMC) standards are expected [6].

Mitigation techniques are recurrent in the technical and scientific literature [7,8]. Basically, the solutions can be divided into three groups. One approach is to reduce induced bearing currents via increasing the impedance between the rotor shaft contact points and the inner ring in bearings. A less expensive option involves the replacement of standard bearings with electrical isolated bearings. The common-mode voltage and current generated by the converter can be reduced by passive or active filters. The CMV can be reduced or even cancelled by special converter topologies or modulation techniques. In the following, a review of these methods is presented. Some basic motor modifications (e.g., carbon brushes and bearing insulations) developed against the classical bearing currents are still in use for the mitigation of converter-generated bearing currents. Carbon brushes are used for grounding the rotating shaft and shunting the bearing current to the ground. A drawback of the carbon brush is that a motor equipped with a brush needs more maintenance. Bearing currents can be prevented by bearing insulations embedded in the end shields, or by hybrid bearings with ceramic rolling elements [9].

Passive filters are used in electric drives to reduce over-voltages at the motor terminals, the EMI, the output current harmonics and the common-mode current [10]. Active filters and modulation techniques are some other CMV mitigating strategies that are used in some scholarly papers. An active common-mode voltage canceller employing the common-mode transformer was proposed in [11]. An emitter-follower, controlled by the CMV obtained using an artificial neutral point, connects the DC-link voltage in the secondary winding in order to compensate the common-mode voltage at the motor terminals. The authors of [12] proposed a similar active filter where the emitter-follower was replaced by a single-phase multilevel half-bridge inverter, which is more suitable for voltage levels commonly used in frequency converters than the emitter-follower. In the simulations, the filter reduced all relevant quantities to about 2% of the original values. Modulation techniques have also been proposed for the reduction of the common-mode voltage of the inverter. The authors of [13] have proposed a method that reduces the common-mode voltage by 50%. It is based on a modulation pattern that does not apply zero vectors. Hence, the common-mode voltage will have only two possible values instead of four. This method is not suitable for modulation methods that actively use the zero vectors, such as the direct torque control (DTC). The authors of [14] proposed the zero vector to be produced by shorting the motor terminals with three auxiliary star-connected switches, which reduces the common-mode voltage without the restriction on the use of the zero vector. In a neutral point clamped (NPC) three-level inverter, it is possible to use only the voltage vectors that give exactly zero common-mode voltage. However, such modulation reduces the number of applicable voltage vectors from the original 27 to 7 [15–17]. Special converters as the topologies can also be modified in such a way that the CMV is compensated, are the other approach. Several methods based on altering the number of inverter legs to an even number have been presented. The advantage of an even number of inverter legs is that the common-mode voltage, which is the average of the phase voltages, can be controlled to zero [18,19].

In general, the solutions to face CMV could be classified into two types: hardware solutions and software solutions. Hardware-based strategies make use of elements such as the common-mode choke filter, passive and active filters, as well as approaches with topology changed such as the four-phase inverter. Though capable of suppressing CMV to some degree, the hardware solutions require additional components, which increase the size, cost and complexity of control and parameter design, whereas the software solutions for suppressing CMV are realised through adjusting the

switching control signals or modulation algorithm of the inverters. They are more economical and flexible, especially when used along with digital signal processing (DSP) technology.

So far, software strategies based on PWM modifications have aroused widespread attention. Previous studies of reduced CMV PWM (RCMVPWM) were mainly conducted on modifications from space vector modulation (SVM) [20–23], carrier-based PWM (CBPWM) [24,25], selected harmonic elimination PWM (SHEPWM) [26–28] and so on. Of these, the RCMV-PWM based on SVM attracted more attention. These RCMV methods can be applied in various inverters with different levels. Considering the diversity of topologies and the universality of application, we focus on three-phase two-level driving systems here, such as space vector PWM (SVPWM), discrete PWM (DPWM), active zero state (AZSPWM), sinusoidal PWM (SPWM) and real state PWM (RSPWM). These strategies are depicted in Figure 1 to show the switching vector areas.

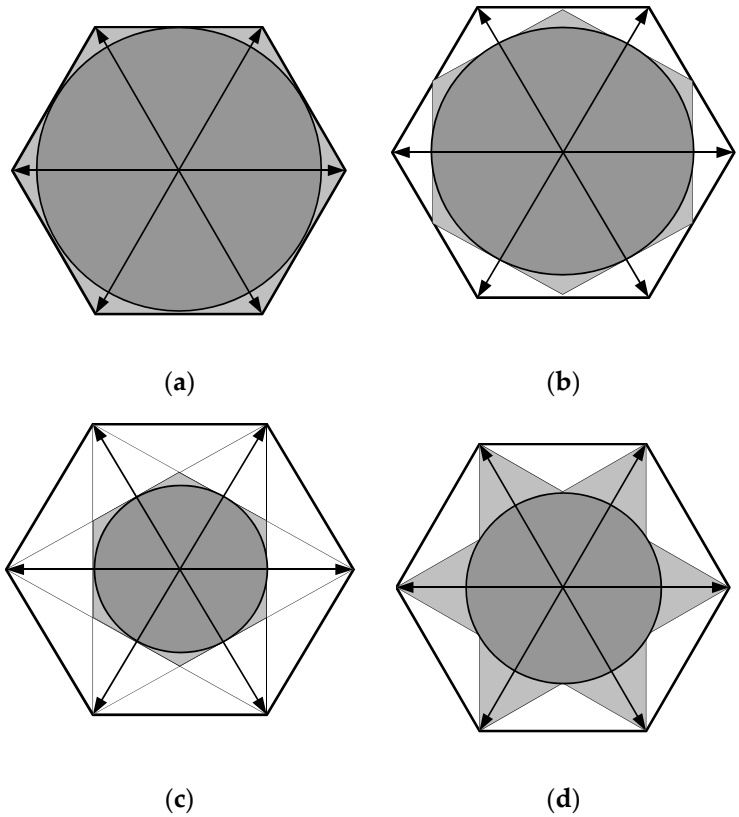


Figure 1. PWM switching algorithms: (**a**) SVPWM, DPWM, AZSPWM; (**b**) SPWM; (**c**) RSPWM; (**d**) RCMV-PWM.

2. CMV Generation

In Figure 2, a conventional three-phase inverter is represented that can be used as a speed control drive for three-phase induction motors. In this Figure, indices g, 0 and n imply the reference ground with zero potential, middle of DC link potential and motor neutral point potential, respectively. Therefore, three-phase output voltages of the inverter could be written by:

$$V_{a0} = V_{an} + V_{n0} \tag{1}$$

$$V_{b0} = V_{bn} + V_{n0} \tag{2}$$

$$V_{c0} = V_{cn} + V_{n0} \tag{3}$$

where V_{xn} are the line-to-neutral voltages and V_{x0} are three-phase output voltages with respect to 0 (DC bus midpoint). Combining equations from (1) to (3), V_{n0} is given as:

$$V_{n0} = \frac{V_{a0} + V_{b0} + V_{c0} - V_{an} - V_{bn} - V_{cn}}{3} \tag{4}$$

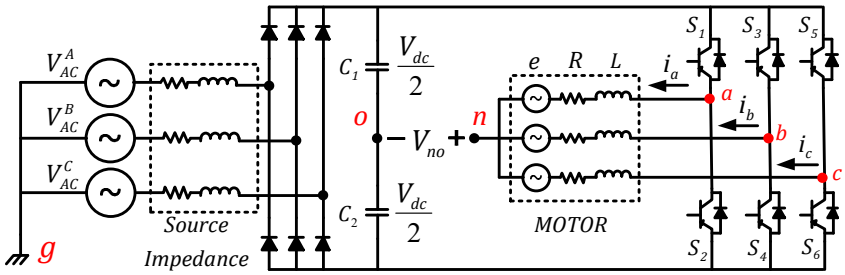


Figure 2. PWM inverter-controlled induction machine.

Assuming balanced load ($V_{an}+V_{bn}+V_{cn} = 0$):

$$V_{n0} = \frac{V_{a0} + V_{b0} + V_{c0}}{3} \tag{5}$$

The quantity V_{n0} is the average of the AC output voltage in relation to the ground, or known as CMV. This voltage is also available in multi-level inverters that have more advantages than conventional three-phase bridges, which should be removed. As mentioned before, the CMV usually appears on stray capacitances of the system.

Figure 3 highlights the parasitic capacitance paths between stator windings and the motor frame where C_{sf} is the capacitance between stator windings and the motor frame, C_{sr} represents the capacitance between stator and rotor, C_{rf} is the rotor to frame capacitance, and finally C_{rf} is the bearing capacitance.

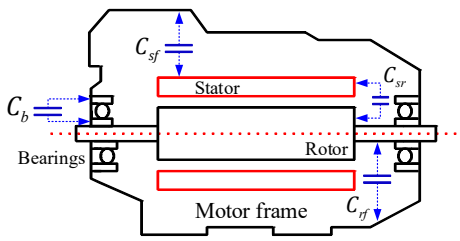


Figure 3. Motor stray capacitances.

For analysis purposes, an equivalent electrical model provides a way to evaluate the leakage and the bearing currents in an AC motor [2]. It is shown in Figure 4. The elements causing line frequency currents to flow over the motor are: (a) the AC or DC magnetic flux circulating through different paths such as the rotor shaft, bearings and motor frame; (b) the voltage between shaft and ground that is distributed by the electrostatic field resulting from the friction of mechanical parts such as pulleys, belts, self-bearings and even ionized air; (c) the AC voltage induced in the motor shaft produced by the monopole magnetic flux passing through the shaft. The third case is the most problematic by inducing a current in the rotor shaft, which in turn it closes through the bearings, motor support and concrete foundations, which cause the appearance of a phenomenon named Electrical Discharge Machining (EDM).

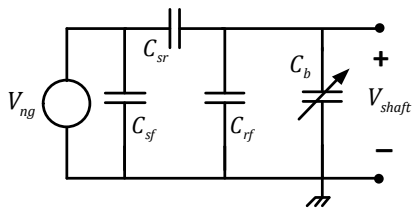


Figure 4. Electrical model of stray capacitances.

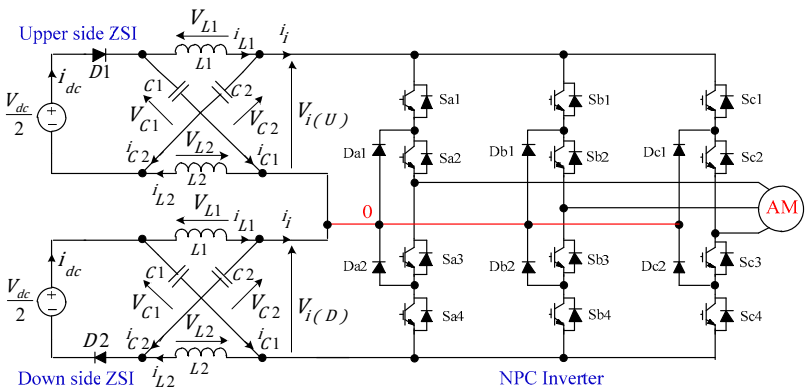
3. Proposed Topology Principles and Evaluation

The three-level NPC inverter is commonly used as the preferred choice for medium voltage AC drives. More recently, low voltage renewable grid-interfacing applications are taking advantage of this topology. Despite their generally favorable output performance, the basic NPC inverter has a known drawback related to its operation. Without an additional power conversion stage, it can only perform in voltage-buck mode operation. To overcome this limitation, a buck–boost Z-source NPC inverter is proposed in [29], where two additional X-shaped impedance networks are added between two isolated DC sources and traditional NPC circuitry. The added impedance networks are responsible for balanced inductive voltage boosting upon shooting through any of the inverter phase-legs without causing damage to their semiconductor switches. This protection from sudden current surge is provided by the inductors found within the Z-source impedance networks. The network consists of a split-inductor (L_1 and L_2) and two capacitors (C_1 and C_2), connected between the input DC source and a traditional NPC inverter circuitry. The input source can be a split-DC source formed by two series-connected capacitors, rather than two isolated sources. On the other hand, the rear-end NPC circuitry allows the inverter to assume three distinct voltage levels per phase leg, whose expressions and corresponding gating signals are shown in Table 1. Compared with the traditional NPC inverter, Table 1 includes also four non-traditional states.

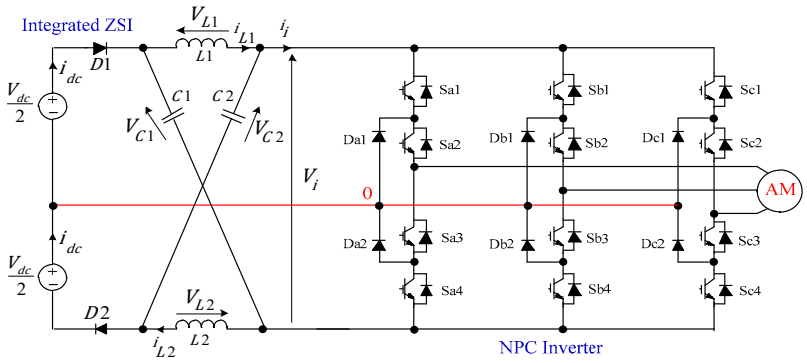
Table 1. Switching states and output values, summarized only for phase A.

State	Conducting Switches	Conducting Diodes	V_A (Phase Voltage)
NST (1)	S_{a1}, S_{a2}	D_1, D_2	$+\frac{V_{dc}}{2}$
NST (2)	S_{a2}, S_{a3}	D_1, D_2, $\{D_{a1}$ *or* $D_{a2}\}$	0
NST (3)	S_{a3}, S_{a4}	D_1, D_2	$\frac{-V_{dc}}{2}$
FST (1)	S_{a1}, S_{a2}, S_{a3}, S_{a4}	–	0
FST (2)	S_{a1}, S_{a2}, S_{a3} S_{c1}, S_{c2}, S_{c3}	D_{a2}, D_{c1}	0
UST	S_{a1}, S_{a2}, S_{a3}	D_{a2} , D_1	$-\frac{\frac{V_{dc}}{2}}{1-D}$
DST	S_{a2}, S_{a3} , S_{a4}	D_{a1}, D_2	$+\frac{\frac{V_{dc}}{2}}{1-D}$

Since the economic considerations and loss analysis restrict us from constructing such a topology as that shown in Figure 5a, the structure represented in Figure 5b has been taken into account to evaluate the performance analysis.



(**a**)



(**b**)

Figure 5. Impedance source multi-level network: (**a**) Two network utilization; (**b**) integrated network utilization.

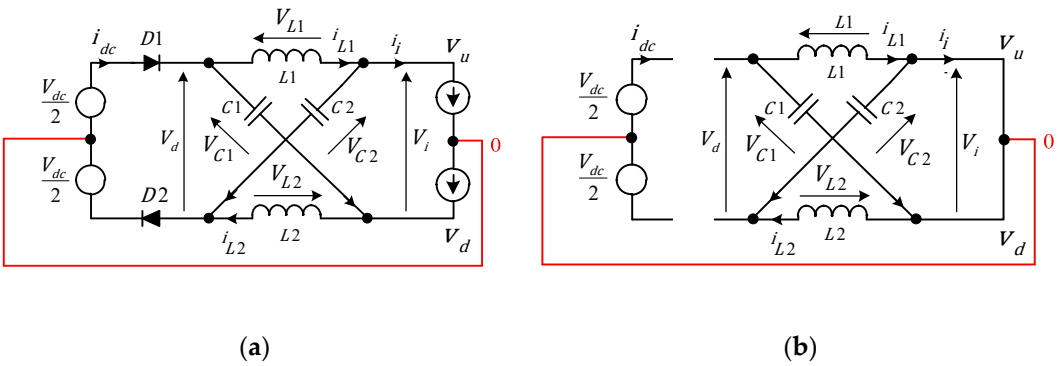
Like the two-level Z-source inverter, these non-traditional states are for boosting voltages carried by the Z-source NPC inverter. In particular, the two full shoot-through (ST) states help to short circuit the DC-link fully, and can be used together with other non-shoot-through (NST) active and null states in a typical modulation state sequence for a Z-source NPC inverter. For distinctly representing the non-shoot-through and shoot-through states, Figure 6 shows their simplified equivalent circuits for analysis, where in Figure 6a the inverter circuitry and external load have been represented by a simplified current source in the NST state. Using this equivalent representation with input diodes D_1 and D_2 conducting, the inductive voltage of the single symmetrical Z-source network ($V_{L1} = V_{L2} = V_L$ and $V_{C1} = V_{C2} = V_C$) and all the voltage gains of Z-source inverter (ZSI) are expressed as below:

$$V_C = 2\frac{V_{dc}}{2}\frac{1 - t_{ST}}{1 - 2t_{ST}} \tag{6}$$

$$V_C = 2\frac{V_{dc}}{2}\frac{1 - t_{ST}}{1 - 2t_{ST}} \tag{7}$$

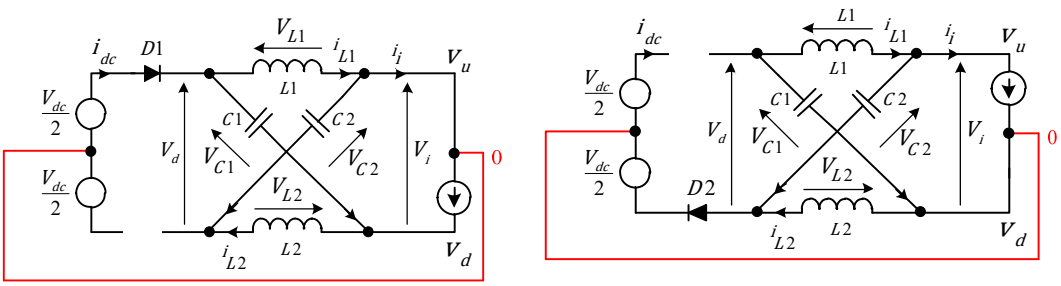
$$V_x = M.B.\frac{V_{dc}}{2}; \quad x\epsilon\{a,\ b,\ c\} \tag{8}$$

where V_C, V_{dc} and V_x are the capacitor voltage, DC link voltage and output ZSI voltage of each phase, respectively. The parameters t_{ST} is shoot-through time interval, M is the modulation index and B is the ZSI voltage gain. An alternative simplified equivalent circuit is presented in Figure 7 for investigating the up shoot-through (UST) and down shoot-through (DST) conditions.



(**a**) (**b**)

Figure 6. Simplified equivalent circuit for evaluating conditions: (**a**) NST state; (**b**) ST state.



(**a**) (**b**)

Figure 7. Simplified equivalent circuit for evaluating conditions: (**a**) Up shoot-through (UST); (**b**) down shoot-through (DST).

As shown in Table 1, the false shoot-through condition can happen, being originated from gate signals that turn-on the transistors. These states led the device to malfunction. For the proposed algorithm and due to the reliability constraints, they are neglected in this paper considering the proposed switching algorithm. Table 2 represents all vectors that can be obtained by the switching vectors represented in Figure 8.

Table 2. CMV generation by Z-source converter.

Vectors	State	CMV	State	CMV	State	CMV
Zero	[OOO]	0	[PPP]	$+\frac{V_{dc}}{2}$	[NNN]	$-\frac{V_{dc}}{2}$
Positive Small	[POO]	$+\frac{V_{dc}}{6}$	[PPO]	$\frac{+V_{dc}}{3}$	[OPO]	$+\frac{V_{dc}}{6}$
	[OPP]	$+\frac{V_{dc}}{3}$	[OPP]	$+\frac{V_{dc}}{6}$	[POP]	$+\frac{V_{dc}}{3}$
Negative Small	[ONN]	$-\frac{V_{dc}}{3}$	[OON]	$-\frac{V_{dc}}{6}$	[NON]	$\frac{-V_{dc}}{3}$
	[NOO]	$-\frac{V_{dc}}{6}$	[NOO]	$-\frac{V_{dc}}{3}$	[ONO]	$-\frac{V_{dc}}{6}$
Medium	[PON]	0	[OPN]	0	[NPO]	0
	[NOP]	0	[ONP]	0	[PNO]	0
Large	[PNN]	$-\frac{V_{dc}}{6}$	[PPN]	$-\frac{V_{dc}}{6}$	[NPN]	$-\frac{V_{dc}}{6}$
	[NPP]	$-\frac{V_{dc}}{6}$	[NPP]	$-\frac{V_{dc}}{6}$	[PNP]	$-\frac{V_{dc}}{6}$

N: negative state, P: positive state.

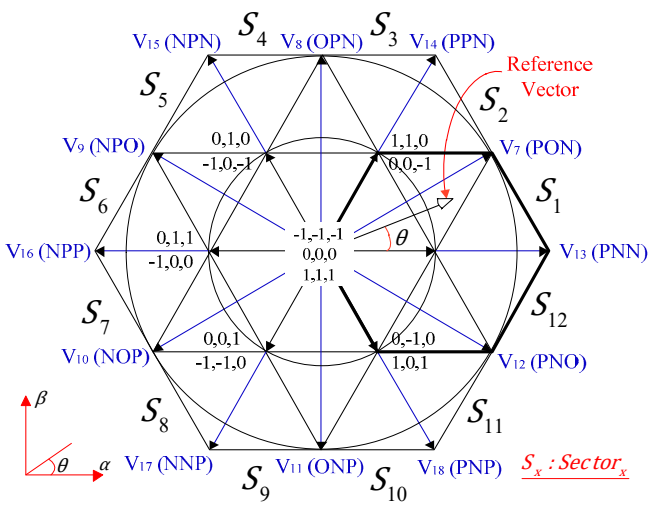


Figure 8. Switching states of the proposed algorithm.

The switching areas shown in Figure 8 are sectionalized into 12 sub-areas. According to Table 2, there are four sections that belong to each phase at ST states which are summarized in Table 3.

Table 3. Switching states of ST in each phase.

Phase	A	B	C
ST Sectors	S_2, S_5, S_8, S_{11}	S_3, S_6, S_9, S_{12}	S_1, S_4, S_6, S_{10}

To investigate the operation principles, it is supposed that the reference vector is positioned in sector 5, for instance.

Then the large, medium and zero vectors around it should have been considered to synthesize the reference voltage as:

$$\vec{V}_{ref} T_s = \vec{V}_0 t_0 + \vec{V}_9 t_9 + \vec{V}_{15} t_{15} \tag{9}$$

where $t_{15} = t_L$ (L: stands for large) and $t_9 = t_M$ (M: stands for medium). The vectors $\vec{V}_0$, $\vec{V}_9$ and $\vec{V}_{15}$ are defined as:

$$\vec{V}_0 = 0 \tag{10}$$

$$\vec{V}_9 = \frac{\sqrt{3}}{3} B \frac{V_{dc}}{2} \measuredangle \frac{5\pi}{6} \tag{11}$$

$$\vec{V}_{15} = \frac{2}{3} B \frac{V_{dc}}{2} \measuredangle \frac{2\pi}{3} \tag{12}$$

Since $\vec{V}_{ref} = V_{ref} \measuredangle \theta$, then the dwell times of the above-mentioned vectors could be calculated as follows:

$$t_L = \sqrt{3}\, M\, T_s \sin\left(\frac{2\pi}{3} - \theta\right) \tag{13}$$

$$t_M = 2M\, T_s \sin\left(\frac{5\pi}{6} - \theta\right) \tag{14}$$

$$t_0 = T_s - t_L - t_M \tag{15}$$

The time interval T_s corresponds to the switching period, while t_L, t_M and t_0 represent the dwell times of the large vectors, medium vectors and the zero vector, respectively. The reference vector angle is assumed to be in the range $\frac{2\pi}{3} \leq \theta \leq \frac{5\pi}{6}$ and the modulation index M is computed as:

$$M = \sqrt{3}\frac{V_{ref}}{B\frac{V_{dc}}{2}} \tag{16}$$

While the modulation index is assumed as $M^{MAX} = 1$, the maximum magnitude of $\vec{V_{ref}}$ and the root mean square (RMS) value of phase to phase voltage (V_{LL}) are figured out as:

$$V_{ref}^{MAX} = \frac{\sqrt{3}}{3}B\frac{V_{dc}}{2} \tag{17}$$

$$V_{LL}^{MAX} = \sqrt{3}\frac{V_{ref}^{MAX}}{\sqrt{2}} = \frac{\sqrt{2}}{2}\,B\,\frac{V_{dc}}{2} \tag{18}$$

Therefore, according to Figure 8, since the small vectors are not considered in voltage analysis calculations, the DC link voltage does not affect the phase to phase voltage. As a result, in the proposed approach, the V_{LL} is similar to the SVPWM switching pattern. All switching sequences in sector 5 are $\{[OOO] \rightarrow [NPO] \rightarrow [NPN] \rightarrow [NPO] \rightarrow [OOO]\}$. The transient interval for switching changing in three phases is given by:

$$T_a = \frac{t_0}{2},\ T_b = \frac{t_0 + t_M}{2},\ T_c = \frac{t_0}{2} \tag{19}$$

where T_a, T_b and T_c are the time interval of each phase vector. In the next section, when the reference vector is located in Section 6, the reference voltage is synthesized as:

$$\vec{V_{ref}} = \frac{1}{T_s}\left(\vec{V_0}t_0 + \vec{V_{16}}t_{16} + \vec{V_9}t_9\right) \tag{20}$$

where $t_{15} = t_L$ and $t_9 = t_M$. Then these triple vectors can be defined in (21), (22) and (23) and their dwell times are expressed in (24), (25) and (26), where the permissible range of the reference vector angle is considered as $\frac{5\pi}{6} \leq \theta \leq \pi$. Then, the synthesis switching sequences in sector 6 are introduced with the following statement: $\{[OOO] \rightarrow [NPO] \rightarrow [NPP] \rightarrow [NPO] \rightarrow [OOO]\}$.

$$\vec{V_0} = 0 \tag{21}$$

$$\vec{V_9} = \frac{\sqrt{3}}{3}B\frac{V_{dc}}{2}\ \measuredangle\frac{5\pi}{6} \tag{22}$$

$$\vec{V_{15}} = \frac{2}{3}B\frac{V_{dc}}{2}\ \measuredangle\pi \tag{23}$$

$$t_L = \sqrt{3}\,M\,T_s\sin(\pi - \theta) \tag{24}$$

$$t_M = 2M\,T_s\sin\left(\frac{5\pi}{6} - \theta\right) \tag{25}$$

$$t_0 = T_s - t_L - t_M \tag{26}$$

The ST time interval in the ZSI topology is a key design parameter, which should be carefully chosen. This means that in the proposed topology, the reference vector should be defined by ST states. Therefore, the improved reference voltage $\vec{V_{ref}}$ and the sampling time T_s are determinate as:

$$\vec{V_{ref}}T_s = \vec{V_0}t_0 + \vec{V_L}t_L + \vec{V_M}t_M + \vec{V_{ST}}t_{ST} \tag{27}$$

$$T_s = t_0 + t_L + t_M + t_{ST} \tag{28}$$

where $\vec{V_{ST}}$ is the ST voltage vector across ST time intervals (t_{ST}) as presented in Table 1. As the ST and NST states are described in Tables 2 and 3, it is worth-mentioning that the UST and DST states are never generated if an appropriate sector and switching sequence are adopted. Moreover, the output voltage waveform is not affected by the proposed ST states, because the ST states have the same effect as the zero vectors have. Therefore, the ST time transitions are sectionalized into two equal parts which are supposed to be inserted between medium vectors and zero ones, due to symmetrical characteristic satisfaction, as shown in Figure 8. Assuming that $\vec{V_{ref}}$ is located in sector 5, then the ST interval insertion is applied to phase A, according to Table 4. Formerly, the [SOO] ("S" denotes the ST state) is going to be added to the reference frame vectors. Since the t_{ST} affects the zero vectors, the new modified dwell time of these vectors (t'_0) is calculated as:

$$t'_0 = t_0 - t_{ST} \tag{29}$$

Table 4. Switching vectors during ST intervals.

Sector	Switching Vectors During ST Intervals
S_1	$[OOO], [OOS], [PON], [PNN], [PON], [OOS], [OOO]$
S_2	$[OOO], [SOO], [PON], [PPN], [PON], [SOO], [OOO]$
S_3	$[OOO], [OSO], [OPN], [PPN], [OPN], [OSO], [OOO]$
S_4	$[OOO], [OOS], [OPN], [PNN], [OPN], [OOS], [OOO]$
S_5	$[OOO], [SOO], [NPO], [NPN], [NPO], [SOO], [OOO]$
S_6	$[OOO], [OSO], [NPO], [NPP], [NPO], [OSO], [OOO]$
S_7	$[OOO], [OOS], [NOP], [NPP], [NOP], [OOS], [OOO]$
S_8	$[OOO], [SOO], [NOP], [NNP], [NOP], [SOO], [OOO]$
S_9	$[OOO], [OSO], [ONP], [NNP], [ONP], [OSO], [OOO]$
S_{10}	$[OOO], [OOS], [ONP], [PNP], [ONP], [OOS], [OOO]$
S_{11}	$[OOO], [SOO], [PNO], [PNP], [PNO], [SOO], [OOO]$
S_{12}	$[OOO], [OSO], [PNO], [PNN], [PNO], [OSO], [OOO]$

As the new inserted intervals are symmetrically sectionalized, the improved transition times of three phases (T'_a, T'_b, T'_c) are expressed as:

$$T'_a = T_a - \frac{t_{ST}}{2} \tag{30}$$

$$T'_b = T_b \tag{31}$$

$$T'_c = T_c \tag{32}$$

It is obvious that the switching vector during ST interval insertion in sector 5 belongs to $\{[OOO] \rightarrow [SOO] \rightarrow [NPO] \rightarrow [NPN] \rightarrow [NPO] \rightarrow [FOO] \rightarrow [OOO]\}$. After that, as the reference vector moves to sector 6, the ST interval is inserted into the phase B switching period and the modified time intervals are expressed as:

$$T'_a = T_a \tag{33}$$

$$T'_b = T_b - \frac{t_{ST}}{2} \tag{34}$$

$$T'_c = T_c \tag{35}$$

The switching vector during ST interval insertion in sector 6 belongs to $\{[OOO] \rightarrow [OSO] \rightarrow [NPO] \rightarrow [NPP] \rightarrow [NPO] \rightarrow [OSO] \rightarrow [OOO]\}$. The complete sequence selections at all ST sites are represented in Table 4.

4. Dead Time Impact on CMV Cancelation

The dead time (t_d) effects on CMV elimination are documented in [29]. As power switches such as insulated gate bipolar transistors (IGBTs) and metal oxide semiconductor field effect transistors (MOSFETs) do not turn on instantaneously, an adverse effect on CMV suppression is expected. Figure 9a represents the ideal scenario where the dead time requirement is not necessary. However, real power switches require finite time to turn-on. In order to prevent the shoot-through condition, the dead time condition will force the CMV not be zero, as can be verified in Figure 9b. Considering that the value of t_d is taking into account the trigger switch gate pulses according to the $sign(I)$. $dv/dt < 0$ condition, CMV high-frequency pulses can be eliminated.

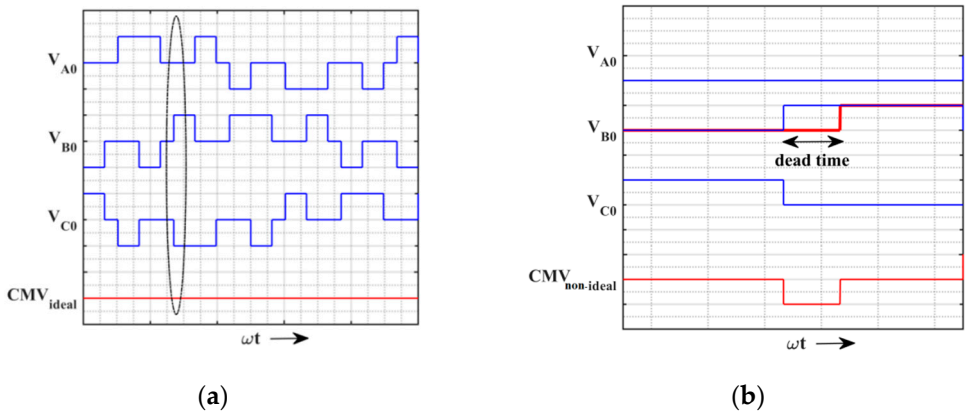


Figure 9. CMV mitigation: (**a**) The CMV in ideal condition [2]; (**b**) the CMV in real condition (needs compensation).

In order to reduce the dead time contribution on CMV generation, it is proposed that the dead time transition interval is incorporated into the reference voltage equation as:

$$\vec{V}_{ref}T_s = \vec{V}_0 t_0 + \vec{V}_L t_L + \vec{V}_M t_M + \vec{V}_{ST} t_{ST} + \vec{V}_d t_d \tag{36}$$

$$T_s = t_0 + t_L + t_M + t_{ST} + t_d \tag{37}$$

where $\vec{V}_d$ is the dead time voltage vector. The changes of the switches in this mode are visible in Figure 10a. The CMV is zero at all instants of simulation. Currently, in phase "A", for instance, these principle operations, transient states and the impact of dead time are investigated. There are two analysis sub-sections: The first one represents the positive current ($sign(I_a) > 0$) and the second one will discuss about the negative current flow through the load ($sign(I_a) < 0$). These switching transitions are depicted in Figures 10 and 11, respectively. For better realization, the Figure 10a is explained as below: In this case, S_3 and S_4 are switched on and voltage V_{a0} is equal to $-V_{dc}/2$. The final state is to reach the condition shown in Figure 5; that switches S_2 and S_3 are turned on and voltage V_{a0} is zero. In this transient mode, switch S_2 starts to turn on, but due to the dead time, until this switch is completely turned on, current I_a still passes through the two previous switches. In the next section, the proposed constructed laboratory prototype would be tested in the power electronics and drive laboratory of our university.

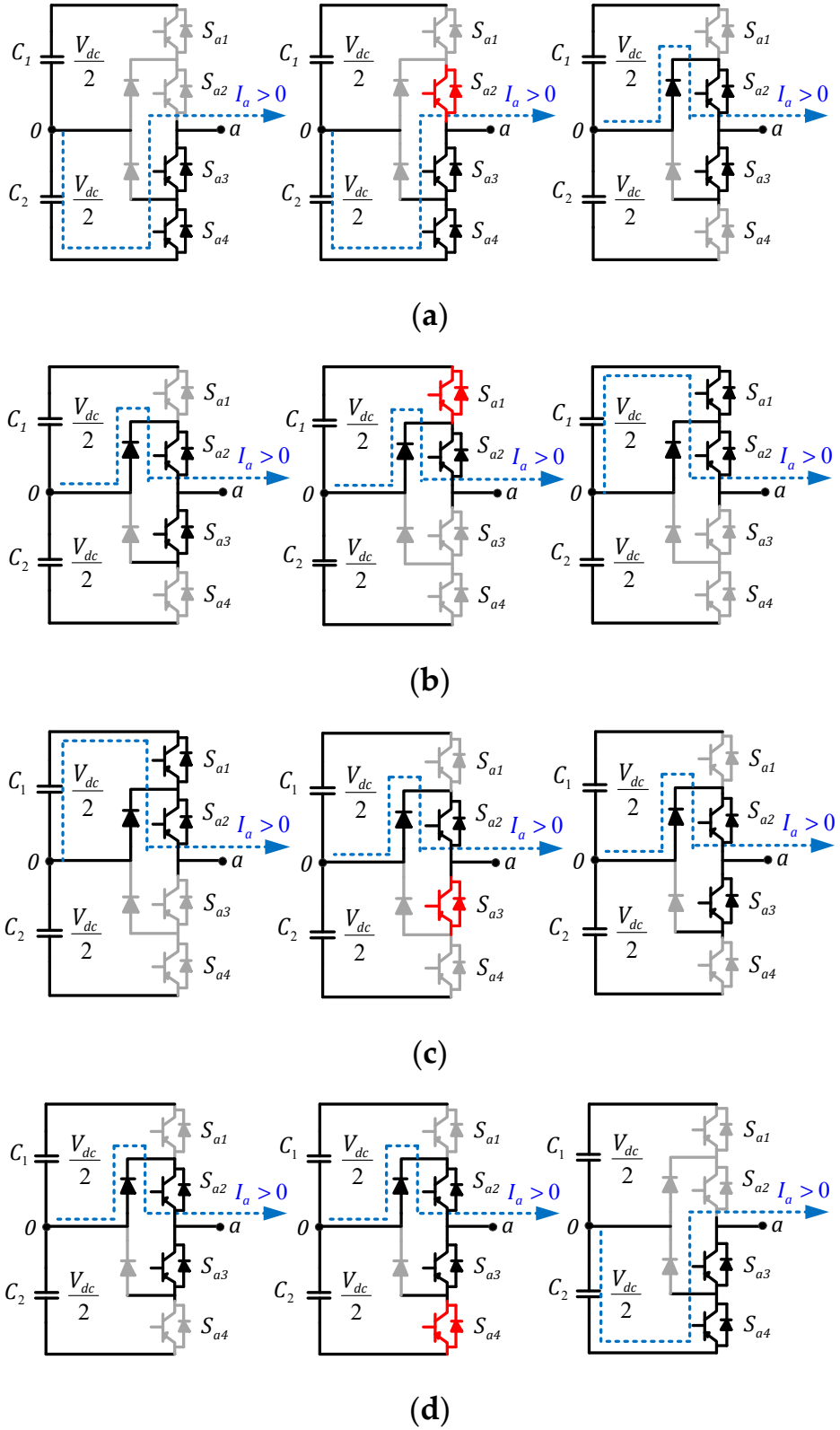


Figure 10. Transient state of switching at positive current: (**a**) From $-V_{dc}/2$ to 0; (**b**) from 0 to $+V_{dc}/2$; (**c**) from $+V_{dc}/2$ to 0; (**d**) from 0 to $-V_{dc}/2$ [2].

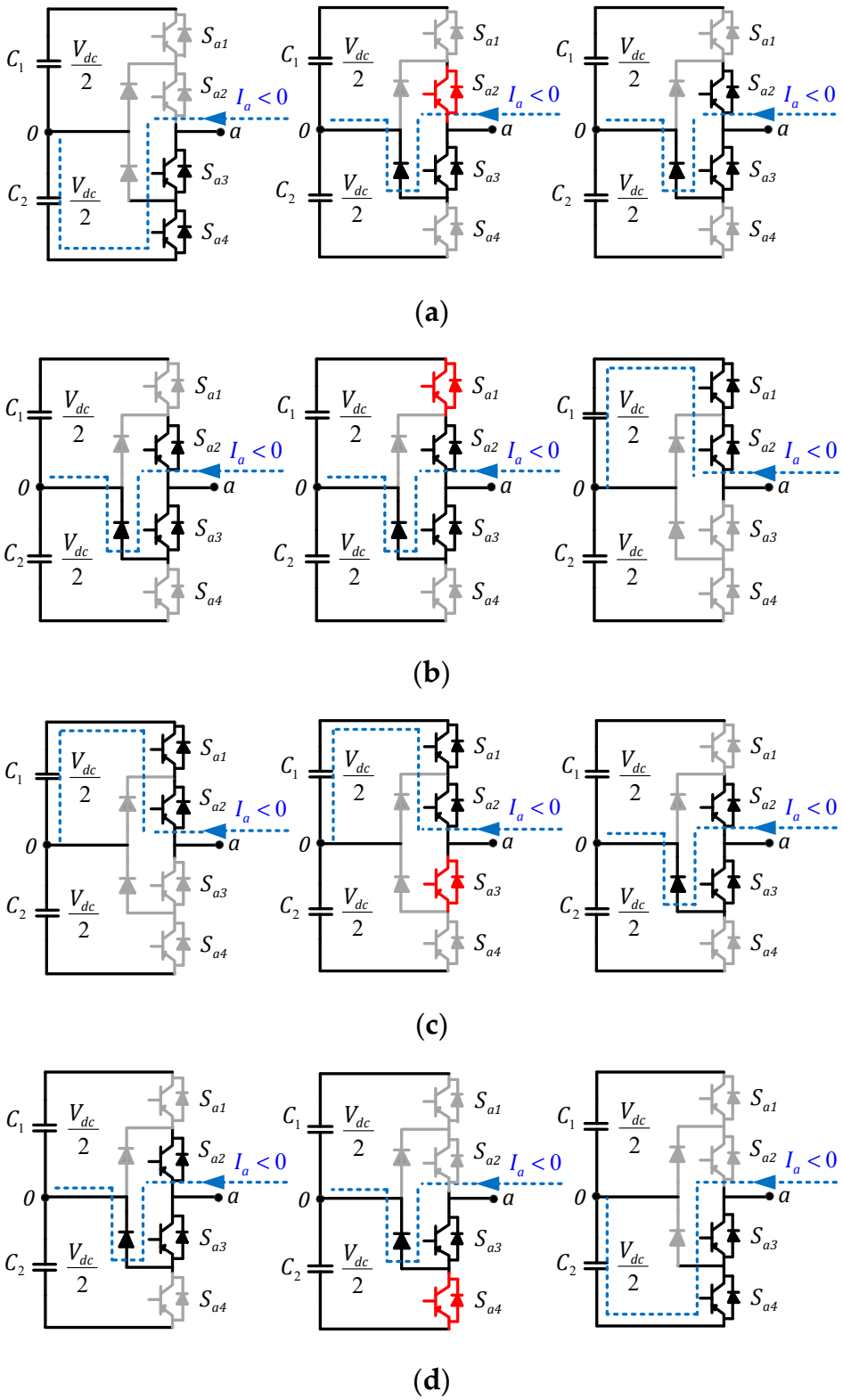


Figure 11. Transient state of switching at negative current: (**a**) From $-V_{dc}/2$ to 0; (**b**) from 0 to $+V_{dc}/2$; (**c**) from $+V_{dc}/2$ to 0; (**d**) from 0 to $-V_{dc}/2$ [2].

5. Verification of CMC Cancelation through Experimental Evaluation

The prototype was built according to the specifications shown in Table 5. A general view of the test bench can be seen in Figure 12. A base switching frequency of 12 kHz was used for synthesizing

three-phase voltage waveforms at 50 Hz. Available laboratory resources are restricted to low power tests. Hence, load maximum rated power is 300 W and fixed at unity power factor. The SVPWM variant presented in this paper is compared to the SPWM switching scheme. Figure 13 depicts CMV output regarding the two PWM switching schemes. In conventional SPWM CMV cancellation is not possible. In addition, it can generate high-frequency pulses associated with the CMV pattern. As for the proposed SVPWM variant, the CMV profile is virtually null thanks to the dead time compensation algorithm implemented in the novel switching scheme. The three-phase load current with a semi-pure sinusoidal waveform is represented in Figure 14a. The current total harmonic distortion (THD) is computed as 1.12%, which is in the standard range. Figure 14b shows the input voltage and capacitor voltages jointly, which imply that the dead time compensation does not have any bad effect on the capacitor voltage.

Table 5. Prototype Main Specifications.

Parameter	Value
DC voltage (V_{dc})	150 V
Line frequency (f_{line})	50 Hz
Switching frequency (f_{sw})	12 kHz
Output power (P_{out})	300 W
Filter inductance (L_f)	2 mH
Filter capacitance (C_f)	220 µF
ZSI inductance ($L_{Z-Source}$)	1.5 mH
ZSI capacitance ($C_{Z-source}$)	670 µF
IGBT	*BUP314*
Diode	*DSEI8-06*

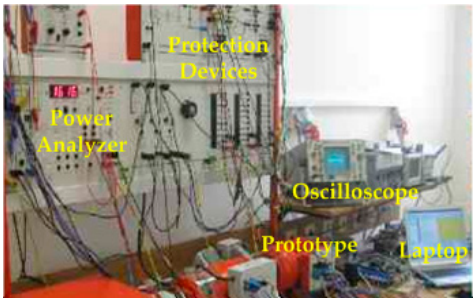


Figure 12. Laboratory implementation setup.

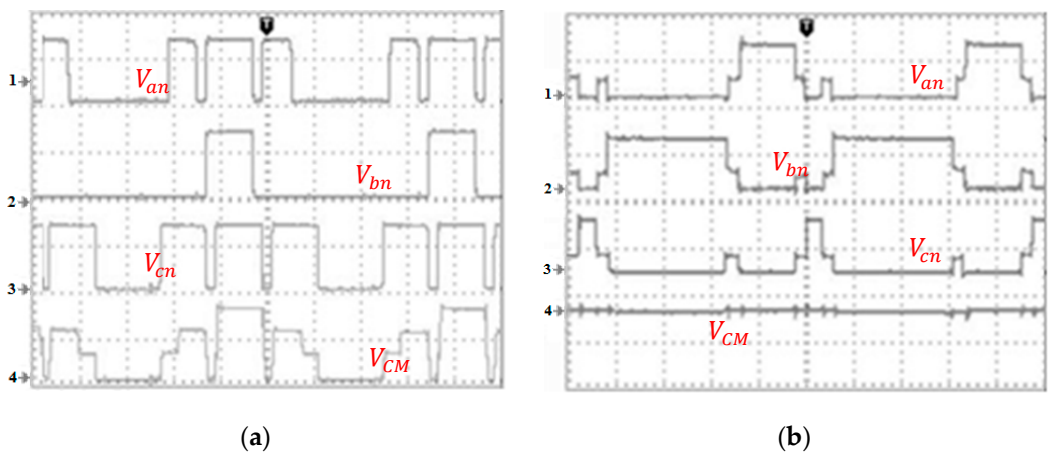
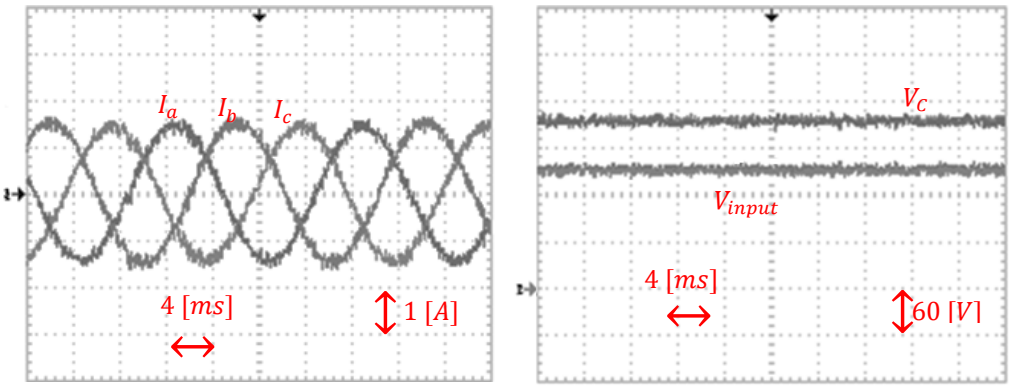


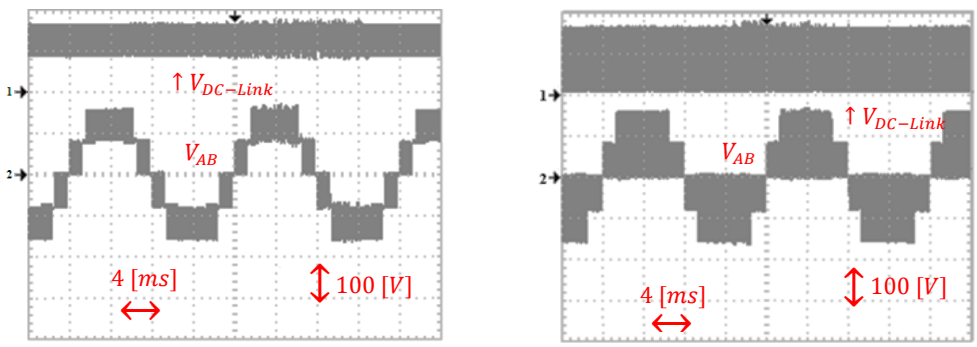
Figure 13. Three phase output voltage and CMV waveforms (100 volts/div and 10 µs time/div): (**a**) SPWM method; (**b**) proposed approach.



(**a**) (**b**)

Figure 14. Three phase load current and input voltages: (**a**) Three phase load current; (**b**) input voltage and capacitors' voltages.

As the proposed method is to resolve the impact of the dead time in the CMV cancellation, it can be observed in Figure 15b that the V_{AB} waveform has higher THD content because V_{a0} and V_{an} remain equal. In the same Figure, the DC input voltage of the PWM inverter running the SVPWM variant reveals a high voltage ripple that goes down to 0V. Nevertheless, it does not compromise the inverter's main function, which is to drive the AC motor. The THD profile was measured and compared to the results of [6,16] in Figure 16. The figure shows a slight increase in this quantity, which is not significant over the switching frequency range under study. This small increase is due to the algorithm implemented to minimize dead time interval. It is worth mentioning that the THD value is still within the acceptable range according to international standards.



(**a**) (**b**)

Figure 15. DC link voltage and line-to-line voltage waveforms: (**a**) SPWM method; (**b**) proposed approach.

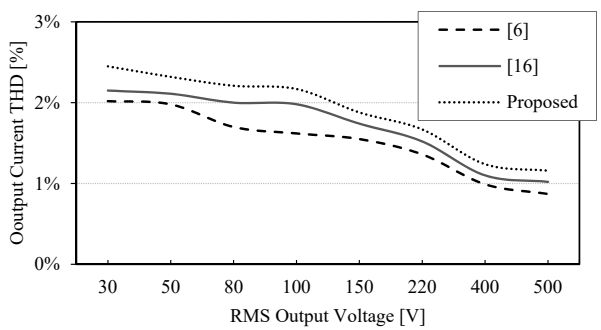


Figure 16. Output current THD comparison as a function of output AC voltage.

In Figures 17 and 18, the effectiveness of applying the dead time compensation is evaluated from an electrical efficiency viewpoint. This implies a need for better performance evaluation to feed the inductive dynamic loads in low voltage distribution networks. All efficiencies calculated are more than 90%, which represents the useful performance. The experimental efficiency analysis is realized in Figure 18 in terms of input voltage variations. As a result, comprehensive comparison is represented in Table 6 to show the effectiveness of the proposed switching algorithm.

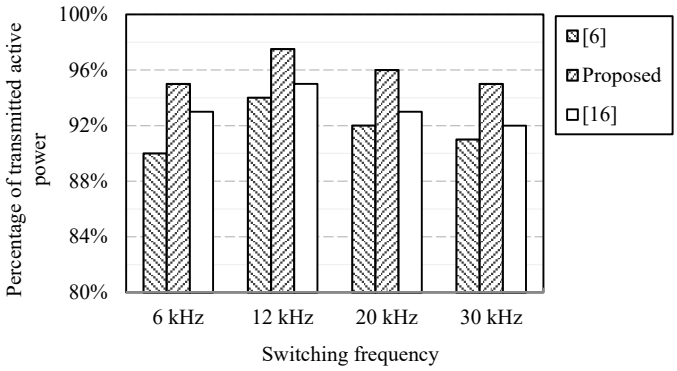


Figure 17. Transmitted active power vs. switching frequency.

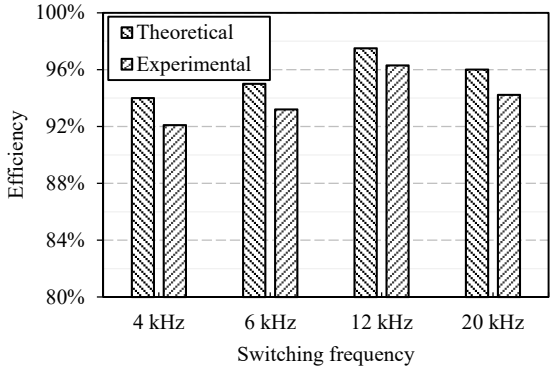


Figure 18. Efficiency analysis in terms of switching frequency.

Table 6. Measured maximum CMV.

Methods	Max{CMV}
[6]	$V_{dc}/6$
[8]	$V_{dc}/2$
[9]	$V_{dc}/6$
[16]	$V_{dc}/\sqrt{3}$
[17]	$V_{dc}/2$
Proposed approach	Zero

6. Conclusions

This paper has presented a variant of the SVPWM algorithm for CMV cancellation in a PWM inverter-driven three-phase motor. The dead time requirement for the proper operation of power switches in a bridge configuration is also a source of high frequency noise, contributing to the sharp edged CMV transitions as well as to an increase in its amplitude. The proposed SVPWM variant is able to eliminate the dead time impact on the CMV level while providing a complete cancellation of it. The pulsating output of the impedance source module is correlated with the shoot-through interval without changing the sinusoidal-shaped waveform of the three-phase output. The impedance source topology provided in the DC power side of structure makes it possible to control the output AC voltage

in both the stepping-up/down modes. The experimental results have shown a slight increase of 0.2% in the output current THD calculation.

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