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Compact Rectifier Circuit Design for Harvesting GSM/900 Ambient Energy

Surajo Muhammad ¹, Jun Jiat Tiang ¹, Sew Kin Wong ¹, Amjad Iqbal ^{1,*},
Mohammad Alibakhshikenari ^{2,*} and Ernesto Limiti ²

¹ Centre For Wireless Technology (CWT), Faculty of Engineering, Multimedia University, Cyberjaya 63100, Malaysia; doguwa_2002@yahoo.com (S.M.); jjtiang@mmu.edu.my (J.J.T.); skwong@mmu.edu.my (S.K.W.)

² Electronic Engineering Department, University of Rome “Tor Vergata”, Via del Politecnico 1, 00133 Rome, Italy; limiti@ing.uniroma2.it

* Correspondence: amjad730@gmail.com (A.I.); Alibakhshikenari@ing.uniroma2.it (M.A.);
Tel.: +60-1128-784-475 (A.I.)

Received: 6 September 2020; Accepted: 29 September 2020; Published: 1 October 2020



Abstract: In this paper, a compact rectifier, capable of harvesting ambient radio frequency (RF) power is proposed. The total size of the rectifier is 45.4 mm × 7.8 mm × 1.6 mm, designed on FR-4 substrate using a single-stage voltage multiplier at 900 MHz. GSM/900 is among the favorable RF Energy Harvesting (RFEH) energy sources that span over a wide range with minimal path loss and high input power. The proposed RFEH rectifier achieves measured and simulated RF-to-dc (RF to direct current) power conversion efficiency (PCE) of 43.6% and 44.3% for 0 dBm input power, respectively. Additionally, the rectifier attained 3.1 V DC output voltage across 2 kΩ load terminal for 14 dBm and is capable of sensing low input power at −20 dBm. The work presents a compact rectifier to harvest RF energy at 900 MHz, making it a good candidate for low powered wireless communication systems as compares to the other state of the art rectifier.

Keywords: RF energy harvesting; impedance matching network (IMN); power conversion efficiency; rectifier; IoT

1. Introduction

The ubiquitous nature of wireless communication technology has over the years attract and gained much attention and contribution from researchers globally [1,2]. Additionally, GSM900/1800, 3G, 4G, Wi-Fi, and the evolving auspicious 5G are among a few dominant wireless technology generation operating daily to cater for human needs and demand [3,4]. Recent development in wireless communication technology gave birth to new and evolving technological innovations. The increasing demand of such invention led to one or more application driver in the areas of IoT, industrial IoT, autonomous driving, smart farming, smart cities, and many more [5,6]. Uninterrupted power supply over remote places limits the potential of wire-based ultra-low powered IoT devices and sensor nodes. which directly restricts their capabilities for security surveillances, smart farming, and other related applications besides a copper loss [5–7]. One of the main challenges with the evolving ultra-low powered IoT devices is energy storage limitation. These, in turn, increase the need for RFEH systems. To over come the major challenges with traditional battery-based systems to charge/maintain/replace a battery. RFEH is believed to be a promising technology through direct power or battery recharging from abundant electromagnetic (EM) energy radiating in the environment. The technology can be deployed in low-powered devices for security surveillance, smart farming and many more [5–8]. Initially, the concept of energy harvesting started to evolve in the 1990s along with Tesla finding’s on electrical energy conversion from an EM wave [5]. RF power system typically comprises an antenna, IMN,

a rectifying diode, a storage element (DC pass filter), and a terminal load. A combination of five circuit elements gives rise to rectenna. A rectenna without the antenna component is categorized as a rectifying circuits. Figure 1 provides a block diagram containing the key components of rectenna. The matching network (MN) and the rectifier circuit play an important role in the RFEH system. MN is aim at ensuring optimum energy transfer between the receiving antenna and the load, and the latter transform the scavenged RF EM signals into a usable DC output voltage. RFEH module can be deployed in a sensitive and critical environment such as autonomous driving, security surveillance, and healthcare systems, for their capability to operate under both environmental and nonenvironmental condition unlike the other forms of energy harvesting system [5]. The operation of rectifying circuit and RFEH system are generally assessed through (PCE). Several RFEH circuits design have been studied and proposed to achieve significant PCE through the use of wide-band, multi-band, dual and single band rectifiers. Among the designs, single-band rectenna used to be more efficient as compared to their wide or broad band counter parts [5,8]. The broadband rectifiers are generally associated with much more circuits complexity, which reduces the overall circuit performance because of parasitics capacitance at the junction of the diode and other lumped elements [8,9]. The authors of [10,11] designed a rectenna with maximum PCE at 37.8% and 28% using -1.5 dBm and -15 dBm input power. To recycle ambient RF signal, a rectenna with 20% efficiency is described in [12] using $62 \mu\text{W}/\text{cm}^2$ (13.27 dBm) input power with a total geometry of 342.55 cm^2 . Several research projects have been developed to accomplish efficient rectenna at relatively low input power [13,14]. An RF rectifier is proposed in [15], the design can achieve up to 33% efficiency at -10 dBm input power at the cost of complex circuit with large electrical length. A maximum PCE of 47.8% and 38% is highlighted in [16,17], using an input power between (5–14 dBm), respectively. The authors of [13] also worked on rectifier circuit and realized 50% maximum PCE using 21 dBm solar panel. A rectenna that achieved up to 24% PCE is proposed in [14], using -20 dBm input power with help of an antenna array and rectifier with a total geometry of 32.4 cm^2 .

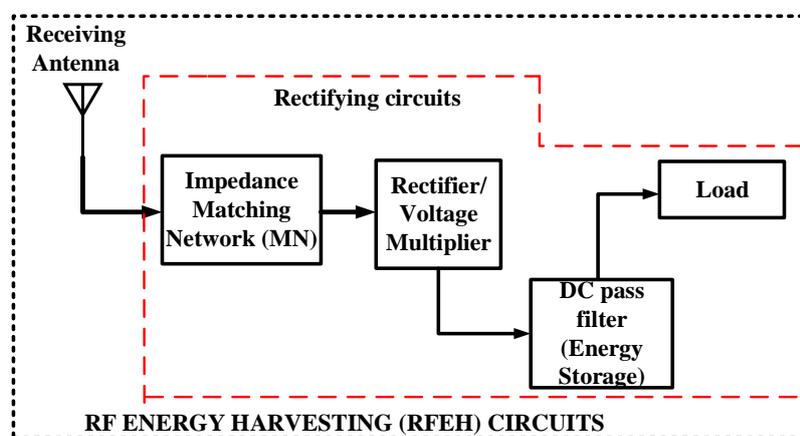


Figure 1. Block diagram of RF energy harvesting circuits.

Many foregoing types of research in the RFEH system focused on a much higher frequency between GSM/1800 to WLAN/5200 to achieve compactness. The operational frequency contributed significantly to achieving a compact RFEH circuit [7–18]. The RF spectral survey from the open literature and the one carried out in this work, using (Aim TTI PSA6005 6 GHz RF spectrum analyzer), come out with a notable result surrounding the lower GSM/900 band towards generating higher available ambient RF power [14,15]. This paper, proposed a compact 3.51 cm^2 rectifier at 900 MHz using simple L-section MN. Conversely, the designed is a good candidate for harvesting RF energy in ambient environment with capability of sensing RF input power below -20 dBm integrable with low powered IoT devices. In the remaining sections of this work, Section 2 presents a rectifier circuit

design and analysis, Section 3 highlights the result of a finding of the proposed rectifier and Section 4 provides the concluding remarks. The following outlines the main contribution of this work:

- To the best of our knowledge, this is the compact RFEH rectifier as compares to state of the art rectifiers at 900 MHz.
- This research targets an energy harvesting rectifier that works over GSM/900 to cover long and remote places suitable for low powered IoT devices and sensor nodes.
- The proposed design can receive an RF input signal at less than -20 dBm and also provides detailed circuit and performance analysis.

2. Rectifier Circuit Design and Analysis

The voltage appears at the end of an RFEH antenna is considerably of small quantity and as well analogous to sinusoidal signal. A conditioning circuit across the load terminal is an important figure to improve the output DC signals of the RFEH module. Diode(s), MN, and load terminal are primary components to the rectifying circuits. The diode(s) is playing a vital role in converting the accessible ambient RF power into a usable DC supply. The MN minimizes the reflection losses for RF input power received by the antenna. The low powered RFEH MN need to be simple in design with minimum losses.

2.1. Transmission Line and Input Impedance Matching Network

A 50Ω microstrip transmission line width and length to match the antenna with MN and voltage multiplier was first to design using FR-4 substrate ($\epsilon_r = 5.4$, $h = 1.6$ mm, and $\tan\delta = 0.02$). The substrate is chosen for its low cost, light weight, and ease of fabrication [7]. ADS LineCal operator is applied to compute and optimized the proposed width and length of the line at 2.7 mm and 30 mm, respectively. MN is significant part of the rectifier circuits. The design process of MN is a challenging task because the rectifier input impedance (Z_{in}) is controlled by: operating frequency (f_c), input power (P_{in}), diode inconstant internal resistance (R_d) and terminal load (R_L) [19].

Figure 2 shows L-section MN to match the impedances between the source and the load. The proposed model reduces circuit complexity using two simple inductive (L_m) and capacitive (C_m) reactive elements. The inductor (L_m) plays a vital role towards enhancing the input signal getting into the rectifier and the capacitor (C_m) enhances the rectifier matching [19]. The MN parameters can be computed by negating source and load imaginary part and equating their real part at the design frequency as illustrated in Equations (1)–(5). The equivalent power source from the antenna (P_s) is analogous to the antenna available power (P_{av}) passing through the transmission line and the MN. Other related reference power notation in the circuit model includes rectifier input power (P_{in}) and the output power consumed by the load terminal (P_L).

Equating the real part of the antenna with the rectifier input impedance we get:

$$R_{ant} = R_{in} \cdot \left(\frac{1}{1 + Q^2} \right) \quad (1)$$

where R_{in} = rectifier input impedance, R_{ant} = source impedance, and the quality factor Q is given by:

$$Q = \sqrt{\frac{R_{in}}{R_{ant}} - 1} \quad (2)$$

To determine the reactance parameters, the quality factor Q can be express as the ratio of imaginary (reactive) part of the impedance to the respective real (resistive) components as:

$$Q = \frac{Im(Z)}{Re(Z)} = \frac{Im\left(\frac{1}{\frac{1}{R_{in}} + j\omega_0 C_{in} + \frac{1}{j\omega_0 L_m}}\right)}{Re\left(\frac{1}{\frac{1}{R_{in}} + j\omega_0 C_{in} + \frac{1}{j\omega_0 L_m}}\right)} = \frac{R_{in}}{\omega_0 L_m} - \omega_0 C_{in} R_{in} \quad (3)$$

where C_{in} = reactive components of the load impedance operating at frequency ω_0 , using Equation (3) the inductance L_m of the network is given as:

$$L_m = \frac{R_{in}}{\omega_0(Q + \omega_0 C_{in} R_{in})} \quad (4)$$

L-section capacitance C_m can be computed by setting the imaginary part of Equation (3) to zero as:

$$C_m = \frac{R_{in}}{L_m(R_{in} - R_{ant})} \cdot \frac{1}{(\omega_0^2 - \frac{1}{L_m C_{in}})} \quad (5)$$

A two-element MN ($L1$ and $C1$) is designed at 900 MHz using a 50Ω transmission line as (R_{ant}), terminated with a $2 \text{ k}\Omega$ load. The numerical values of $L1$ and $C1$ were computed at 55 nH and 0.5 pF , respectively. The parameters were transfer into ADS simulation software using ideal component palette. Because of the effects of the transmission line in the circuits, the lumped elements need to be tune and optimize. ($L1$) and ($C1$) were compensated with -10 nH and $+0.5 \text{ pF}$, and the rectifier is matched at 45 nH and 1 pF , respectively. The circuit is further tuned by replacing the ideal elements with *muRata* equivalent surface mount device (SMD) in the ADS library at 27 nH and 2 pF .

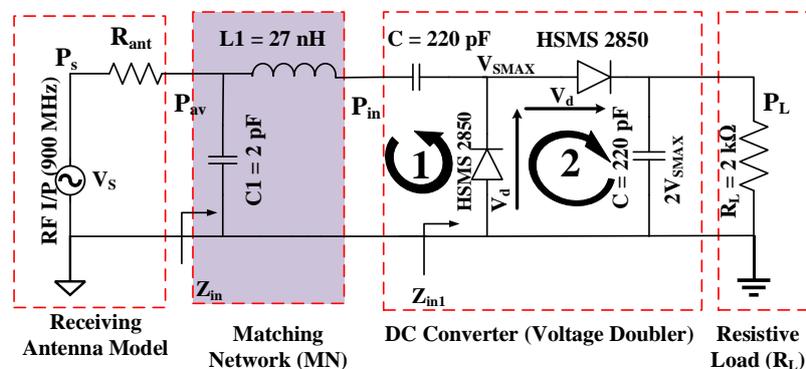


Figure 2. Detailed circuit configuration of the proposed rectifier.

2.2. Rectifier Design

Rectifying circuits are of different configuration layout. The circuits can be achieved as a single series or shunt rectifier diode, voltage doubler rectifiers, up to the level of multistage and cascaded rectifiers. The authors of [9] highlights an extensive study on various types of rectifier circuits topology. Rectifier selection to operate at high frequency need to have: reliable power response, and the ability to manage power with minimal dissipation [7] for efficient and effective power harvesting. A single-stage voltage multiplier configuration is a suitable candidate to be deployed in RFEH circuits as compared to a single series/shunt half-wave configurations. An RF rectifier circuit with a single-stage voltage multiplier is more efficient with higher output power compares with single series/shunt half-wave rectifiers. Single-stage voltage multiplier rectifiers also offer fewer losses in contrast to multistage rectifiers for a low-powered RF harvester [9]. The proposed rectifier is built based on a voltage

multiplier topology with a pair of HSMS-2850 diode (SOT-323 layout), as shown in Figure 2. The diode is a suitable candidate for low power RF application with a small junction capacitance of 0.18 pF and a minimum detectable voltage of 150 mV at 0.1 mA [5]. The rectifier junction capacitance (C) is controlled by the operating frequency f_c and voltage as express in Equation (6).

$$C = I \cdot \frac{dt}{dV} \quad (6)$$

where C is the capacitance of the capacitor with current I passing through junction diode at the rate of non linear voltage “ V ”.

The antenna then receives and transmits the reactive AC power into the rectifier as express by the equivalent wave Equation (7) [9]. During the negative half-wave AC cycle diode $D1$, become forward bias and charges (C) in label (1) to (V_{SMAX}). At the positive half-wave AC cycle, diode $D1$ is reverse bias blocking the DC voltage in label (1) from discharging, and diode $D2$ in label (2) change into forward bias. The reserve (V_{SMAX}) in label (1) and diode $D2$ synchronously sum up the output DC voltage to ($2V_{SMAX}$) onto the capacitor (C) in label (2), which discharges through the load terminal (R_L) as describe in Equations (8) and (9).

$$V_S = V_{SMAX} \sin \omega t \quad (7)$$

where V_{SMAX} is the amplitude of the RF input signal received at the output of the MN operating at frequency ω [20].

$$-V_{SMAX} - V_{C1} + V_{C2} + 2V_d = 0 \quad (8)$$

where V_d is the forward bias voltage of the rectifying diode, and

$$V_{C2} = V_{SMAX} + V_{C1} - 2V_d, \text{ and}$$

$$V_{C1} = V_{SMAX}$$

$$V_{C2} = 2V_{SMAX} - 2V_d \quad (9)$$

3. Results and Discussion

The propose rectifier is fabricated on a low-cost commercial FR-4 board with a total dimension 45.4 mm \times 7.8 mm \times 1.6 mm connected via 50 Ω SMA probe. A pair of small crocodile clip is used to connect the rectifier across the load terminal to measure the output parameters as seen in Figure 3b. Figure 3a also provides layout model of the rectifier prototype.

Equation (10) provides a wheeler’s transmission line width equation that portrays the effects of (W) on the rectifier matching [21]. Decreasing (W) below the designed value causes a direct rectifier mismatch at the proposed frequency. Increasing (W) above the designed value shifted the rectifier operating frequency by 20 MHz in addition to impedance mismatch. The transmission line length is computed through a guided wave at $\lambda_g/4 = 42.5$ mm and is optimized at 30 mm.

$$Z_o = \frac{120\pi}{\sqrt{\epsilon_e}} \left[\frac{W}{h} + 1.393 + 0.667 \ln \left(\frac{W}{h} + 1.444 \right) \right]^{-1} \quad (10)$$

where Z_o is the characteristic impedance of the line, W = width of transmission line, h = height of the substrate, and ϵ_e gives the effective dielectric constant of the substrate.

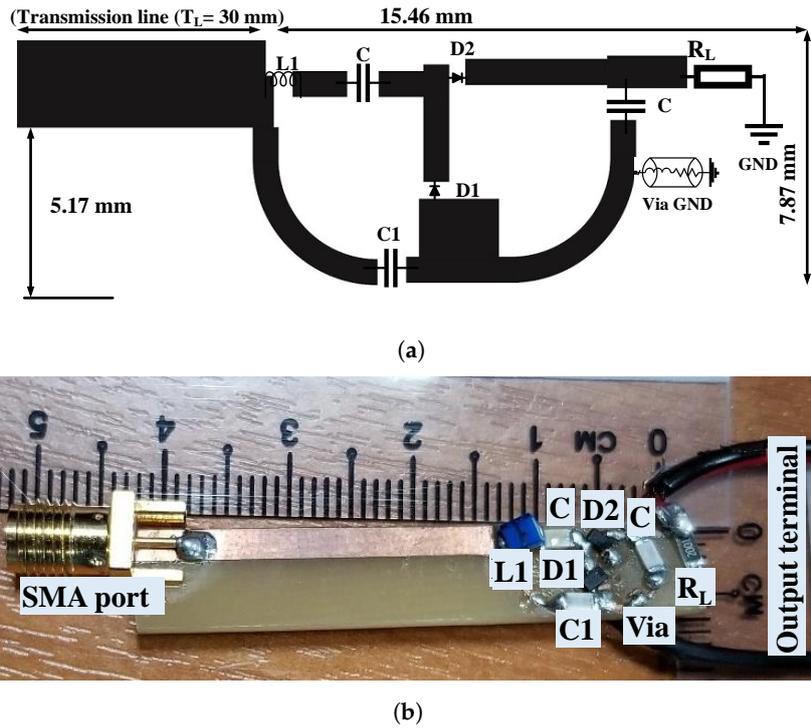


Figure 3. Rectifier proposed topology: (a) EM model layout, (b) fabricated prototype.

To evaluate the rectifier performance at the design frequency, L-section MN undergo a parametric study. Figure 4a depicts the simulated reflection coefficient versus frequency at different values of the inductor ($L1$). The design frequency shifted to about 1.1 GHz for an inductance value from 27 nH to 18 nH. Following the inductive reactance properties, frequency increases the current flowing through the inductor, which lowers the inductance value in the circuits [3–5,13]. Figure 4b also shows the effect of capacitance ($C1$) in the MN, varying the capacitance from 2 pF to 10 pF deteriorates the rectifier matching. Hence, lowering or increasing the capacitance value leads to rectifier mismatched which can render the rectifying circuit inefficient [9,20].

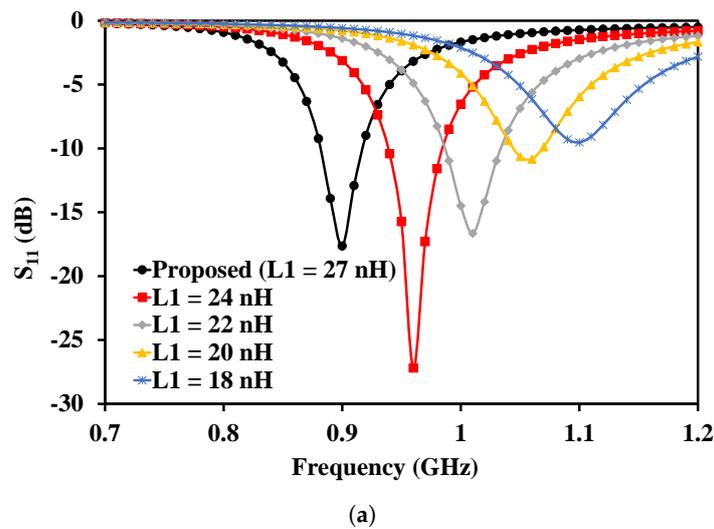


Figure 4. Cont.

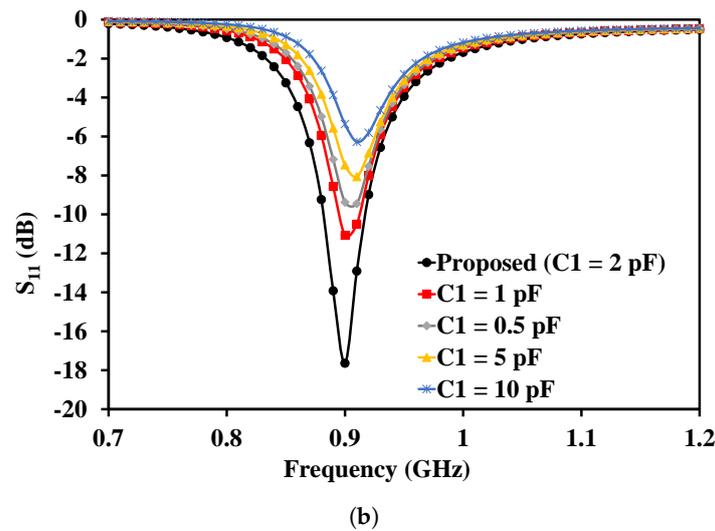


Figure 4. Simulated reflection coefficient of the rectifier for: (a) Inductance (L_1) (b) Capacitance (C_1).

To analyze the PCE of the proposed rectifier, Figure 5a presents the result of the load terminal (R_L) sweep at various input power levels (from -15 dBm to 10 dBm in step of 5 dBm). The result shows that the efficiency increases with an increase of input power across the load which agreed well with Equation (7) [5–22]. The rectifier achieves a maximum PCE along the $2\text{--}4$ k Ω load terminal in both cases. The design shows a low PCE for -15 dBm with an efficiency greater than 20% for a load above 2.5 k Ω . A 60% high efficiency is also observed around the $2\text{--}4$ k Ω load for $+10$ dBm input power.

Figure 5b presents the simulated and measured reflection coefficient (S_{11}) of the proposed rectifier at 900 MHz. The design achieved a simulated and measured -10 dB bandwidth of 45 MHz ($880\text{--}925$ MHz) and 46 MHz ($870\text{--}916$ MHz) respectively. A vector network analyzer (E5062A) from Agilent Technologies is used to measure the (S_{11}) of the rectifier for -20 dBm input power level.

Equation (12) provides a relation that describes the rectifier ability in converting the received RF signal in to a usable output DC signal known as (PCE) in terms of output and input power. To determine the simulated output DC voltage and efficiency over a range of frequency, input power and a terminal load. A large signal s-parameter (LSSP) and harmonic balance (HB) simulation modules that coexist in ADS is deployed into the design owing to the non-linear characteristics of the rectifying diode [5–11]. A 12 GHz APSIN12G signal generator sweep from -30 dBm to 10 dBm input power is used to measure the rectifier output DC voltage across the 2 k Ω load terminal. The measured result is in good agreement with simulation, as depicted in Figure 6a. The rectifier can receive an RF input signal at -30 dBm with the capability of harvesting 3.1 V for both simulated and measured results at 14 dBm and 16 dBm, respectively. Equation (11) provides the rectifier output DC voltage from Equation (9) [9,23].

$$V_{DC} = V_{C2} \tag{11}$$

$$\eta_{PCE}\% = \frac{P_{DC}}{P_{in}} \times 100\% = \left(\frac{V_{DC}^2}{R_L}\right) \times \left(\frac{1}{P_{in}}\right) \times 100\% \tag{12}$$

where η_{PCE} is the power conversion efficiency, P_{DC} is DC output power across the load R_L and V_{DC} gives the output DC voltage.

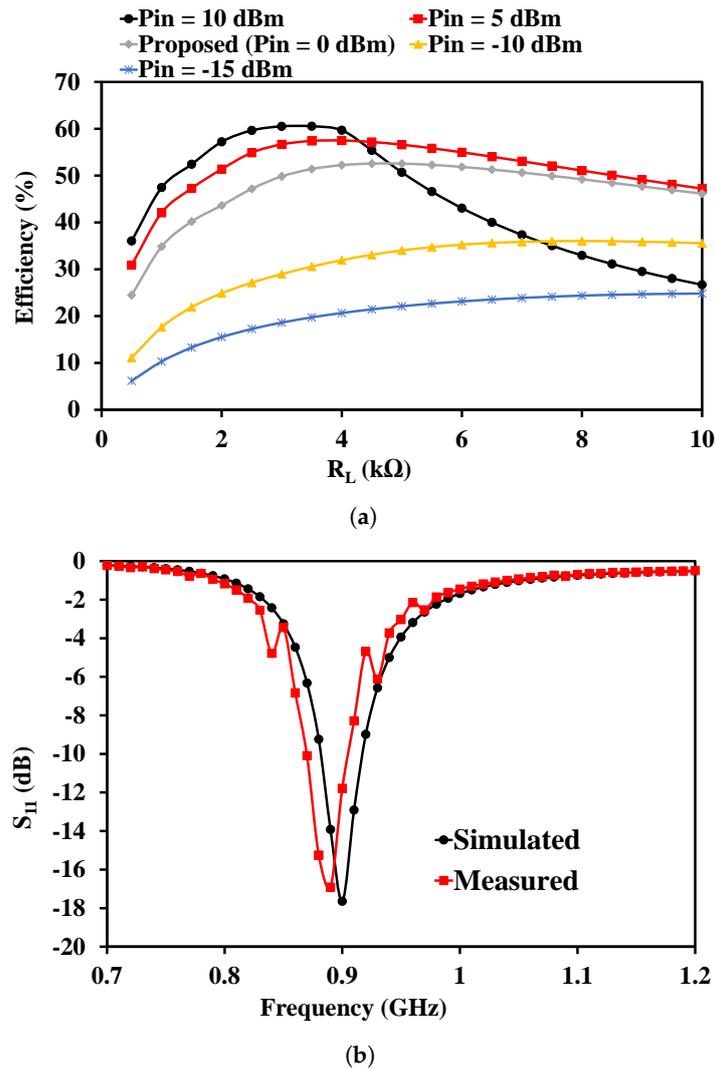


Figure 5. (a) Simulated efficiency sweep against load terminal (R_L) at various input power (P_{in}). (b) Simulated and measured reflection coefficient of the proposed rectifier for -20 dBm input power.

Figure 6b presents the simulated and measured PCE across the 2 k Ω load terminal, and the rectifier achieves a PCE of 44.3% and 43.6% for 0 dBm input power, respectively. The rectifier experiences a drop in measured efficiency because of nonlinear characteristics of the diode as reported in the datasheet, in connection with other losses from the circuit board (Such as SMA connector probe, interconnecting transmission lines, soldering, and chip-component tolerant losses) [3].

Table 1 provides a comparison table of the proposed design with other related works in the literature. The authors of [10,11] presents an energy harvester with about times larger in electrical length than the proposed design. The authors of [13] did not record the amount of input power at which the rectifier achieves its maximum PCE, but uses a solar antenna [24] with 21 dBm capacity and a much larger rectifier. The authors of [14] also comes out with a harvesting circuit without describing the MN used besides rectifier large electrical length. A much lower PCE at high input power is reported in [16,17]. The proposed design in the open literature target high-frequency band rectifier starting from GSM/1800—WLAN/5200 which contributes to achieving rectifier compactness. The proposed design in this work offers a compact size rectifier capable of harvesting RF signal over a long-range cover by GSM/900.

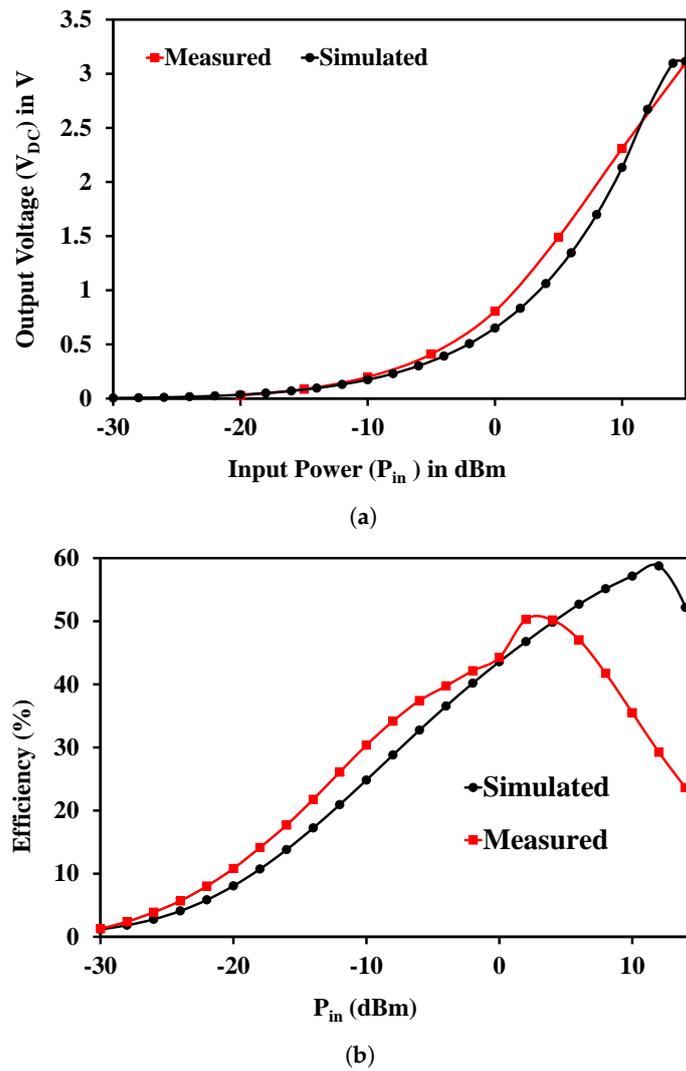


Figure 6. Simulated and measured: (a) Output DC voltage sweep against the input power (b) PCE sweep over an input power P_{in} at 900 MHz.

Table 1. Comparison of the proposed rectifier and related.

Ref	Electrical Size (λ_g)	η_{PCE} (%) @ P_{in} (dBm)	Frequency (GHz)	Diode
[10]	$1.03\lambda_g \times 1.03\lambda_g$	37.8%@-1.5	2.45	HSMS286C
[11]	$0.76\lambda_g \times 0.84\lambda_g$	28%@-15	2.45	HSMS2850
[13]	$3.86\lambda_g \times 4.89\lambda_g$	50%@NA	1.8/2.1	SMS7630
[14]	$0.88\lambda_g \times 0.57\lambda_g$	24%@-20	1.8/2.5	HSMS2850
[16]	$0.34\lambda_g \times 0.21\lambda_g$	(47.8, 37, 46.7, 42)% @(14, 12, 13, 12)	0.87/1.27/ 2.02/2.38	HSMS2860
[17]	$0.38\lambda_g \times 0.22\lambda_g$	(38, 37, 18, 12.5)% @5	1.3/1.7/ 2.4/3.6	SMS7630
This work	$0.31 \lambda_g \times 0.05 \lambda_g$	50.2%@2	0.90	HSMS2850

4. Conclusions

This paper, proposes the design and construction of a compact rectifier at a 900 MHz GSM band, using HSMS-2850 Schottky diode. A transmission line and an L-section impedance matching network are designed from the closed-form equations, to match the input impedance of the rectifier with 50Ω . The circuit undergoes parametric tuning from an ideal to model component to achieve better performance and minimizes the effects of the transmission line in the network. The fabricated prototype can receive an ambient RF signal below -20 dBm and achieved 50.2% and 49.1% maximum PCE for both simulated and measured results at 14 dBm and 2 dBm, respectively. Similarly, the circuit reaches an output DC voltage of 3.1 V for simulated and measured results at 14 dBm and 16 dBm, respectively using a $2 \text{ k}\Omega$ load terminal. The proposed rectifier occupies a total of 351 mm^2 ($0.31\lambda_g \times 0.05\lambda_g$) on the PCB circuit board, offering efficiency and compactness improvement as compares to other recent designs making it suitable for various compact energy harvesting applications.

Author Contributions: Conceptualization, S.M.; methodology, S.M. and M.A.; software, S.M.; validation, S.M., A.I., M.A. and E.L.; formal analysis, S.M.; investigation, S.M.; resources, J.J.T. and S.K.W.; data curation, S.M.; writing—original draft preparation, S.M.; writing—review and editing, S.M. and A.I.; visualization, S.M., M.A. and E.L.; supervision, J.J.T. and S.K.W.; project administration, J.J.T. and S.K.W.; funding acquisition, J.J.T. and S.K.W. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by TM R&D Malaysia under project number MMUE/190001.

Conflicts of Interest: The authors declare no conflict of interest.

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