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A Low-Distortion 20 GS/s Four-Channel Time-Interleaved Sample-and-Hold Amplifier in 0.18 μm SiGe BiCMOS

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Abstract: This paper presents a 20 GS/s four-channel time-interleaved sample-and-hold amplifier (SHA), which aims to improve the harmonic distortion performance, eliminate the common-mode voltage fall in track-to-hold transition, and solve the difficulty of timing mismatch calibration among different sampling channels. In data path, the harmonic distortion of the track-hold switch is optimized by introducing a distortion-improving resistor into the switched emitter follower. The common-mode voltage fall is eliminated by an inserted delay-regulating resistor. Additionally, broadband data buffers are utilized to further guarantee a wide bandwidth. In clock path, an interpolator-based phase regulator in analog domain is implemented to calibrate the timing mismatch, hence avoiding the large area cost and complicated algorithm in the digital domain. Fabricated in a 0.18 μm SiGe BiCMOS process, the experimental results show that the SHA achieves a bandwidth of 16 GHz and a total harmonic distortion of -39.6 to approximately -51.8 dB with a -3 dBm input. By applying the proposed sampling phase regulator, the timing mismatch can be optimized to satisfy the requirement of 6-bit resolution at a 4×5 GS/s sampling rate. The proposed SHA shows prominent performance on both bandwidth and linearity, which makes it suitable for ultra-high-speed communication networks.

Keywords: low distortion; sample-and-hold amplifier; time-interleaved sampling; track-hold switch

1. Introduction

Analog to digital converter (ADC) is an essential bridge to connect the analog domain with the digital domain. Due to the rapid growth of wireless and wireline communications, high-speed broadband ADC with low distortion is required. For example, 10~30 GS/s ADCs with 6~8-bit resolution are demanded in the PAM-4 wireline receiver [1–3]. The sample-and-hold amplifier (SHA) at the front end of an ADC is a key block, because it can not only alleviate the bandwidth requirement for the following blocks, but also eliminate the influence of clock jitter and signal skew in the following ADCs [4]. In particular, the master–slave structured SHA, where the output is held constant over the whole clock cycle, supplies sufficient operating time for ADCs [5]. It is difficult for a standalone SHA to achieve tens of GS/s sampling rate with high precision. With several identical SHAs sampling successively under control of multiphase clocks, the time-interleaved structure is an effective method to solve this problem. In theory, sampling rate can be consistently multiplied along with the increasing channel number. However, the offset mismatch, gain mismatch, and timing mismatch between

interleaved channels limit the infinite improvement of the sampling rate, where the timing mismatch is the most difficult one to be calibrated [6–9].

A variety of multi-GS/s SHAs have been reported, but several aspects still need to be improved. First, most of the current sampling switches are based on switched emitter follower (SEF), which is simple in structure and easy to be realized. However, they suffer from high distortions [10–12]. Usually, a small-scale sampling capacitor is implemented to suppress harmonic distortion. However, a decreasing sampling capacitor deteriorates the performance of signal feedthrough, hold-mode voltage drop, and signal-to-noise rate (SNR). In other words, the properties of SHA restrict each other and it is difficult to make appropriate trade-offs by only regulating the sampling capacitance. Second, common-mode voltage fall is induced during the track-to-hold transition as a result of the mismatch between turn-on and turn-off speed of the sampling switches [13–15]. Although this common-mode fall can be eliminated by differential output, it influences the performance of following blocks, especially when the common mode rejection ratio is not very appropriate. Third, timing mismatch in many interleaved SHAs is calibrated in digital domain using complicated algorithms, which may cause a significant overhead in terms of area occupation and power consumption [7,16,17].

In this paper, a four-channel time-interleaved 20 GS/s master–slave SHA fabricated in a 0.18 μm SiGe BiCMOS process is presented. The contributions of this paper are mainly focused on the following aspects: First, a distortion-improving resistor is introduced into the SEF-based track-hold switch, which can reduce the distortion by enhancing emitter negative feedback, without deteriorating the signal feedthrough and hold-mode voltage drop performance. In other words, decoupling among these mutually restrictive properties is realized, and design difficulty is reduced. Second, a delay-regulating transistor is added in the path of hold clock. By adjusting the size of transistor, the common-mode voltage fall in track-to-hold transition can be eliminated. Third, an interpolator-based phase regulator is implemented to remove the timing mismatch among the four interleaved channels. As a result, large area consumption and complex mismatch calibration algorithm in digital domain are avoided. Finally, fabricating process is another important consideration besides circuit structure. Compared with traditional designs, the adopted SiGe BiCMOS process is less costly than the InP process [5,18] and provides higher cut-off frequency and better matching property than the CMOS process [12,19]. The measurement results show that the proposed SHA can achieve a 16 GHz bandwidth and a -39.6 to approximately -51.8 dB THD, with a -3 dBm input.

The remainder of this paper is organized as follows. Section 2 shows the system architecture of the proposed SHA. The distortion-improved broadband track-hold switch, the interpolator-based phase regulator, and the data buffers are elaborated in Section 3. The measurement results are presented in Section 4, and the conclusions are drawn in Section 5.

2. SHA Architecture

Figure 1 presents the block diagram of the proposed SHA, which consists of a data path and a clock path. In the data path, the input signal is sampled successively by the four identical sampling channels. Each channel is composed of two sampling stages (master stage and slave stage) and three data buffers (input buffer, middle buffer, and output buffer). The two sampling stages are driven by a pair of clocks with 180-degree phase shift (i.e., CKAM for master stage and CKAS for slave stage in channel A), thus operating in track mode and hold mode alternately. When the master stage is tracking the input signal, the slave stage is in hold mode, to keep the output constant. When the master stage turns to hold mode, the slave stage quickly tracks the held voltage in master stage. As a result, the output can be kept stable during almost the whole clock cycle, hence providing a sufficient operating time for the following data conversion. The data buffers are utilized to provide isolating and driving capability.

Figure 1. Block diagram of the proposed sample-and-hold amplifier.

In traditional designs, small-scale sampling capacitance is usually utilized in the track-hold switch, to achieve low distortions at the cost of deteriorating the feedthrough performance and hold-mode voltage drop [10]. It is rather difficult to make appropriate trade-offs among these properties at the same time. Besides, due to the nonlinearity of clock switches, common-mode voltage fall is induced at the transition from track mode to hold mode. In order to solve the two problems, a distortion-improving resistor and a delay-regulating transistor are implemented in the track-hold switches, which will be described in Section 3.

The temporal relation of the four interleaved channels are controlled by four-phase sampling clocks generated in the clock path. Compared with offset mismatch and gain mismatch, timing mismatch among sampling clocks is more critical for bit resolution, as it directly affects the sampling accuracy and is more costly and more difficult to be calibrated. It is necessary to take timing mismatch calibration into consideration in architecture design instead of putting all stresses on digital calibration, for the sake of saving area and reducing algorithm complexity. An interpolator-based phase regulator is utilized to realize this consideration, where the dividing clock signals (I/IN , Q/QN) are the input and the driving clocks for each channel are the output whose phase difference can be regulated by the control voltage (i.e., dly_a controls the phase relation among $CKAM \sim CKDM$ or $CKAS \sim CKDS$).

3. Circuit Design

3.1. Broadband Distortion-Improved Track-Hold Switch

Figure 2 demonstrates the transistor-level schematic of the track-hold switch, which alternatively operates in track mode and hold mode. In track mode, high-level *Track* signal switches on transistor Q_2 and low-level *Hold* signal turns off Q_1 , thus steering tail current I_{SEF} to Q_3 . The switch acts as an emitter follower, and the input is captured quickly and accurately by the sampling capacitor C_H . In hold mode, Q_2 is switched off by the low-level signal *Track* and Q_1 is turned on by high-level *Hold*. I_{SEF} is steered to resistor R_1 , inducing a significant voltage drop on the base of Q_3 . As a result, Q_3 is switched off, and the voltage is held by C_H .

Figure 2. Half transistor-level schematic of the track-hold switch.

Harmonic distortion is one of the most important parameters to characterize the performance of the track-hold switch. The distortion of the track-hold switch is mainly induced by the nonlinear base-emitter voltage modulation of Q_3 , as its collector current, I_c , has exponential relationship to base-emitter voltage V_{be} , which is expressed as follows:

$$I_c = I_S \cdot e^{V_{be}/V_T}. \quad (1)$$

Compared with traditional design, an extra resistor R_t is in series after the Q_3 emitter and before the sampling capacitor C_H . Applying the Volterra analysis and negative feedback theory, the second and third harmonic distortions, $HD2$ and $HD3$, can be respectively expressed as the following equations (see Appendix A for detailed derivations):

$$\begin{aligned} |HD2| &= \frac{A \cdot V_T}{4} \cdot \frac{1}{I_{SEF}^2} \cdot \left(\frac{1}{|1/SC_H|} \right)^2, \\ |HD3| &= \frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_{SEF}^3} \cdot \left(\frac{1}{|1/SC_H|} \right)^3, \end{aligned} \quad \text{(in traditional design)} \quad (2)$$

$$\begin{aligned} |HD2| &= \frac{A \cdot V_T}{4} \cdot \frac{1}{I_{SEF}^2} \cdot \left(\frac{1}{|R_t + 1/SC_H|} \right)^2, \\ |HD3| &= \frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_{SEF}^3} \cdot \left(\frac{1}{|R_t + 1/SC_H|} \right)^3. \end{aligned} \quad \text{(in proposed SHA)} \quad (3)$$

These expressions indicate that the second and third harmonic distortions, $HD2$ and $HD3$, are the functions of signal amplitude, A , thermal voltage, V_T , tail current, I_{SEF} , distortion-optimizing resistor, R_t , and sampling capacitance, C_H . It is obvious that, compared with traditional design, the addition of R_t improves the performance of harmonic distortions $HD2$ and $HD3$. This improvement can be attributed to the enhanced Q_3 emitter negative feedback. Figure 3a future gives the simulated relationship between $HD3$ and R_t at different frequency, which verifies the effectiveness of R_t . It can be seen that larger R_t induces better harmonic performance. Figure 3b demonstrates the relationship between the improvement on $HD3$ compared with traditional design ($R_t = 0$) at different frequencies. It can be seen that the $HD3$ improvement becomes more significant as the input frequency increases.

Figure 3. (a) Simulated $HD3$ varies along with R_t at different frequency; (b) simulated improvement on $HD3$ compared with traditional design ($R_t = 0$).

Ideally, the voltage should be kept constant on sampling capacitor during the hold period. However, the base leakage current I_{b6} of Q_6 discharges C_H and induces a voltage drop, which is called as hold-mode voltage drop. In addition, a portion of the input is coupled to the sampling capacitor through the Q_3 base-emitter parasitic capacitance C_{be3} , which is called as signal feedthrough. Meanwhile, the bandwidth is dominated by the sampling capacitor, C_H , and the equivalent resistance at the sampling capacitor. Table 1 summaries the comparison of these properties between the proposed switch and traditional one. In the table, the hold-mode voltage drop rate refers to voltage drop per unit time on sampling capacitor during hold mode. Decreasing C_H is the main method to achieve low distortion in traditional design, but signal feedthrough and hold-mode voltage drop aggravate the cost. It is rather difficult to optimize these properties at the same time by regulating C_H . In the proposed structure, the addition of R_t can suppress the harmonic distortion without aggravating the signal feedthrough and hold-mode voltage drop performance. As a result of the small emitter output resistance of Q_3 , it is simple to achieve broad bandwidth, even when R_t is implemented. Thus, although the addition of R_t decreases the bandwidth in some degree, dozens of GHz bandwidth is still available.

Table 1. Properties of the proposed SHA and traditional design.

	The Proposed SHA		The Traditional Design
$ HD2 $	$\frac{A \cdot V_T}{4} \cdot \frac{1}{I_{SEF}^2} \cdot \left(\frac{1}{ R_t + 1/SC_H } \right)^2$	$\leq$	$\frac{A \cdot V_T}{4} \cdot \frac{1}{I_{SEF}^2} \cdot \left(\frac{1}{ 1/SC_H } \right)^2$
$ HD3 $	$\frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_{SEF}^3} \cdot \left(\frac{1}{ R_t + 1/SC_H } \right)^3$	$\leq$	$\frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_{SEF}^3} \cdot \left(\frac{1}{ 1/SC_H } \right)^3$
Signal feedthrough	$\frac{C_{be3}}{ C_{be3} + C_H + S \cdot R_t C_H C_{be3} }$	$\leq$	$\frac{C_{be3}}{C_{be3} + C_H}$
Hold-Mode voltage drop rate	$\frac{I_{b6}}{C_H}$	$=$	$\frac{I_{b6}}{C_H}$
Bandwidth	$\frac{1}{2\pi(R_t + R_{out3})C_H}$	$<$	$\frac{1}{2\pi R_{out3}C_H}$

Benefitting from the master–slave sampling structure, the master stage and the slave stage can be optimized separately. The master stage is required to be broadband and low-distortion, as it is utilized to capture the input signal precisely. The slave stage needs to possess the properties of high isolation and low feedthrough, as its input is held by the master stage. Consequently, small-scale resistor $R = 39 \text{ ohms}$ and capacitance $C_H = 78 \text{ fF}$ are chosen in the master stage, achieving simulated

38 GHz bandwidth and -85 dB HD3 @5 GHz. In the slave stage, larger-size 50 ohms R and 135 fF C_H are adopted to achieve a simulated 20 GHz bandwidth, 2.1 mV/ns voltage drop rate, -72 dB HD3, and -60 dB feedthrough @5 GHz.

The transition from track mode to hold mode is another factor influencing dynamic performance [13–15]. Due to the nonlinear exponential relationship between collector current and base-emitter voltage of bipolar transistor, during the transition from track mode to hold mode, the speed of turning on Q_1 is faster than switching off Q_2 . The base voltage fall of Q_3 induced by tail current drawn from R_1 is transmitted to C_H through the incompletely closed Q_3 . As a result, the common-mode voltage on C_H is pulled down during hold cycle, as shown in Figure 4. Although the voltage drop can be eliminated by differential topology, it will shift the DC operating point, deteriorating the performance of the following transistors. Particularly, dynamic performance can be severely affected when the common-mode rejection ratio is not high enough. In order to address this issue, an extra transistor Q_4 is utilized. The collector current I_{C1} of Q_1 discharges the parasitic capacitors at node B before pulling down the base voltage of Q_3 through R_1 , thus the transmitting delay between *Hold* signal rising up and base voltage of Q_3 falling down is generated. During the inserted delay, Q_3 emitter voltage soaring is induced by the switching off of Q_2 , which compensates the common-mode voltage fall on the sampling capacitor. The compensation effectiveness is determined by the delay time, which is tuned by the size of Q_4 . The delay should be optimized carefully, because short delay will induce under-compensation of common-mode voltage fall, while long delay will result in over-compensation.

Figure 4. Common-mode voltage fall during the track-to-hold transition.

The small current, I_1 , is utilized to suppress the voltage fluctuation on node B ; otherwise, it needs to take more time for node B voltage (V_B) to decrease from high level to switch on Q_4 when turning to hold mode. Without I_1 , the decreasing time of V_B could be comparable to hold period at high sampling rate, resulting in overcompensation.

Figure 5 reveals that the common-mode voltage fall is significantly reduced by the added transistor Q_4 . The size of Q_4 is supposed to be $0.15 \mu\text{m} \times 16 \mu\text{m}$, because the corresponding voltage fall is about 0 mV. However, considering the area cost and the effect on the bandwidth of node A , the size of Q_4 is chosen to be $0.15 \mu\text{m} \times 5 \mu\text{m}$, which limits the voltage fall into an acceptable value of 3 mV from the original 24 mV, and guarantees a 40 GHz bandwidth on node A .

Figure 5. Simulated common-mode voltage fall with different size of Q4 (with 0.15 μm emitter width).

3.2. Interpolator-Based Phase Regulator

The sampling timing is under control of four-phase differential clocks generated by the phase regulator, as shown in Figure 1. For a 6-bit resolution with an input frequency of 10 GHz, the standard deviation of the timing mismatch is required to be less than 0.2 ps, which corresponds to 0.36 degree [20–22]. An interpolator-based phase regulator is employed in the clock path to calibrate the timing mismatch in the analog domain, thus large area cost and complicated algorithm in digital calibration are avoided. Taking I/IN as an example, Figure 6a shows the schematic of the phase adjusting and Figure 6b demonstrates the circuit implementation of interpolator. An input pair of the interpolator (ap/an) is the buffered I/IN , another input pair (bp/bn) is the delayed ap/an through a CML buffer. The output CKAM is utilized to drive the track-hold switch in master stage directly, and in slave stage after a CML buffer, matching the delay between the track-hold switches of the two stages. The two pairs of inputs are interpolated by the control voltage dly_ap/an , generated by dly_a through an S2D converter. The output of the interpolator $y(t)$ can be expressed as the function of input ap/an and bp/bn :

$$y(t) = \frac{\alpha \cdot A \cdot \sin(\omega t) + \beta \cdot B \cdot \sin(\omega t + \theta)}{\sqrt{(\alpha A)^2 + 2\alpha\beta AB \cdot \cos\theta + (\beta B)^2}} \cdot \sin\left[\omega t + \arctan \frac{\beta B \cdot \sin\theta}{\alpha A + \beta B \cdot \cos\theta}\right] \quad (4)$$

where $A \cdot \sin(\omega t)$ indicates the input ap/an , $B \cdot \sin(\omega t + \theta)$ is another input bp/bn , θ denotes the phase difference between ap/an and bp/bn generated by the CML buffer, and α and β are the corresponding interpolation weights controlled by dly_ap/an . It can be seen that output amplitude of the interpolator is modulated by the interpolating weights α and β , indicating gain variations of the interpolator when tuning the delay. In order to mitigate the effect of gain variation, in our practical circuit, a two-stage rectifier is employed to convert the output amplitude to full swing before it is applied to the track-hold switches (see the Figure 6a). By this method, the amplitude of the clock signal can be kept constant during the timing mismatch calibration.

Figure 7a shows the simulated Monte Carlo timing mismatch of the sampling channels, and Figure 7b presents the adjusting range of the interpolator at different frequencies. The variation range of simulated phase difference and phase adjusting range of the interpolator for each frequency are annotated in Figure 7a,b, respectively. It can be seen that the phase mismatch can be covered by the adjusting the control voltage between 0 and 3.3 V. Taking 5 GHz as an example, the phase adjusting range of the interpolator is $0^\circ \sim 24.1^\circ$, and the variation range of phase difference at 5 GHz is $75.8^\circ \sim 99.5^\circ$, indicating that the timing mismatch can be mitigated.

Figure 6. (a) Block schematic of the phase adjusting; (b) circuit implementation of the interpolator.

Figure 7. (a) Distribution histogram of channel phase difference with different frequency; (b) phase-adjusting range of the interpolator with different frequency.

3.3. Data Buffers

Data buffers, including input buffer, middle buffer, and output buffer, play an important role in the SHA. They are employed to provide appropriate broadband voltage gain and isolate track-hold switches from other blocks. Figure 8 presents their circuit implementation, where emitter degeneration resistors are utilized to achieve low distortion and broad bandwidth. It is worth noting that a common-mode feedback topology is utilized in the middle buffer to protect the input common voltage

of slave track-hold switch from the voltage fall in master track-hold switch. The feedback path can be elaborated as follows:

$$V_{cm} \uparrow \rightarrow I_{f1}, I_{f2} \uparrow \rightarrow V_1 \uparrow \rightarrow I_{f3} \downarrow \rightarrow I_{f4} \uparrow \rightarrow V_{fb} \downarrow \rightarrow V_{cm} \downarrow$$

When V_{cm} increases because of the process-voltage-temperature (PVT) variation, I_{f2} is supposed to increase along with I_{f1} , but $I_{f1} + I_{f2}$ is kept as constant I_{s1} , so V_1 rises up to suppress I_{f2} . I_{f3} also decreases as the increasement of V_1 downgrades the gate-source voltage of Q_{fb} . V_{fb} is pulled down, because larger current $I_{f4} = I_{s0} - I_{f3}$ is drawn from resistor R_{fb} , which inhibits the increasement of V_{cm} as a result. The Miller capacitor C_1 is utilized to keep the feedback stable, and C_2 is implemented to maintain the pure voltage of V_{fb} .

Figure 8. Schematic of data buffer: (a) input buffer; (b) output buffer; and (c) middle buffer.

4. Measurement Results

The proposed four-channel time-interleaved SHA was fabricated in a 0.18 μm SiGe BiCMOS process, and it occupies an area of $1.26 \times 1.60 \text{ mm}^2$. Figure 9a presents the chip microphotograph, and the power breakdown is displayed in Figure 9b, where it consumes 2200 mW from a 4.5/3.3 V supply when operating at $4 \times 5 \text{ GS/s}$ sampling rate. The measurement setup is presented in Figure 10, where differential input signal and sampling clock are provided by the analog signal generators through broadband baluns. The output spectrum information is measured by a spectrum analyzer, and the real-time output waveform is observed by the Teledyne Lecroy MCM-Zi-A oscilloscope.

Figure 9. (a) Chip microphotograph; (b) power breakdown.

Figure 10. Measurement setup.

Figure 11a shows the time-domain measurement result of one channel, where a 600 MHz sinusoid input is sampled at 5 GS/s. It can be seen that the fabricated SHA has good hold-mode performance, with less than 0.4 mV feedthrough. Figure 11b presents the result of a 13.6 GHz input sampled at 5 GS/s, where the curves remain flat during the hold period, revealing good over-sampling performance of the SHA.

Figure 11. Time-domain measurement. The upper two waveforms are complementary single-ended outputs, and the bottom one is the differential output. (a) A 600 MHz input signal sampled by 5 GS/s; (b) a 13.6 GHz input signal sampled by 5 GS/s.

The four-channel output waves are presented in Figure 12. Because the oscilloscope is equipped with only two broadband channels, they are successively demonstrated along with the output of channel A. It can be seen that the channel-timing mismatch is limited to 0.118 ps, verifying the effectiveness of the proposed interpolator-based phase regulator.

Figure 12. Four-channel output waves with 500 MHz input sampled at 4×5 GS/s. (a) Output of channel A and channel B with 0.1ps phase error; (b) output of channel A and channel C, indicating 0.3 ps phase error between channels A and C; (c) output of channel A and channel D, indicating 0.2 ps phase error between channels A and D. As a result, the standard deviation of the timing mismatch is 0.118 ps, satisfying the requirement of 6-bit resolution.

The spectral measurement results are shown in Figure 13. Since the single-ended spectrum analyzer is used, only single-ended output spectrum is measured. Figures 14 and 15 give the *THD* and bandwidth curve of the proposed SHA, respectively. It can be seen that, due to the broadband distortion-improved track-hold switch topology, the SHA achieves good harmonic distortion performance of -39.6 to approximately -51.8 dB *THD*, with an input frequency swept up to 11 GHz, as well a broad 16 GHz bandwidth.

Table 2 compares the proposed SHA with several previous designs. The results demonstrate that this design achieves higher sampling rate and wider bandwidth than the designs in 65 nm CMOS and similar 0.18 μm SiGe process [23–26]. The *THD* performance is even comparable with those designs utilizing advanced InP processes [5,18].

Figure 13. Spectrum of the SHA (325 MHz -3 dBm signal sampled at 5 GS/s).

Figure 14. Measured THD (-3dBm input).

Figure 15. Measured bandwidth.

Table 2. Performance summary and comparison.

	This Work	[5]	[18]	[23]	[24]	[25]	[26]
Process	0.18 μm SiGe BiCMOS	InP/210G	InP DHBT /320G	65 μm CMOS	65 μm CMOS	0.18 μm SiGe BiCMOS	0.18 μm SiGe HBT
Fsample (GS/s)	20	1	4	8	12	16	18
Bandwidth (GHz)	16	15	16	8	3	8	7
THD	−43	−42	−50	−33	−40.6	−45	−32.3
(dB@GHz@Vpp)	@5.325@0.45	@0.6@1	@1@0.4	@1@0.14	@2.72@0.5	@4@0.5	@2@1
Vdd/Power (V/mW)	3.3, 4.5/2200	−7/5200	−/2100	1.32/178	1.8/197	2.5/132	3.5/128
Area (mm ²)	1.26 × 1.60	1.6 × 1.4	1.5 × 1.8	1.1	0.9 × 1	1.3 × 0.89	1.58 × 1.7

5. Conclusions

In this paper, a four-channel time-interleaved SHA was developed, with an area of $1.26 \times 1.60 \text{ mm}^2$ and a power consumption of 2200 mW. In order to solve the low-distortion design problem, a track-hold switch with a distortion-improving resistor and a delay-tuning transistor is proposed. The measurement results show that a 16 GHz bandwidth and a −39.6 to approximately −51.8 dB THD are achieved. In addition, an interpolator-based phase regulator is implemented in the clock path, which calibrates the timing mismatch to satisfy the requirement of 6-bit resolution at the $4 \times 5 \text{ GS/s}$ sampling rate. Performance comparison shows that the proposed SHA has advantages on the sampling rate, bandwidth, and distortion performance, revealing a good prospect for application in direct RF sampling receiver, digital oscilloscope, and ADC-DSP based PAM-4 wireline receiver. The future work will be focused on developing an integrated self-adaptive calibration algorithm for timing mismatch, gain mismatch, and offset mismatch. The performances of distortion, bandwidth, and sampling rate are expected to be improved by utilizing a more advanced process and new circuit topology. What's more, a high-speed time-interleaved ADC on the basis of the proposed SHA has been put on the agenda.

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Appendix A Harmonic Distortion Analysis of the Track-Hold Switch

It is generally known that the input/output relationship of a weakly nonlinear amplifier can be modeled by a Taylor series:

$$v_{out} = a_0 + a_1 \cdot v_{in} + a_2 \cdot v_{in}^2 + a_3 \cdot v_{in}^3 + \dots, \quad (\text{A1})$$

where the second and third harmonic distortions, $HD2$ and $HD3$, can be expressed as follows [10,27]:

$$|HD2| = \left| \frac{1}{2} \cdot \frac{a_2}{a_1} \cdot A \right|, \quad |HD3| = \left| \frac{1}{4} \cdot \frac{a_3}{a_1} \cdot A^2 \right|, \quad (\text{A2})$$

where A is the amplitude of the input. When the negative feedback in Figure A1 is applied to the signal path, $HD2$ and $HD3$ will vary with the open-loop gain $T = a_1 \cdot F$ [28] as follows:

$$|HD2_f| = \left| \frac{1}{2} \cdot \frac{a_2}{a_1} \cdot \frac{A}{(1+T)^2} \right|, \quad |HD3_f| = \left| \frac{1}{4} \cdot \left[\frac{a_3}{a_1} \cdot \frac{1}{1+T} - \left(\frac{a_2}{a_1} \right)^2 \frac{2T}{(1+T)^2} \right] \cdot \frac{A^2}{(1+T)^2} \right|. \quad (\text{A3})$$

Figure A1. Harmonic distortion in negative feedback.

Based on the abovementioned analysis, the exponential relationship between collector current I_C and base-emitter voltage V_{in} of the bipolar transistor in Figure A2a can be expressed as follows [11,28,29]:

$$I_C = I_S \cdot \exp\left(\frac{V_{in}}{V_T}\right) \rightarrow i_c = \frac{I_C}{V_T} \cdot v_{in} + \frac{1}{2} \cdot \frac{I_C}{V_T^2} \cdot v_{in}^2 + \frac{1}{6} \cdot \frac{I_C}{V_T^3} \cdot v_{in}^3 + \dots \quad (A4)$$

where i_c is the variation of the base collector current, and I_C is the corresponding DC operating current. The simplified small-signal model of the track-hold switch on the track mode is shown in Figure A2b, where a negative feedback impedance, Z_E , is introduced into the emitter. The corresponding second and third harmonic distortions can be expressed as follows:

$$|HD2_f| = \left| \frac{1}{4} \cdot \frac{A}{V_T} \cdot \frac{1}{(1+T)^2} \right| \approx \left| \frac{1}{4} \cdot \frac{A}{V_T} \cdot \frac{1}{T^2} \right|, \quad |HD3_f| = \left| \frac{1}{24} \cdot \frac{A^2}{V_T^2} \cdot \frac{1-2T}{(1+T)^4} \right| \approx \left| \frac{1}{12} \cdot \frac{A^2}{V_T^2} \cdot \frac{1}{T^3} \right| \quad (A5)$$

where $T = g_m \cdot Z_E = \frac{I_C}{V_T} \cdot Z_E$.

In traditional SEF-based track-hold switch, the feedback load is composed of the sampling capacitor, C_H (shown in Figure A2b). As a result, $Z_E = \frac{1}{sC_H}$ and the harmonic distortions can be expressed as follows:

$$\begin{aligned} |HD2_f| &\approx \frac{A \cdot V_T}{4} \cdot \frac{1}{I_C^2} \cdot \frac{1}{|1/SC_H|^2} = \frac{A \cdot V_T}{4} \cdot \left(\frac{2\pi f C_H}{I_C} \right)^2, \\ |HD3_f| &\approx \frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_C^3} \cdot \frac{1}{|1/SC_H|^3} = \frac{A^2 \cdot V_T}{12} \cdot \left(\frac{2\pi f C_H}{I_C} \right)^3. \end{aligned} \quad (A6)$$

The expressions are the same as those derived in [10,13], which confirm the correctness of the analysis above.

When it turns to our proposed track-hold switch, the feedback load consists of distortion-improving resistor R_t and sampling capacitor C_H . As a consequence, $Z_E = R_t + \frac{1}{sC_H}$ and the expressions of the improved harmonic distortions are obtained as follows:

$$|HD2_f| \approx \frac{A \cdot V_T}{4} \cdot \frac{1}{I_C^2} \cdot \frac{1}{|R_t + 1/SC_H|^2}, \quad |HD3_f| \approx \frac{A^2 \cdot V_T}{12} \cdot \frac{1}{I_C^3} \cdot \frac{1}{|R_t + 1/SC_H|^3}. \quad (A7)$$

Figure A2. The relationship between I_C and V_{in} : (a) without negative feedback; (b) with emitter negative feedback impedance R_E , which consists of sampling capacitor, C_H , in traditional design, R_t , and C_H in the proposed design.

References

1. LaCroix, M.A.; Wong, H.; Liu, Y.H.; Ho, H.; Lebedev, S.; Krotnev, P.; Nicolescu, D.A.; Petrov, D.; Carvalho, C.; Alie, S.; et al. A 60Gb/s PAM-4 ADC-DSP-Based Transceiver in 7nm CMOS with SNR-Based Adaptive Power Scaling Achieving 6.9pJ/b at 32dB Loss. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 17–21 February 2019. [\[CrossRef\]](#)
2. Tabasy, E.Z.; Shafik, A.; Lee, K.; Hoyos, S.; Palermo, S. A 6 bit 10 GS/s TI-SAR ADC with Low-Overhead Embedded FFE/DFE Equalization for Wireline Receiver Applications. *IEEE J. Solid-State Circuits* **2014**, *49*, 2560–2574. [\[CrossRef\]](#)
3. Delong, C.; Heng, Z.; Nick, H.; Ali, N.; Burak, C.; Hyo, G.R.; Zhang, B.; Momtaz, A.; Cao, J. A 320mW 32Gb/s 8b ADC-based PAM-4 analog front-end with programmable gain control and analog peaking in 28nm CMOS. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 31 January–4 February 2016. [\[CrossRef\]](#)
4. Jiang, T.; Patrick, Y.C. 14.4-GS/s, 5-bit, 50mW time-interleaved ADC with distributed track-and-hold and sampling instant synchronization for ADC-based SerDes. In Proceedings of the 2015 IEEE International Wireless Symposium, Shenzhen, China, 30 March–1 April 2015. [\[CrossRef\]](#)
5. Bouvier, Y.; Konczykowska, A.; Ouslimani, A.; Godin, J. A 1 GSample/s, 15 GHz input bandwidth master-slave track-&-hold amplifier in InP-DHBT technology. In Proceedings of the 2009 IEEE MTT-S International Microwave Symposium Digest, Boston, MA, USA, 7–12 June 2009. [\[CrossRef\]](#)
6. Cai, S.C.; Tabasy, E.Z.; Shafik, A.; Kiran, S.; Hoyos, S.; Palermo, S. A 25GS/s 6b TI Two-Stage Multi-Bit Search ADC With Soft-Decision Selection Algorithm in 65 nm CMOS. *IEEE J. Solid-State Circuits* **2017**, *52*, 2168–2179. [\[CrossRef\]](#)
7. Razavi, B. Design Considerations for Interleaved ADCs. *IEEE J. Solid-State Circuits* **2013**, *48*, 1806–1817. [\[CrossRef\]](#)
8. Nam, J.W.; Hassanpourghadi, M.; Zhang, A.; Chen, M.S.W. A 12-Bit 1.6, 3.2, and 6.4 GS/s 4-b/Cycle Time-Interleaved SAR ADC With Dual Reference Shifting and Interpolation. *IEEE J. Solid-State Circuits* **2018**, *53*, 1765–1779. [\[CrossRef\]](#)
9. Lukas, K.; Danny, K.; Christian, M.; Matthias, B.; Pier, A.F.; Thomas, M. A 24-to-72GS/s 8b time-interleaved SAR ADC with 2.0-to-3.3pJ/conversion and >30dB SNDR at nyquist in 14nm CMOS FinFET. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 11–15 February 2018. [\[CrossRef\]](#)
10. Kristian, N.M.; Timothy, D.G.; Saeid, D.; Thomas, C.O.; James, C.L.; James, F.B. A High-Linearity, 30 GS/s Track-and-Hold Amplifier and Time Interleaved Sample-and-Hold in an InP-on-CMOS Process. *IEEE J. Solid-State Circuits* **2015**, *50*, 2692–2702. [\[CrossRef\]](#)
11. Konstantinos, V. Front-End Building Blocks for 100+ GS/s ADCs. Master's Thesis, University Toronto, Toronto, ON, Canada, 2016.
12. Heather, O.; Gopinath, A. A 20 GS/s 1.2 V 0.13 μ m CMOS switched cascode track-and-hold amplifier. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2010**, *47*, 512–516. [\[CrossRef\]](#)
13. Lee, J.; Leven, A.; Weiner, J.S.; Baeyens, Y.; Yang, Y.; Sung, W.J.; Frackoviak, J.; Kopf, R.F.; Chen, Y.-K. A 6-b 12-GSample/s track-and-hold amplifier in InP DHBT technology. *IEEE J. Solid-State Circuits* **2003**, *38*, 1533–1539. [\[CrossRef\]](#)
14. Gathman, T.; Madsen, K.; Li, J.; Oh, T.; Buckwalter, J. A 30 GS/s double-switching track-and-hold amplifier with 19 dBm IIP3 in an InP BiCMOS technology. In Proceedings of the 2014 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 11–15 February 2014. [\[CrossRef\]](#)
15. Arnaud, M.; Patricia, D.; Hervé, P.; Bruno, L.; Remi, C. Single-ended/differential 2.5-GS/s double switching Track-and-hold amplifier with 26GHz bandwidth in SiGe BiCMOS technology. In Proceedings of the 2016 IEEE MTT-S International Microwave Symposium, San Francisco, CA, USA, 22–27 May 2016. [\[CrossRef\]](#)
16. Sunghyuk, L.; Anantha, P.C.; Hae-Seung, L. A 1 GS/s 10b 18.9 mW Time-Interleaved SAR ADC with Background Timing Skew Calibration. *IEEE J. Solid-State Circuits* **2014**, *49*, 2486–2856. [\[CrossRef\]](#)
17. Law, C.H.; Hurst, P.J.; Lewis, S.H. A four-channel time-interleaved ADC with digital calibration of inter-channel timing and memory errors. *IEEE J. Solid-State Circuits* **2010**, *45*, 2091–2103. [\[CrossRef\]](#)

18. Deza, J.; Ouslimani, A.; Konczykowska, K.A.; Godin, J. A 4 GSa/s, 16-GHz input bandwidth master-slave track-and-hold amplifier in InP DHBT technology. In Proceedings of the 2012 IEEE Telecommunications Forum, Belgrade, Serbia, 20–22 November 2012. [\[CrossRef\]](#)
19. Gregor, T.; David, F.; Mohammad, M.K.; Corrado, C.; Frank, E. A 55-GHz-Bandwidth Track-and-Hold Amplifier in 28-nm Low-Power CMOS. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2016**, *63*, 229–233. [\[CrossRef\]](#)
20. Ma, S.; Wang, J.; Yu, H.; Ren, J. A 32.5-GS/s two-channel time-interleaved CMOS sampler with switched-source follower based track-and-hold amplifier. In Proceedings of the 2014 IEEE MTT-S International Microwave Symposium, Tampa, FL, USA, 1–6 June 2014. [\[CrossRef\]](#)
21. El-Chammas, M.; Murmann, B. General analysis on the impact of phase-skew in time-interleaved ADCs. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2009**, *56*, 902–910. [\[CrossRef\]](#)
22. Jamal, S.M.; Fu, D.; Singh, M.P.; Hurst, P.J.; Lewis, S.H. Calibration of sample-time error in a two-channel time-interleaved analog-to-digital converter. *IEEE Trans. Circuits Syst. I Reg. Papers* **2004**, *51*, 130–139. [\[CrossRef\]](#)
23. Mattos, D.; Hellmuth, P.; Recoquillon, C.; Gauffre, S.; Cais, P.; Pedroza, J.L.; Baudry, A. An 8Gsps, 65nm CMOS Wideband Track-and-Hold. In Proceedings of the 2011 IEEE International New Circuits and Systems Conference, Bordeaux, France, 26–29 June 2011. [\[CrossRef\]](#)
24. Liu, Y.C.; Chang, H.Y.; Chen, K. A 12Gb/s 3-GHz input bandwidth track-and-hold amplifier in 65 nm CMOS with 48-dB spur-free dynamic range. In Proceedings of the IEEE International Microwave Symposium, Tampa, FL, USA, 1–6 June 2014. [\[CrossRef\]](#)
25. Lin, Y.A.; Yeh, Y.C.; Liu, Y.C.; Chang, H.Y. A 55-dB SFDR 16-GS/s Track-and-Hold Amplifier in 0.18 μ m SiGe Using Differential Feedthrough Cancellation Technique. In Proceedings of the IEEE International Microwave Symposium, San Francisco, CA, USA, 22–27 May 2016. [\[CrossRef\]](#)
26. Li, X.T.; Kuo, W.M.L.; Lu, Y.; Krithivasan, R.; Cressler, J.D.; Joseph, A.J. A 5-bit, 18GS/sec SiGe HBT Track-and-Hold Amplifier. In Proceedings of the 2005 IEEE Compound Semiconductor Integrated Circuit Symposium, Palm Springs, CA, USA, 30 October–2 November 2005. [\[CrossRef\]](#)
27. Madsen, K. BiCMOS Sampling Circuits for High-Speed Data Converters. Master's Thesis, University California, San Diego, CA, USA, 2013.
28. SanSen, W.M.C. *Analog Design Essentials*; Springer: Dordrecht, The Netherlands, 2006; pp. 519–565.
29. Daneshgar, S.; Griffith, Z.; Seo, M.; Rodwell, M. Low distortion 50 G samples/s track-hold and sample-hold amplifiers. *IEEE J. Solid-State Circuits* **2014**, *49*, 2114–2126. [\[CrossRef\]](#)

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