

Article

An Isolated High Voltage Boost Current-Fed DC–DC Converter Based on 1:1 Transformer Multiplier Cells and ZVS Operation

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Abstract: This paper presents a high step up, current fed, interleaved, isolated DC–DC converter with voltage multipliers and ZVS (zero voltage switching). The converter provides zero voltage switching for all active switches and provides a high step up voltage gain that is suitable for very low voltage source applications, such as PV and other renewable sources. In addition, this converter allows the utilization of very low voltage stress switches and diodes. It reduces the current stress by interleaving the input current, and reduces the voltage stress by utilizing a half bridge based multiplier cell integrated configuration at the output voltage while providing high frequency galvanic isolation. The isolation is achieved through the use of 1:1 transformers which are easier to design, and the need for a high turns ratio is absent in this converter. The main theory of operation and the design guideline are presented, as is a laboratory prototype, all to validate the concept.

Keywords: DC–DC converter; transformer; ZVS

1. Introduction

Emerging renewable energy sources, such as solar PV and fuel cells, produce a very low DC voltage. Integrating them into the grid requires a converter with high voltage gain capability such as the system in Figure 1. The conventional boost converter cannot meet the required voltage gain unless there is a series connection for several input sources, and it also requires a galvanic isolation stage since it is not isolated.

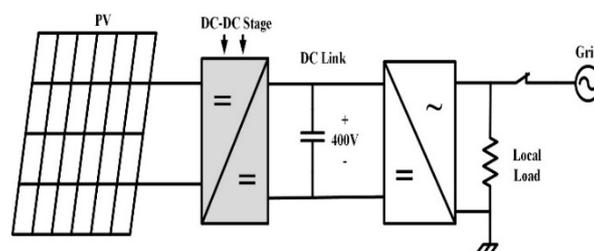


Figure 1. A converter's role in renewable energy systems.

In addition, these sources require a smooth input current to make maximal power tracking possible. To address these issues, several techniques have been proposed [1–3]. Some non-isolated topologies were proposed in [4–10] to provide a high voltage gain and reduce the voltage stress on switches and diodes. In [4], the high conversion ratio was achieved through a multi-winding coupled

inductor that feeds two multiplier cells. The main switch in this converter is hard switched and the input current consists of high ripple. Papers [5–7] present converters with high voltages and low input current ripple, utilizing SEPIC based converters and integrating multiplier cells coupled to the second inductor. The main switch, however, is still hard switched and the required duty cycle for 380 V applications is still higher than 0.5. Converters from [8–10] produce high voltage gain and reduced stress on switches but still introduce high input current ripple. Converters from [11–13] have solved these issues by being high voltage gain with ZVS and low input ripple. These would be good candidates for an application where galvanic isolation is not required. In the case where galvanic isolation is required, high frequency isolated DC–DC converters become the viable choice. Current fed, isolated DC–DC converters are the favorite in this category due to their boosting capability and their low ripple input current; additionally, they utilize high-frequency transformers with a relatively simple structure [14–16]. In these topologies, the duty cycle is usually more than 0.5. In [14–16], boosting was achieved through a transformer with a turn’s ratio, and ZVS operation of the main switches was realized but the transformer’s turns ratio needed to be high for sufficient voltage gain. In addition, the high turn’s ratio will reflect on the voltage stress of the secondary side switches and diodes.

The authors of this paper propose an innovative, high voltage gain DC–DC converter using multiplier cells and 1:1 ratio transformers as seen in Figure 2. The benefits of the 1:1 ratio main transformer can be summarized as follows:

1. It allows the interleaved input legs to have a series-output or half-bridge configuration.
2. It cuts the required duty cycle in half, since the voltage is the sum of the two cells.
3. The 1:1 ratio minimizes the voltage stress on diodes 1 and 4.

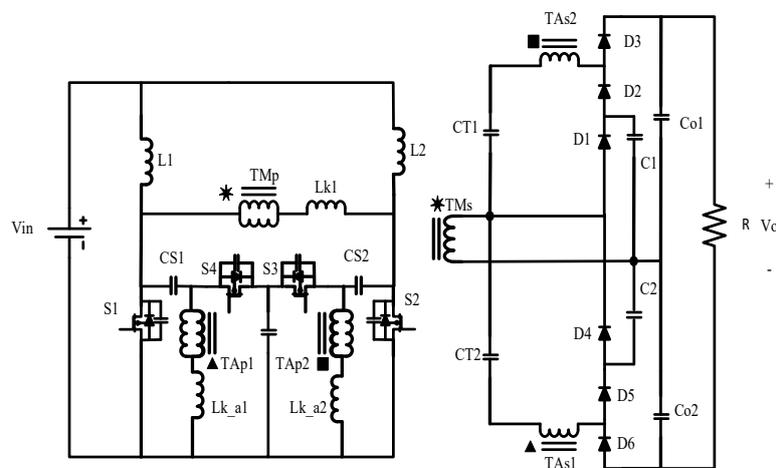


Figure 2. Proposed DC–DC converter topology.

The auxiliary 1:1 transformer’s purpose is to construct a multiplier cell that charges capacitors CT and Co in a soft manner. The charging current will be limited by the leakage inductance of the transformer. The 1:1 ratio will help minimize the voltage stress on diodes d2, d3, d5, and d6. By adopting this configuration, a very high voltage can be produced by using very low rated components. In addition, since the two cells will share the duty cycle burden, both switching and conduction losses will be reduced with the reduction of the duty cycle. The next section details the theory of operation for the proposed converter. After that, the design equations and how this converter compares to other works in terms of voltage gain and switch voltage stress are presented. Experimental results from a 450 laboratory prototype are then presented, and an efficiency study is presented. Finally, a conclusion and considerations for future work are put forward.

2. Theory of Operation

The switching states of the converter and Kirchhoff's voltage and current law (KVL and KCL) equations describing each switching state are described next.

A. First state; (t_0-t_1) S1 -> on S3 -> on S2 -> off S4 -> off:

In this case, Diodes 1, 3, and 5 are on, and Diodes 2, 4, and 6 are off. C1 is being charged by the main transformer, and Co1 is being charged by the main transformer, CT1, and the auxiliary transformer. On the other hand Capacitor CT2 is being charged by the main transformer, the auxiliary transformer, and C2. Capacitor Co2 is discharging the load as seen in Figure 3.

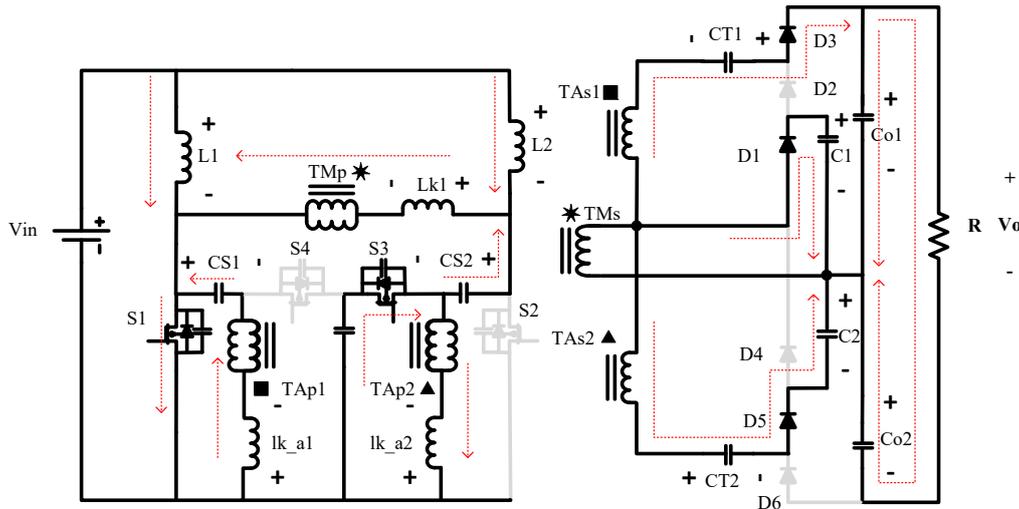


Figure 3. First switching state.

KVL equations during this state are:

$$V_{L1} = V_{in} \tag{1}$$

$$V_{Lk1} = V_{Cs2} + V_{Clamp} - \frac{1}{n}(V_{C1}) \tag{2}$$

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{3}$$

$$V_{Lka-1} = V_{Cs1} - \frac{1}{na}(V_{Co1} - V_{CT1} - V_{C1}) \tag{4}$$

$$V_{Lka-2} = V_{clamp} - \frac{1}{na}(V_{CT2} - V_{C2} - V_{C1}) \tag{5}$$

where na is the turn's ratio for the auxiliary transformers; and the KCL equations during this state are:

$$I_{Cs1} = -I_{Lka-1} \tag{6}$$

$$I_{Cs2} = I_{L2} - I_{Lk1} \tag{7}$$

$$I_{C1} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1} + I_{Lka-2}) \tag{8}$$

$$I_{CT1} = -\frac{1}{na}(I_{Lka-1}) \tag{9}$$

$$I_{CT2} = \frac{1}{na}(I_{Lka-2}) \tag{10}$$

$$I_{Co1} = -\frac{1}{na}(I_{Lka-1}) - I_o \tag{11}$$

$$I_{Co2} = -I_o \tag{12}$$

CS1 is now being discharged into the auxiliary transformer multiplier cell, and the clamp capacitor and CS2 are completing their charging process from the previous state. After the capacitors are charged and in the same switching state, the clamp capacitor starts feeding the auxiliary transformer and CS2 starts discharging into the main transformer.

B. Second state; (t1–t2) S1 -> off S3 -> on S2 -> off S4 -> on:

In this case, S1 turns off and the main transformer current starts circulating through S3 and S4. The current of Auxiliary Transformer 1 descends to zero and diode D3 turns off. Capacitors CS1 and clamp capacitor are charged and the capacitor CS2 continues to discharge in a decreasing manner. In other words, the capacitor continues discharging but at a slower rate as seen in Figure 4.

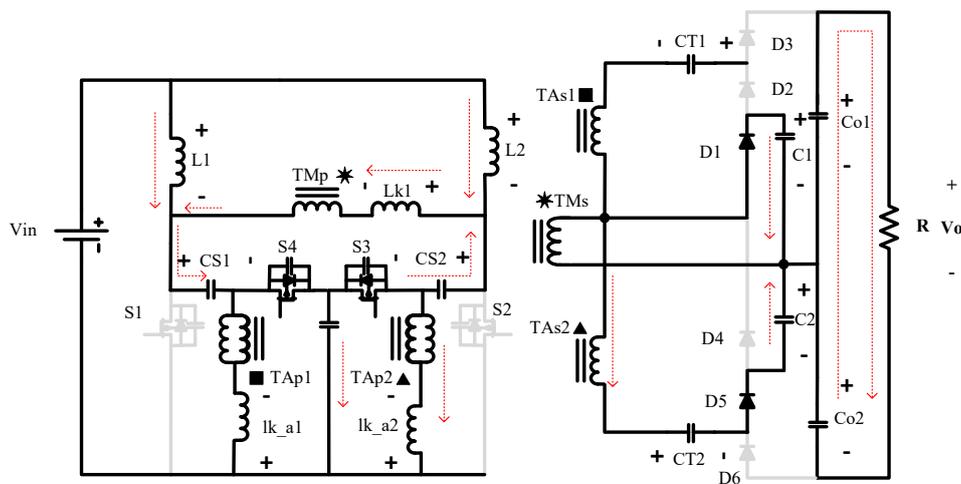


Figure 4. Second switching state.

The capacitor CT2 continues to be charged by C2, the main transformer, and the auxiliary transformer 2. KVL equations during this switching state are:

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{13}$$

$$V_{Lk1} = -\frac{1}{n}(V_{C1}) \tag{14}$$

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{15}$$

$$V_{Lka-1} = 0 \tag{16}$$

$$V_{Lka-2} = V_{clamp} - \frac{1}{na}(V_{CT2} - V_{C2} - V_{C1}) \tag{17}$$

And the KCL during this switching state is:

$$I_{Cs1} = I_{L1} + I_{Lk1} \tag{18}$$

$$I_{Cs2} = I_{L2} - I_{Lk1} \tag{19}$$

$$I_{C1} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1}) \tag{20}$$

$$I_{CT1} = 0 \tag{21}$$

$$I_{CT2} = \frac{1}{na}(I_{Lka-2}) \tag{22}$$

$$I_{Co1} = I_{Co2} = -I_o \tag{23}$$

C. Third switching state; (t2–t3) S1 -> off S3 -> off S2 -> on S4 -> on:

When S3 turns off, the output of the capacitor of S3 starts charging and the capacitor of S2 starts discharging. When the capacitor of S2 is fully discharged, its body diode starts conducting providing a ZVS condition for switch S2 to be turned on at the end of this switching period.

D. Fourth Switching state; (t3–t4) S1 -> off S3 -> off S2 -> on S4 -> on:

In this case (Figure 5), Switch two is turned on. Diodes 2, 4, and 6 are on, and Diodes 1, 3, and 5 are off. C2 is being charged by the main transformer and Co2 is being charged by the main transformer, CT2, and the auxiliary transformer. On the other hand Capacitor CT1 is being charged by the main transformer, the auxiliary transformer, and C1. Capacitor Co1 is discharging on the load.

KVL equations during this state are:

$$V_{L2} = V_{in} \tag{24}$$

$$V_{Lk1} = V_{Cs1} + V_{Clamp} - \frac{1}{n}(V_{C2}) \tag{25}$$

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{26}$$

$$V_{Lka-2} = V_{Cs2} - \frac{1}{na}(V_{Co2} - V_{CT2} - V_{C2}) \tag{27}$$

$$V_{Lka-1} = V_{clamp} - \frac{1}{na}(V_{CT1} - V_{C1} - V_{C2}) \tag{28}$$

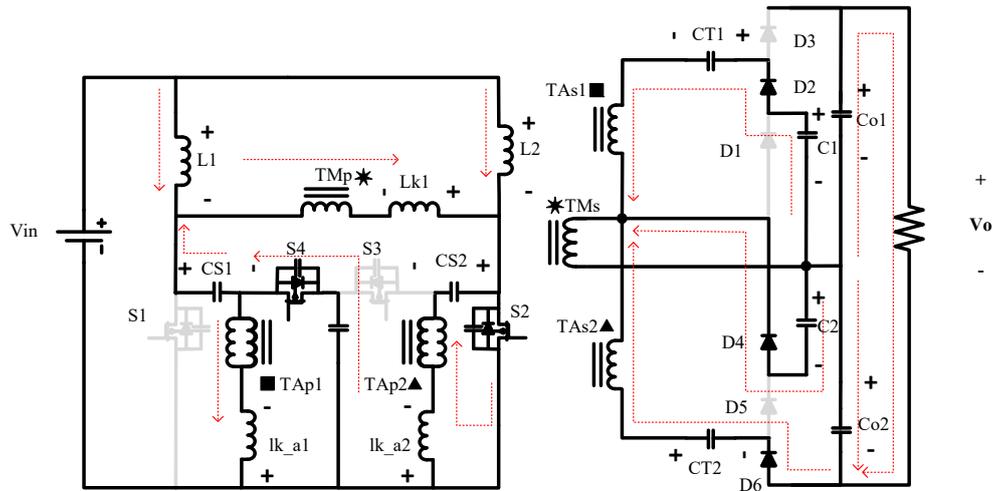


Figure 5. Fourth switching state.

And KCL equations during this state are:

$$I_{Cs2} = -I_{Lka-2} \tag{29}$$

$$I_{Cs1} = I_{L1} - I_{Lk1} \tag{30}$$

$$I_{C2} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-1} + I_{Lka-2}) \tag{31}$$

$$I_{CT2} = -\frac{1}{na}(I_{Lka-2}) \tag{32}$$

$$I_{CT1} = \frac{1}{na}(I_{Lka-1}) \tag{33}$$

$$I_{Co2} = -\frac{1}{na}(I_{Lka-2}) - I_o \tag{34}$$

$$I_{Co1} = -I_o \tag{35}$$

CS2 is now being discharged into the auxiliary transformer multiplier cell, and the clamp capacitor and CS1 are completing their charging process from the previous state. After the capacitors are charged and in the same switching state, the clamp capacitor starts feeding the auxiliary transformer and CS1 starts discharging into the main transformer.

E. Fifth Switching state; (t4–t5) S1 -> off S3 -> on S2 -> off S4 -> on:

In this case (Figure 6), S2 turns off and the main transformer current starts circulating through S3 and S4. The current of the Auxiliary Transformer 2 descends to zero and diode D6 turns off. Capacitors CS2 and the clamp capacitor are charged, and the capacitor CS1 continues to discharge in decreasing order. Capacitor CT1 continues to be charged by C1, the main transformer, and Auxiliary Transformer 1. 1. KVL equations during this switching state are:

$$V_{L2} = V_{in} - V_{Cs2} - V_{clamp} \tag{36}$$

$$V_{lk1} = -\frac{1}{n}(V_{C2}) \tag{37}$$

$$V_{L1} = V_{in} - V_{Cs1} - V_{clamp} \tag{38}$$

$$V_{lka-2} = 0 \tag{39}$$

$$V_{lka-1} = V_{clamp} - \frac{1}{na}(V_{CT1} - V_{C1} - V_{C2}) \tag{40}$$

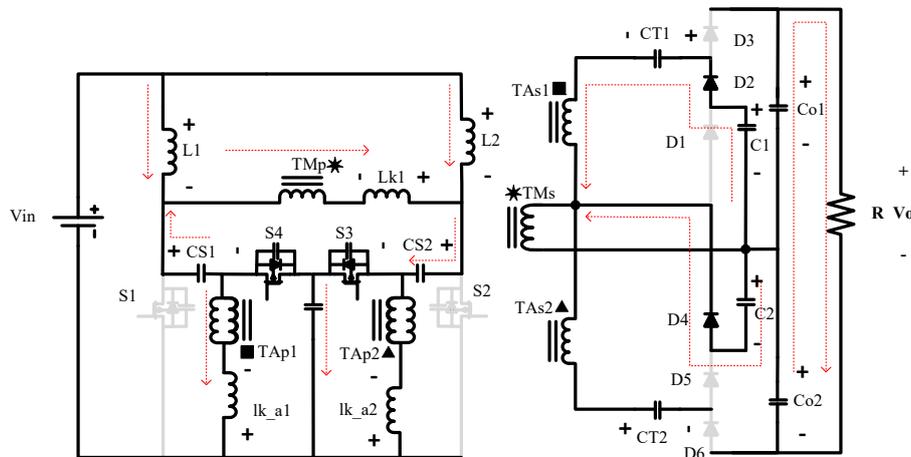


Figure 6. Fifth switching state.

And the KCL equations during this switching state is:

$$I_{Cs2} = I_{L2} + I_{Lk1} \tag{41}$$

$$I_{Cs1} = I_{L1} - I_{Lk1} \tag{42}$$

$$I_{C2} = \frac{1}{n}(I_{Lk1}) - \frac{1}{na}(I_{Lka-2}) \tag{43}$$

$$I_{CT2} = 0 \tag{44}$$

$$I_{CT1} = \frac{1}{na}(I_{Lka-1}) \tag{45}$$

$$I_{Co1} = I_{Co2} = -I_o \tag{46}$$

F. Sixth switching state; (t_5-t_6) S1 -> on S3 -> on S2 -> off S4 -> off

When S4 turns off, the output of the capacitor of S4 starts charging and the capacitor of S1 starts discharging. When the capacitor of S1 is fully discharged, its body diode starts conducting providing a ZVS condition for switch S1 to be turned on at the end of this switching period. The waveforms that describe the operation of this converter are presented in Figure 7:

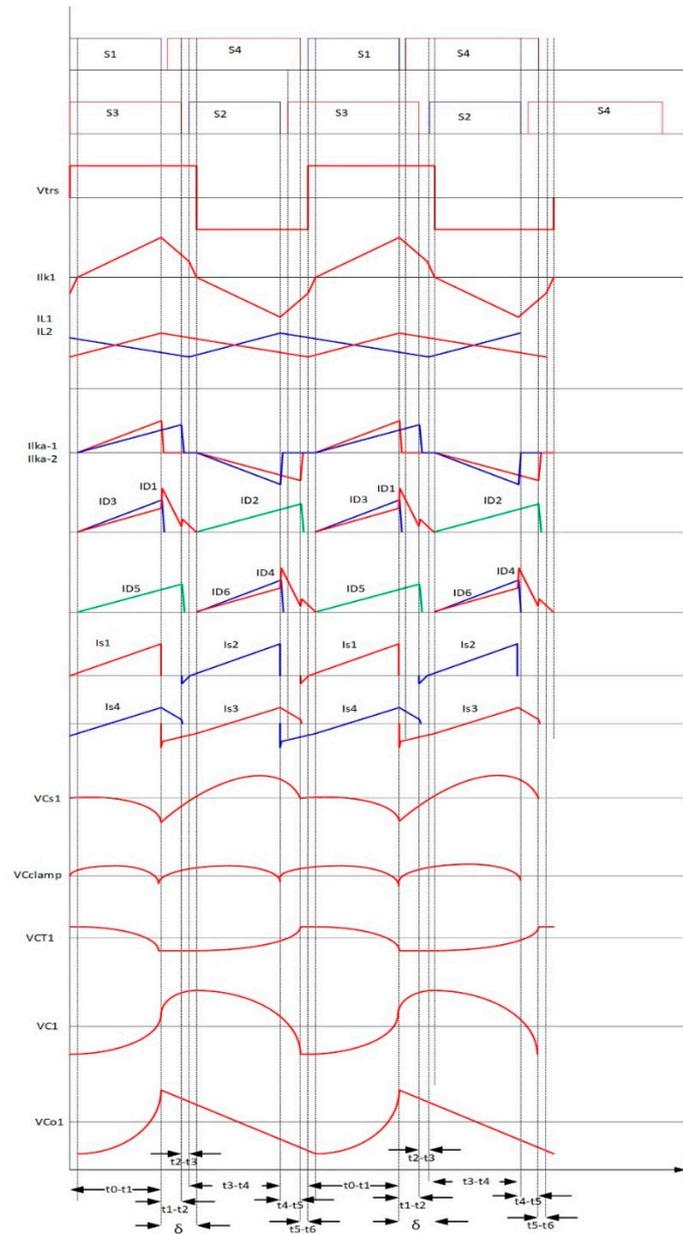


Figure 7. Waveforms of the converter over a complete cycle.

3. Voltage Gain and Design Equations

From the previous set of equations, the voltages of the capacitors and the currents of the inductors can be decided for the converter. In these following equations, the turns ratio of the main transformer and the auxiliary transformers is considered to be 1:1, and the leakage inductances l_{k-a1} and l_{k-a2} are considered to be very small, much smaller than the magnetizing inductances of their transformers, and

therefore their voltage drops are neglected for the purposes of designing equations for the capacitors and are considered equal to each other. From the V -sec balance on L1 and L2 we find:

$$V_{Cs1} = V_{Cs2} = V_{in} \quad (47)$$

$$V_{Clamp} = V_{in} \frac{D}{1-D} \quad (48)$$

Similarly, from the V -sec balance on Lk1 we find:

$$V_{C1} = 2V_{in} \frac{(D-2\delta)}{1-D} = V_{C2} \quad (49)$$

where δ is the period where the leakage current of the main transformer reaches zero. Since the voltage drop on the leakage of auxiliary transformers is negligible:

$$V_{CT1} = V_{CT2} = V_{C1} + V_{C2} + V_{Clamp} = \frac{V_{in}}{1-D} (4(D-2\delta) + D) \quad (50)$$

And the output capacitors voltage is equal to:

$$V_{Co1} = V_{Co2} = V_{CT1} + V_{C1} + V_{Cs} = \frac{V_{in}}{1-D} (6(D-2\delta) + 1) \quad (51)$$

And the output voltage of the Converter is calculated as:

$$V_o = V_{Co1} + V_{Co2} = \frac{V_{in}}{1-D} (12(D-2\delta) + 2) \quad (52)$$

From the conservation of energy principle:

$$\frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} = \frac{1}{1-D} (12(D-2\delta) + 2) \quad (53)$$

Since each input inductor shares half the current, the average current on each inductor is:

$$I_{L1} = I_{L2} = \frac{V_o}{R(1-D)} (6(D-2\delta) + 1) \quad (54)$$

And from the average current on D1:

$$\frac{1}{T} \left\{ \int_{\delta}^D I_{lk1} \cdot dt + \int_D^{0.5} I_{lk1} \cdot dt + \int_{0.5}^{0.5+\delta} I_{lk1} \cdot dt \right\} = 3 \frac{V_o}{R} \quad (55)$$

Solving this integration with respect to δ would lead to a long series of terms to be arranged and would finally lead to an equation defining δ as:

$$\delta^2 - \delta(D + 12Q) + \left(D \cdot \left(6Q - \frac{1}{4} \right) + \frac{D^2 + 2Q}{2} \right) = 0 \quad (56)$$

From which δ can be found and Q is defined as:

$$Q = \frac{6L_{k1} \cdot f_{sw}}{R} \quad (57)$$

After finding δ , the peak current of the leakage current can be found to be what follows:

$$I_{lk1_peak} = \frac{V_{in}}{1-D} (1 - 2(D - 2\delta)) \frac{D - \delta}{L_{k1} f_{sw}} \quad (58)$$

And the capacitor values based on the desired ripple percentage should be:

$$C_{T1,2} \geq \frac{1}{\frac{\Delta V_{CT}}{V_{CT}} \cdot R \cdot f_{sw}} \cdot \frac{12(D - 2\delta) + 2}{4(D - 2\delta) + D} \quad (59)$$

$$C_{o1,2} \geq \frac{2(1 - D + \delta)}{\frac{\Delta V_{Co}}{V_{Co}} \cdot R \cdot f_{sw}} \quad (60)$$

$$C_{1,2} \geq \frac{6(D - 2\delta) + 1}{\frac{\Delta V_C}{V_C} \cdot R \cdot f_{sw} \cdot (D - 2\delta)} \quad (61)$$

$$C_{s1,2} > \frac{24(D - 2\delta) + 4}{\frac{\Delta V_{Cs}}{V_{Cs}} \cdot R \cdot f_{sw} \cdot (1 - D)} \quad (62)$$

For the design of the transformer, the area product method was used. To select a core size for the transformer, the following equation was used:

$$Ap = Ae \cdot Aw = \frac{V_{in} \cdot (0.5 + \delta) \cdot I_{lk1_rms}}{B_{max} \cdot J \cdot K \cdot f_{sw}} \quad (63)$$

where B_{max} the maximum desired flux density in the core and J is the desired current density in the wires. From the Area product that is calculated here a proper core can be chosen if it has a higher area product that is calculated from the datasheet. After that, the number of turns can be calculated by:

$$N1 = N2 = \frac{V_{in} \cdot (0.5 + \delta)}{2B_{max} \cdot Ae \cdot f_{sw}} \quad (64)$$

The same approach was used for the auxiliary transformers where the area product for the core selection is:

$$AP_a = Ae \cdot Aw = \frac{V_{in} \cdot D \cdot I_{lka_rms}}{B_{max} \cdot J \cdot K \cdot f_{sw}} \quad (65)$$

And the number of turns can be found as:

$$Na1 = Na2 = \frac{V_{in} \cdot D}{2B_{max} \cdot Ae \cdot f_{sw}} \quad (66)$$

For the leakage inductor design, a gapped core with well-known effective permeability is chosen. Then the number of turns is calculated as:

$$n = \sqrt{\frac{L \cdot I_e}{\mu_e \cdot Ae}} \quad (67)$$

The next figure (Figure 8) shows the voltage gain compared to other referenced works and it shows that the voltage gain is much higher. It should also be noted that the considered voltage gain for the proposed converter is the practical voltage gain that takes into consideration the drop effect off the leakage inductance, while other converters' voltage gains are the ideal ones.

The normalized switch to voltage ratio for the proposed converter compared to others is in Figure 9.

It can be seen that the normalized switch voltage ratio is much smaller than compared topologies, which allow for the utilization of lower-rated switches.

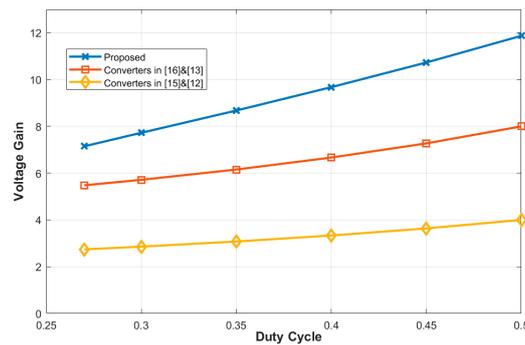


Figure 8. Gain comparison for the proposed converter against other converters.

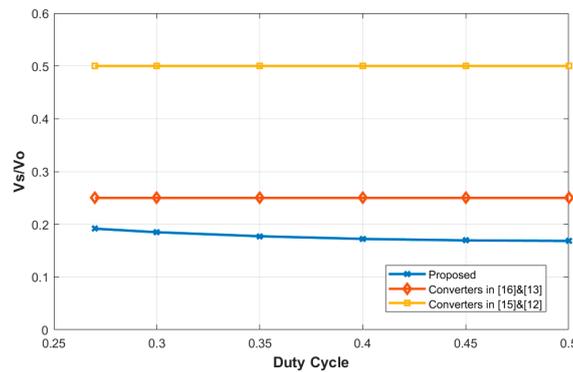


Figure 9. Switch voltage comparison for the proposed converter against others.

4. Experimental Results

A 450 W prototype was developed in the laboratory to validate the concept of this converter, and the parameters and components in Tables 1 and 2, respectively, were used.

Table 1. Experimental parameters.

Parameter	Value
V_{in}	37 V
V_{out}	380 V
Power	450 W
Frequency	25 KHz

Table 2. Description of components.

Component	Description
Input inductors	Coilcraft AGP4233-224ME. 220 μ H
Main Transformers	1:1 ratio TDK E55/28/21 N87 material
Auxiliary transformers	1:1 ratio TDK E42/21/15 N87 material
Leakage Inductor	22 μ H ETD core 29 \times 16 \times 10 N87 gapped 11 turns
Capacitors	2 \times 70 μ F Kemet C4AQLBW5700A3LK
MOSFETs	100 V 3.9 m Ohm Infineon IPP039N10N5
Diodes	Infineon Schottky IDH08SG60C

The first experiment was performed as a proof of concept to validate the analysis made in chapter two. Figure 10 shows the designed prototype and its layout. The current of the input inductors is measured through 2 LA 25NP sensors. The switches are being driven by FOD 3182 drivers with isolated floating supplies. In addition, each switch is equipped by an RC snubber to prevent over voltages from parasitic inductances at turn offs. The RC snubber consists of an 8.2 ohm resistor and

a 10 nF capacitor and its layout is shown in Figure 11. The converter is operated first at 320 W and output voltage of 380 volts. The input voltage is 37 volts and the duty cycle 0.4.

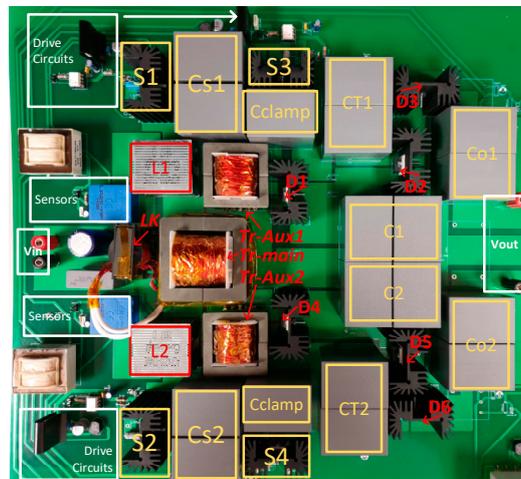


Figure 10. Implementation of the proposed converter.

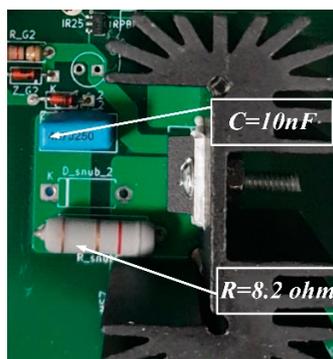


Figure 11. Snubber used in the prototype.

Figure 12a shows the current waveform of the main transformer I_{Lk1} which is probed by a current probe that conforms to the analysis presented in chapter two. Figure 12b shows the two input inductors share the current equally and will effectively reduce the ripple of the input source. With the addition of capacitors at the input, combined with the interleaved structure, the source can achieve zero ripple.

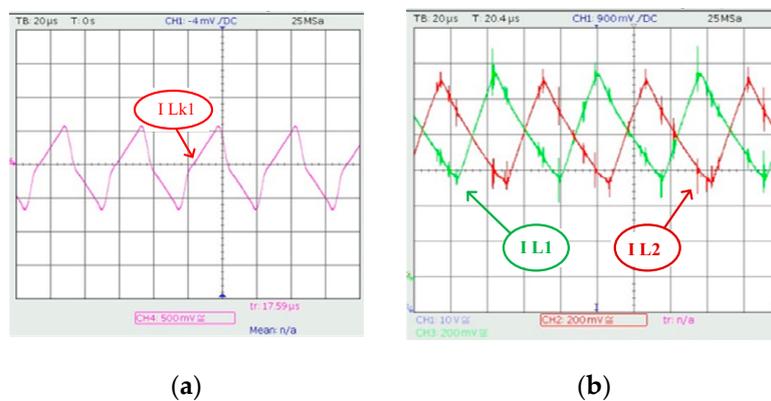


Figure 12. (a) Current waveform of the main transformer. (b) Current waveform of the input inductors.

Figure 13 shows the active switch voltage when the output voltage is 380 volts, the duty cycle is 0.4, and the load is 320 W. It can be seen that the voltage stress on the switch is 60 volts which is much less than the one in [12,15] which would be 120 volts for the same output voltage level.

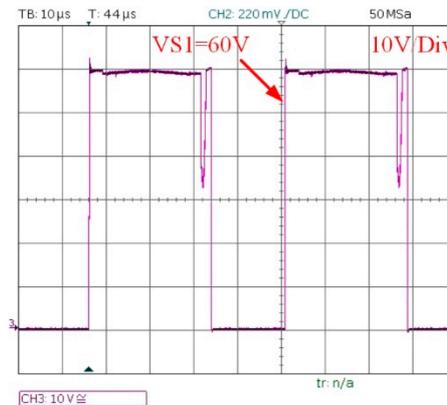


Figure 13. Stress on Switch 1. It is the same for all switches.

Figure 14 shows the switch currents under ZVS operation for the main and complementary switch under full load of 450 W. The other two switches have the same waveforms, only phase shifted 180 degrees.

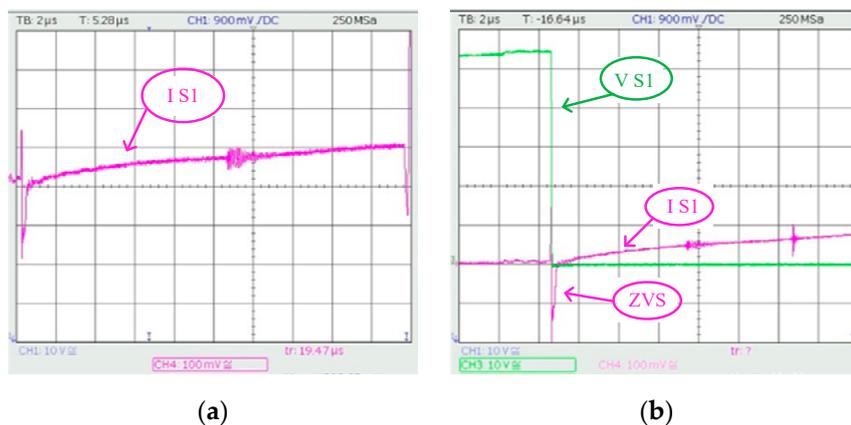


Figure 14. (a) Current waveform of Switch 1. (b) Current and voltage waveforms of Switch 1.

Figure 15 shows the voltages and currents of all diodes in a single leg. The other diodes have the exact waveforms, only phase shifted 180 degrees.

It can be seen that the waveforms conform to the analysis and it can be seen how Diode 1 collects all the leakages. These measurements were performed under a load of 450 Ohms and an output voltage of 380 volts.

The efficiency of the converter was found by measuring the input power and the output power at different loads. Figure 16 shows the overall efficiency of the converter during these loading conditions.

It can be seen that the converter maintains an efficiency of around 93% even at half load. The prototype from [14], for example, drops in efficiency from 93 to 90% at half load. In addition, prototype from [15] has a peak efficiency of 96% that drops to 89% at half load.

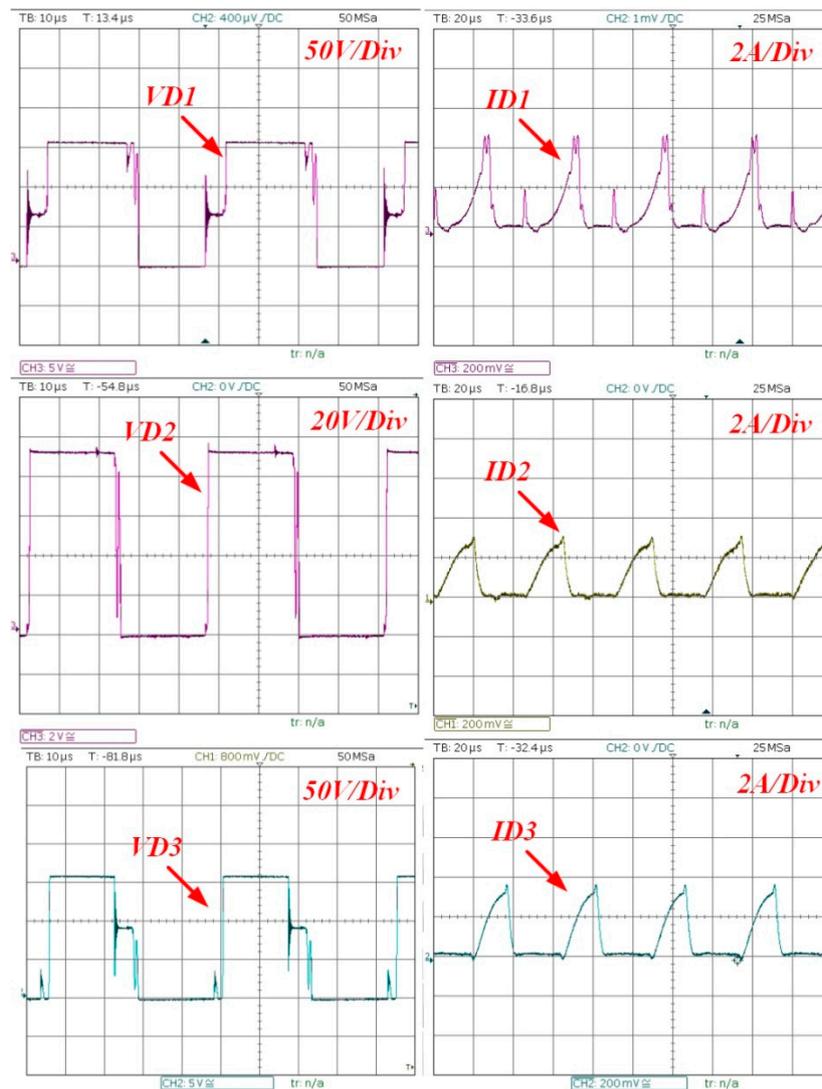


Figure 15. Currents of Diodes 1, 2, and 3.

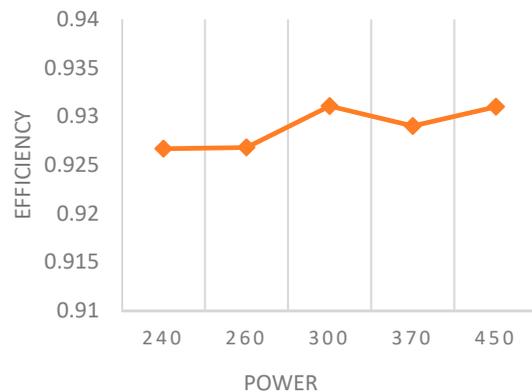


Figure 16. Efficiency of the converter at 37 V input and different loading points.

After that, a power loss distribution study was performed under a 320 W load and an output voltage of 380 volts. The losses for different parts of the converter were calculated based on measured currents and datasheet parameters. The following power loss calculations were performed:

$$P_D = I_{D-ave} * V_{DF} * D \tag{68}$$

$$P_{s1-s2} = I_{s1-s2-ave}^2 * R_{DSon} * D \quad (69)$$

$$P_{s3-s4} = I_{s3-s4-ave}^2 * R_{DSon} * (1 - D) \quad (70)$$

$$P_{L1-L2} = I_{L1-L2-RMS}^2 * R_{L1-L2} \quad (71)$$

$$P_{snubbers} = C.V^2 * f_{sw} * D \quad (72)$$

where VFD is the diode forward voltage that is given in the data sheet and RDS on is the on resistance of the switch found in the datasheet. RL1 and RL2 are the parasitic input inductor resistances. The power loss distribution is presented in Figure 17 and shows how losses are distributed in the converter. The transformers were built manually in the lab with a twisted pair of magnetic wires to reduce the skin effect and proximity effect. However, even though DC resistance can be measured, the effective resistance of the wires cannot be defined exactly under that switching frequency, and therefore the whole loss of the transformers was combined in the other section. The values of parasitic parameters were considered for the actual temperature and current during the calculation of losses.

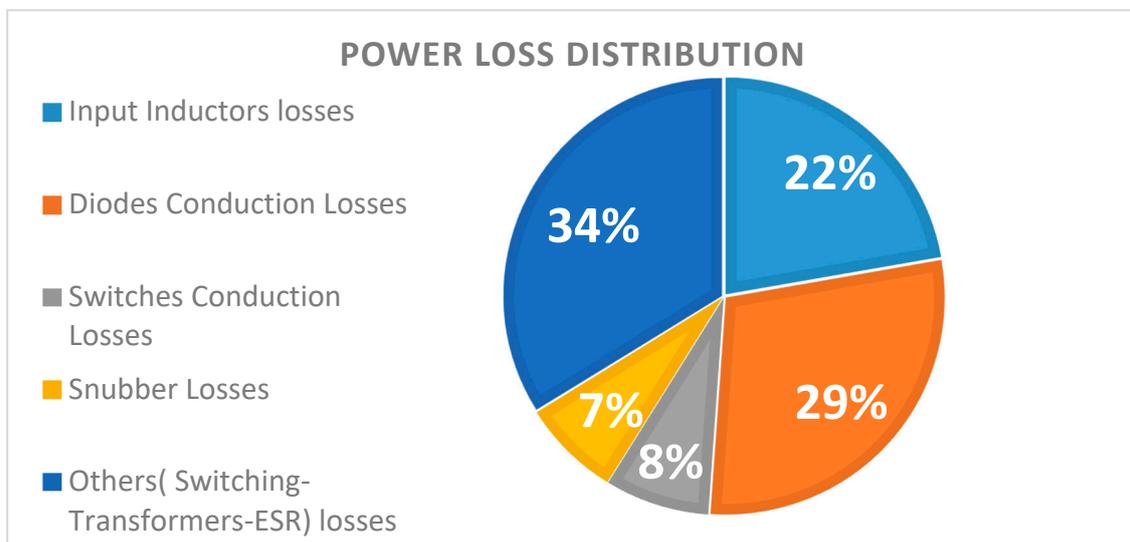


Figure 17. Loss distribution of the proposed converter.

5. Conclusions

The converter showed the ability to boost the voltage around 11 times at only 0.4 duty cycle and using a transformer with only 1:1 ratio. The proposed converter also allowed us to use very low rated switches and still produce high voltages. The efficiency of the converter has been measured under different loading conditions for a given input voltage of 37 volts DC. Figure 15 shows different loading conditions and their efficiencies for different conditions. The converter reached a maximum efficiency of 93.3% at 300 watts for a very high voltage boost ratio i.e., an outstanding improved performance when compared to traditional boost converters. The efficiency is well maintained even at light loading conditions, making possible to operate this converter topology for renewable energy low-voltage input of solar photovoltaics systems or fuel cells.

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