electronics

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Soft-Switching Bidirectional Three-Level DC–DC Converter with Simple Auxiliary Circuit

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Received: 16 August 2019; Accepted: 2 September 2019; Published: 3 September 2019

Abstract: This paper suggests a soft-switching bidirectional three-level DC–DC converter with a simple auxiliary circuit. The proposed converter uses auxiliary *LC* resonant circuits so that the power switches operate under a soft-switching condition. The resonant operation of the *LC* circuits makes power switches turn on at zero voltage, eliminating the turn-on switching power losses. The proposed converter improves the power efficiency, not using complex power switching circuits, but using simple *LC* resonant circuits. The operation of the proposed converter is described according to its operation modes. Experimental results for a 1.0 kW prototype are discussed to verify its performance. The proposed converter achieved the power efficiencies of 97.7% in the step-up mode and 97.8% in the step-down mode, respectively, for the rated load condition.

Keywords: bidirectional three-level DC–DC converter; switching power loss; zero-voltage switching; power efficiency

1. Introduction

The non-isolated bidirectional three-level DC–DC converter has been widely used for energy storage systems [1–3]. As shown in Figure 1, it uses four series-connected power switches and two series-connected capacitors [1]. Switch voltage stresses are reduced by half as power switches are stressed on half of the full DC-link voltage [2]. It can use lower voltage-rated power switches, which have better switching performance than the power switches in the two-level converters [3]. Aside from energy storage systems [4], the bidirectional three-level DC–DC converter has been utilized for ultra-capacitor applications [5] and various electric vehicle charging applications [6,7]. However, it still has switching power losses as it operates under a hard switching condition [8]. Particularly, in the case of using metal oxide semiconductor field effect transistors (MOSFETs), the turn-on switching losses are highly increased as the converter operates at high frequency and high output load condition [9].

In order to reduce switching power losses, the converter should operate under a soft switching condition [8]. The quasi-resonant switching technique can be adopted for reducing switching power losses [10–13]. By varying the switching frequency, power switches operate in a quasi-sinusoidal way [10]. The converter operates at the boundary of continuous and discontinuous conduction modes [11]. The turn-on switching losses can be reduced by turning on the switch at its minimum voltage [12]. However, the inevitable drawback of the quasi-resonant switching technique is that the variable frequency control complicates the design of the filter circuits and control loops [13].

An alternative method to reduce switching power losses is to adopt the active clamp switching technique [14–16]. Auxiliary power switches are used for making power switches to operate under a soft-switching condition [14]. Power switches can be turned on at zero voltage with a constant switching frequency [15]. However, the active clamp switching scheme increases the voltage stress of the power switch, increasing the voltage rating of the power switch, which is not desirable for three-level switching power converters [16]. Moreover, the actively clamped converters using the

auxiliary power switch require additional gate driving circuits, which cause additional gate driving power losses [17]. On the other hand, in [18] and [19], the three-level zero-voltage switching DC–DC converters have been suggested without using auxiliary power switch. Extra power diodes are required for power switches to be turned on at zero voltage. However, the converter in [18] operates only in the step-down mode, while the converter in [19] operates only in the step-up mode. Thus, the converters in [18] and [19] are not suitable for the bidirectional power conversion applications. More recently, the triangular current mode control method [20] has been applied to the bidirectional three-level DC–DC converter [21]. Although it does not require any auxiliary circuits, it suffers from conduction losses due to the extremely high circulating current, which limits its practical uses.

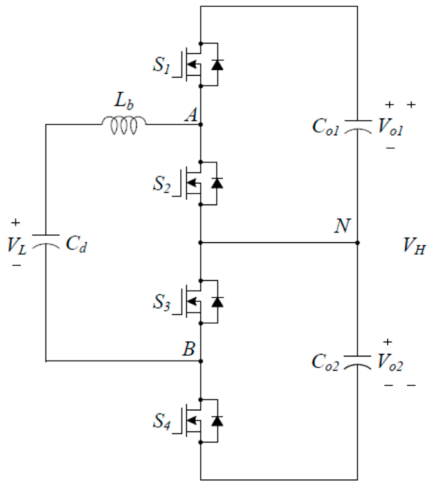


Figure 1. Circuit diagram of the conventional converter.

This paper aims to suggest a soft-switching bidirectional three-level DC–DC converter, which can effectively reduce the switching power losses with a simple auxiliary circuit. Figure 2 shows the circuit diagram of the proposed converter where two *LC* resonant circuits are included. They allow zero-voltage switching of power switches, eliminating the turn-on switching power losses. The proposed converter operates under a soft-switching condition with a constant switching frequency. It does not use any auxiliary active or passive power semiconductor devices, which simplifies the converter design. The proposed converter reduces switching power losses and improves power efficiency, compared to the previous converters, which operate without any auxiliary circuits, suffering from high switching losses. Experimental results for a 1.0 kW prototype are discussed to verify its performance. The proposed converter achieved the power efficiencies of 97.7% in the step-up mode and 97.8% in the step-down mode, respectively, for the rated load condition. The key contributions of this paper are to introduce the proposed idea, to present its theoretical analysis, to evaluate its performance experimentally, and to discuss its utilization for industrial applications.

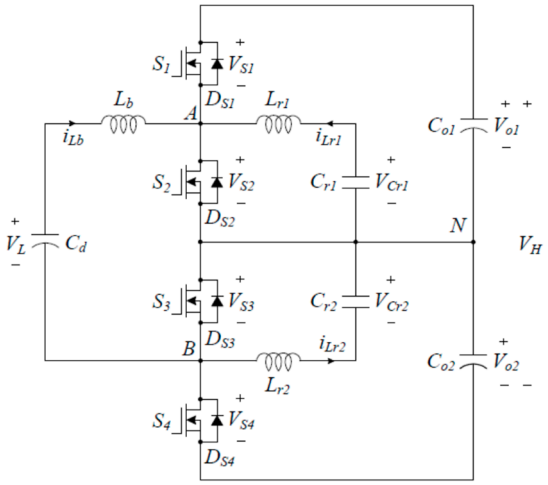


Figure 2. Circuit diagram of the proposed converter.

2. Proposed Converter

2.1. Circuit Configuration

Figure 2 shows the circuit diagram of the proposed converter. V_L is the low voltage. V_H is the high voltage. C_d, L_b, S_1, S_2, S_3, S_4, C_{o1}, and C_{o2} consist of the bidirectional three-level DC–DC converter. Power switches ($S_1 \sim S_4$) include the body diodes ($D_{S1} \sim D_{S4}$), respectively. Two identical LC circuits ($L_{r1} = L_{r2} = L_r$, $C_{r1} = C_{r2} = C_r$) are used for removing the turn-on switching losses of power switches. Power switches operate at a constant switching period T_s. The on-time of S_1 (S_2) is the same as the on-time of S_4 (S_3). The on-time of S_1 (S_2) is shifted by $T_s/2$ with respect to the on-time of S_4 (S_3). S_1 (S_3) and S_2 (S_4) operate complementary with a small dead time T_d. The inductor L_b is large enough so that the inductor current i_{Lb} is continuous. The capacitors C_d, C_{o1}, and C_{o2} are large enough so that the capacitor voltages V_L, V_{o1}, and V_{o2} are constant. It is assumed that $V_{o1} + V_{o2} = V_H$ and $V_{o1} = V_{o2} = V_H/2$. The resonant frequency f_r of the LC resonant circuit is assumed to be lower than the switching frequency f_s of the converter. The capacitor voltages V_{Cr1} and V_{Cr2} are supposed to be constant during T_s.

2.2. Control Operation

The proposed converter operates in a step-up mode when the electric power is transferred from V_L to V_H. As S_2 and S_3 are the main control switches, the duty cycle D is defined as the ratio between the on-time T_{on} of S_2 (S_3) and T_s. The proposed converter operates in a step-down mode when the electric power is transferred from V_H to V_L. S_1 and S_4 are the main control switches in the step-down mode. The duty cycle D is defined as the ratio between the on-time of S_1 (S_4) and T_s. Only the operation principles of the converter in the step-up mode are addressed here because the operation principles of the converter in both modes are analogous. Figure 3 shows the circuit diagrams of the proposed converter according to the switches' states in the step-up mode. The proposed converter has four operation stages:

Stage I: The converter is in *Stage I* only when $D > 0.5$. S_2 and S_3 are turned on. S_1 and S_4 are turned off. i_{Lb} flows through L_b, S_2, S_3, and C_d. The following equation is obtained as

$$-V_L + L_b \frac{di_{Lb}}{dt} = 0. \quad (1)$$

i_{Lr1} flows through L_{r1}, S_2, and C_{r1}. The resonance between L_{r1} and C_{r1} is expressed as

$$-V_{Cr1} + L_{r1} \frac{di_{Lr1}}{dt} = 0, \quad (2)$$

$$C_{r1}\frac{dV_{Cr1}}{dt} = i_{Lr1}. \tag{3}$$

i_{Lr2} flows through L_{r2}, C_{r2}, and S_3. The resonance between L_{r2} and C_{r2} is expressed as

$$-V_{Cr2} + L_{r2}\frac{di_{Lr2}}{dt} = 0, \tag{4}$$

$$C_{r2}\frac{dV_{Cr2}}{dt} = i_{Lr2}. \tag{5}$$

S_2 conducts i_{Lb} and i_{Lr1}, while S_3 conducts i_{Lb} and i_{Lr2}.

Stage II: The converter is in *Stage II* only when $D < 0.5$. S_2 and S_3 are turned off. S_1 and S_4 are turned on. i_{Lb} flows through L_b, S_1, C_{o1}, C_{o2}, S_4, and C_d. The following equation is obtained as

$$V_H + L_b\frac{di_{Lb}}{dt} - V_L = 0. \tag{6}$$

i_{Lr1} flows through L_{r1}, S_1, C_{o1}, and C_{r1}. The resonance between L_{r1} and C_{r1} is expressed as

$$-V_{Cr1} + L_{r1}\frac{di_{Lr1}}{dt} + V_{o1} = 0, \tag{7}$$

$$C_{r1}\frac{dV_{Cr1}}{dt} = i_{Lr1}. \tag{8}$$

i_{Lr2} flows through L_{r2}, C_{r2}, C_{o2}, and S_4. The resonance between L_{r2} and C_{r2} is expressed as

$$-V_{Cr2} + L_{r2}\frac{di_{Lr2}}{dt} + V_{o2} = 0, \tag{9}$$

$$C_{r2}\frac{dV_{Cr2}}{dt} = i_{Lr2}. \tag{10}$$

S_1 conducts i_{Lb} and i_{Lr1}, while S_4 conducts i_{Lb} and i_{Lr2}.

Stage III: S_2 and S_4 are turned on. S_1 and S_3 are turned off. i_{Lb} flows through L_b, S_2, C_{o2}, S_4, and C_d. The following equation is obtained as

$$V_{o2} + L_b\frac{di_{Lb}}{dt} - V_L = 0. \tag{11}$$

i_{Lr1} flows through L_{r1}, S_2, and C_{r1} in a similar way to *Stage I*. i_{Lr2} flows through L_{r2}, C_{r2}, C_{o2}, and S_4 in a similar way to *Stage II*. S_2 conducts i_{Lb} and i_{Lr1}, while S_4 conducts i_{Lb} and i_{Lr2}.

Stage IV: S_1 and S_3 are turned on. S_2 and S_4 are turned off. i_{Lb} flows through L_b, S_1, C_{o1}, S_3, and C_d. The following equation is obtained as

$$V_{o1} + L_b\frac{di_{Lb}}{dt} - V_L = 0. \tag{12}$$

i_{Lr1} flows through L_{r1}, S_1, C_{o1}, and C_{r1} in a similar way to *Stage II*. i_{Lr2} flows through L_{r2}, C_{r2}, and S_3 in a similar way to *Stage I*. S_1 conducts i_{Lb} and i_{Lr1}, while S_3 conducts i_{Lb} and i_{Lr2}.

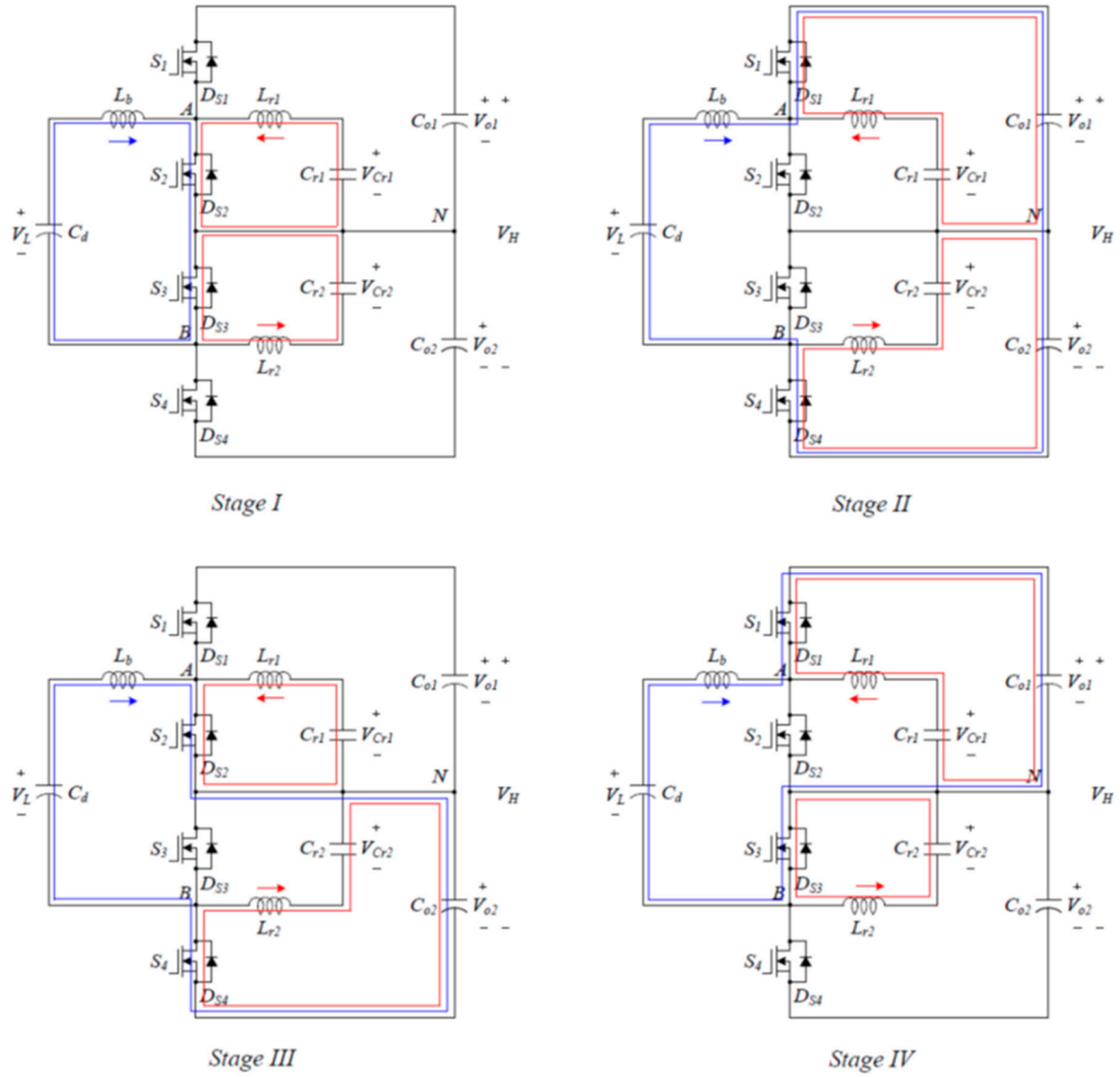
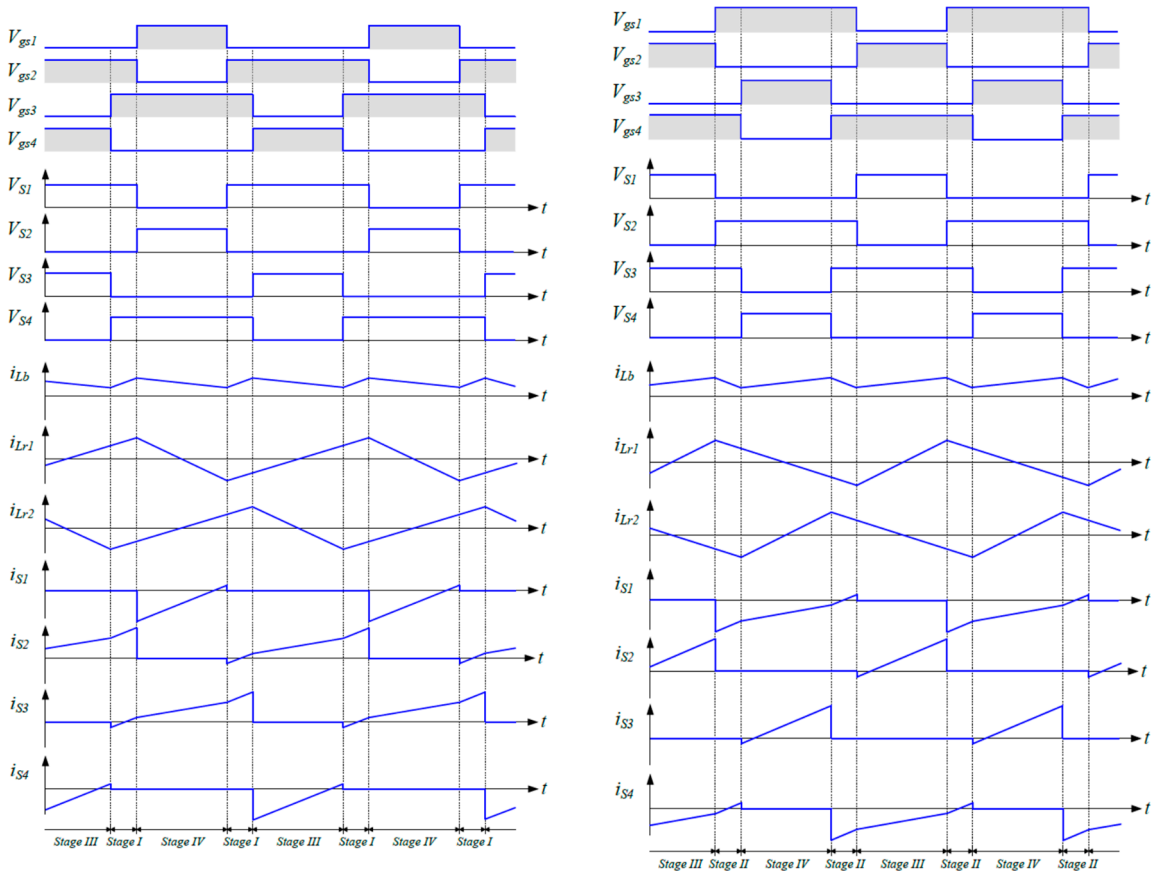


Figure 3. The circuit diagram of the proposed converter according to the switches' states in the step-up mode.

Figure 4 shows the operation waveforms of the converter in the step-up mode, for $D > 0.5$ and $D < 0.5$, respectively. V_{gs1}, V_{gs2}, V_{gs3}, and V_{gs4} are the gate signals for $S_1 \sim S_4$, respectively. i_{S1}, i_{S2}, i_{S3}, and i_{S4} are the switch currents for $S_1 \sim S_4$, respectively.



(**a**) (**b**)

Figure 4. The operation waveforms when the converter operates in the step-up mode: (**a**) $D > 0.5$; (**b**) $D < 0.5$.

2.3. Soft-Switching Condition

Figure 5 shows the equivalent circuit diagrams of the proposed converter for the turn-on switching transition for S_1. This switching transition period corresponds to the switching time from *Stage I* to *Stage IV* in the step-up mode. C_{S1} and C_{S2} are the parasitic output capacitances of S_1 and S_2, respectively. As shown in Figure 5a, C_{S1} has been charged to V_{o1} as i_{Lb} and i_{Lr1} flow through S_2. Figure 5b shows the circuit diagram for the switching transition moment when S_2 is turned off. i_{Lb} and i_{Lr1} are split up between the capacitances, charging C_{S2} and discharging C_{S1}. C_{S1} is completely discharged by i_{Lb} and i_{Lr1}, which flows in reverse through S_1. The switch voltage V_{S1} becomes zero before S_1 is turned on. S_1 can be turned on at zero voltage when a gating signal is applied to S_1, as shown in Figure 5c. C_{S2} has been charged to V_{o1} as i_{Lb} and i_{Lr1} flow through S_1. The switching transition for other power switches is analogous to the switching transition for S_1.

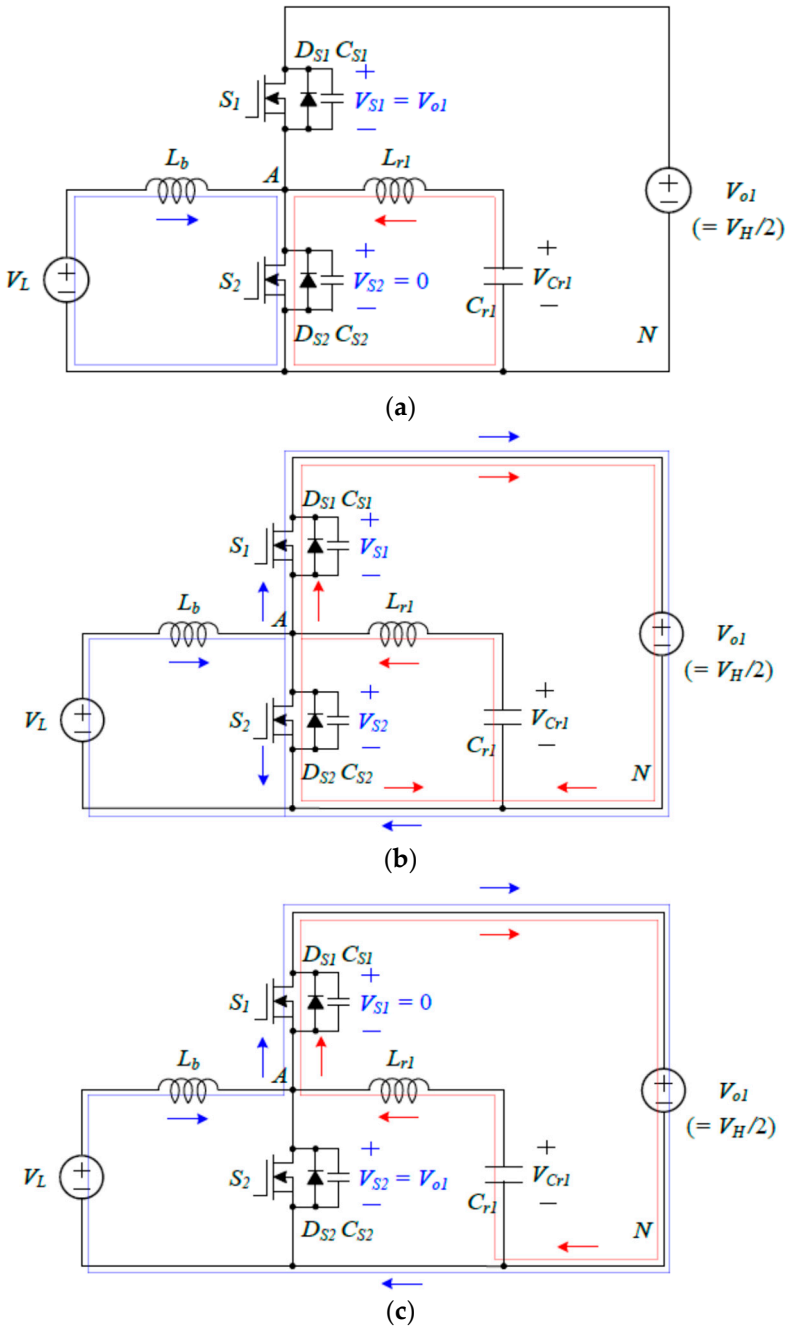


Figure 5. The equivalent circuit diagrams of the proposed converter for the turn-on switching transition for S_1: (**a**) *Stage I* in the step-up mode; (**b**) switching transition from *Stage I* to *Stage IV* in the step-up mode; (**c**) *Stage IV* in the step-up mode.

The switch current i_S becomes the sum of two inductor currents as $i_{Lb} + i_{Lr1}$ for S_1 and S_2 and $i_{Lb} + i_{Lr2}$ for S_3 and S_4, respectively. In order to achieve the zero-voltage switching, i_S should flow in reverse through the body diode of the switch at the switching transition moment. Then, i_S should be lower than the zero current at the switching transition moment. For the moment from *Stage I* to *Stage IV*, the zero-voltage switching condition for S_1 can be expressed as

$$\left|i_{Lb,avg}\right| + \frac{\Delta i_{Lb}}{2} + \frac{\Delta i_{Lr1}}{2} > 0 \tag{13}$$

where Δi_{Lb} and Δi_{Lr1} are

$$\Delta i_{Lb} = \frac{V_L}{L_b} DT_s, \tag{14}$$

$$\Delta i_{Lr1} = \frac{V_L}{L_{r1}} DT_s. \tag{15}$$

Δi_{Lb} is the current ripple of L_b, and Δi_{Lr1} is the current ripple of L_{r1}. $|i_{Lb,avg}|$ is the absolute value of the average inductor current $i_{Lb,avg}$. By the assumption that $L_{r1} = L_{r2} = L_r$, the following relation can be obtained from Equation (13) as

$$\frac{P_d}{V_L} + \frac{V_L T_{on}}{2L_b} + \frac{V_L T_{on}}{2L_r} > 0 \tag{16}$$

where P_d is the rated power of the proposed converter. For the moment from *Stage IV* to *Stage I*, the zero-voltage switching condition for S_2 can be expressed as

$$\left|i_{Lb,avg}\right| - \frac{\Delta i_{Lb}}{2} - \frac{\Delta i_{Lr}}{2} < 0 \tag{17}$$

which can be rewritten by Equations (14) and (15) as

$$\frac{P_d}{V_L} - \frac{V_L T_{on}}{2L_b} - \frac{V_L T_{on}}{2L_r} < 0. \tag{18}$$

Once L_r is determined by Equation (18), Equation (16) can be satisfied without any constraint. By simplifying Equation (18), the inductance of L_r can be chosen, which gives the design criterion of Lr as

$$L_r < \frac{L_b V_L^2 T_{on}}{2P_d L_b - V_L^2 T_{on}}. \tag{19}$$

On the other hand, the switch current should operate under the above-resonant continuous mode to ensure the zero-voltage switching operation. Therefore, the switching frequency f_s (= $1/T_s$) of the converter should be higher than the resonant frequency f_r of the *LC* resonant circuit [22]. After the selection of L_r, the capacitance of C_r can be determined by the following condition as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} < f_s. \tag{20}$$

3. Simulation and Experimental Results

3.1. Simulation Results

Simulation results were obtained for the conventional converter in Figure 1 and the proposed converter in Figure 2. The simulations have been carried out by the physical security information management (PSIM) electronic simulation software. For the key system parameters of V_L = 150 V, V_H = 370 V, P_d = 1000 W, T_s = 50 µsec, T_d = 2 µsec, L_b = 600 µH, and $C_{o1} = C_{o2}$ = 560 µF, Figure 6 shows the simulation results for the conventional converter. Figure 6a shows the simulation results for the step-up mode, and Figure 6b shows the simulation results for the step-down mode. As shown in Figure 6, a voltage spike is observed at the moment that each switch is turned off. This voltage spike causes the turn-on switching loss for the power switch, which eventually decreases the power efficiency. On the other hand, Figure 7 shows the simulation results of the proposed converter. The resonant parameters, such as L_r = 100 µH and C_r = 2 µF, were used. Figure 7a shows the simulation results for the step-up mode, and Figure 7b shows the simulation results for the step-down mode. Compared to the simulation results in Figure 6, no voltage spike is observed at the moment that each switch is turned off in the simulation results in Figure 7. With the help of the auxiliary circuit, the proposed converter eliminated the turn-on switching losses.

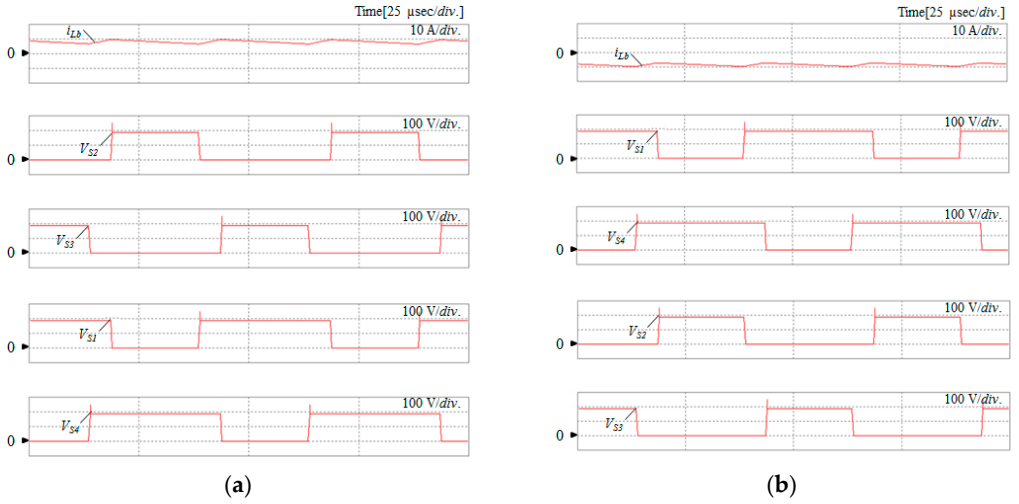


Figure 6. The simulation results of the conventional converter: (**a**) Step-up mode; (**b**) step-down mode.

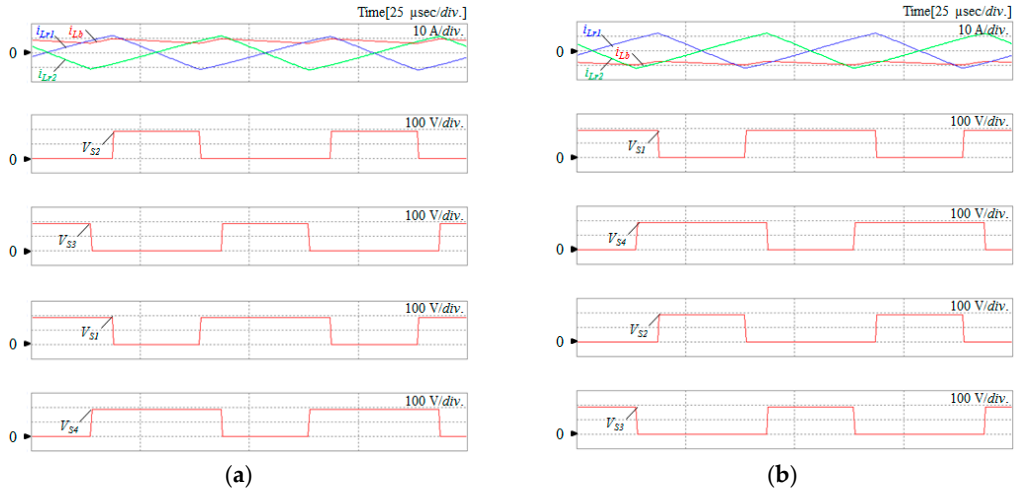


Figure 7. The simulation results of the proposed converter: (**a**) Step-up mode; (**b**) step-down mode.

3.2. Experimental Results

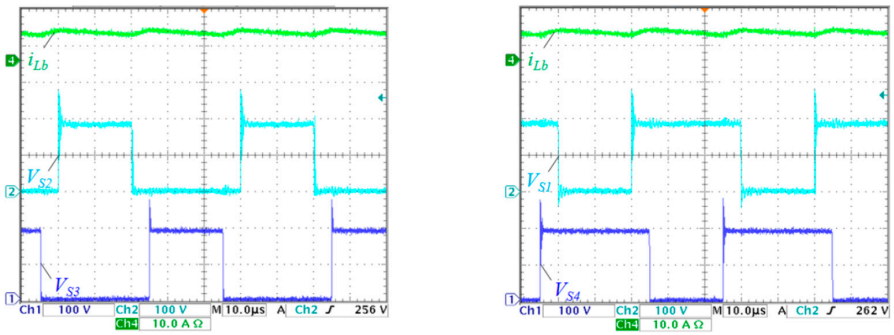
A 1.0 kW prototype circuit was designed and tested for the electrical specifications and circuit parameters in Table 1. The low voltage V_L ranges from 140 V to 160 V. The high voltage V_H ranges from 360 V to 400 V. The valve-regulated lead–acid batteries were used for the low voltage side. Its nominal voltage for each battery cell is 24 V. This type of system configuration can be utilized for grid-tied battery energy storage system applications where the battery power can be transferred into the grid or recharged from the grid.

Figure 8 shows the experimental waveforms of the conventional converter in Figure 1 in the step-up mode. The conventional converter can be tested by removing the *LC* resonant circuits in the proposed converter. Figure 8a shows i_{Lb}, V_{S2}, and V_{S3}. Figure 8b shows i_{Lb}, V_{S1}, and V_{S4}. i_{Lb} is positively continuous because the converter is in the step-up mode. The on-time of S_1 (S_2) is shifted by T_s/2, with respect to the on-time of S_4 (S_3). As shown in Figure 8, a voltage spike is observed at the moment that each switch is turned off. This voltage spike causes the turn-on switching loss for the power switch, which eventually decreases the power efficiency. Figure 9 shows the experimental waveforms of the proposed converter in the step-up mode. Figure 9a shows i_{Lb}, i_{Lr2}, V_{S2}, and V_{S3}. Figure 9b shows i_{Lb}, i_{Lr1}, V_{S1}, and V_{S4}. i_{Lb} is positively continuous. i_{Lr1} and i_{Lr2} flow bidirectionally with a phase-shift of T_s/2 with respect to each other. At the moment that each switch is turned off, the voltage across the power switch is clamped to V_H/2 as 185 V. Figure 9c shows V_{gs2}, V_{S2}, V_{gs3}, and V_{S3}.

Figure 9d shows V_{gs1}, V_{S1}, V_{gs4}, and V_{S4}. As shown in Figure 9c,d, the switch voltage decreases to zero voltage before the gate signal is applied to the power switch. Power switches are turned on at zero voltage. Figure 9e shows i_{S2}, V_{S2}, i_{S3}, and V_{S3}. Figure 9f shows i_{S1}, V_{S1}, i_{S4}, and V_{S4}. Compared to the experimental results in Figure 8, no voltage spike is observed at the moment that each switch is turned off in Figure 9. With the help of the auxiliary circuit, the proposed converter has eliminated the turn-on switching losses for S_1, S_2, S_3, and S_4 effectively in the step-up mode.

Table 1. Electrical specifications and circuit parameters.

Symbol	Quantity	Value
V_L	low voltage	140–160 V
V_H	high voltage	360–400 V
P_d	rated power	1000 W
T_s	swiching period	50 µsec
T_d	dead time	2 µsec
S_1, S_2, S_3, S_4	power switch	IXFP30N25X3
C_{S1}, C_{S2}, C_{S3}, C_{S4}	capacitor	1450 pF
L_b	inductor	600 µH (CM508125)
C_{o1}, C_{o2}	capacitor	560 µF/450 V
L_{r1}, L_{r2}	inductor	100 µH (EE2828)
C_{r1}, C_{r2}	capacitor	2 µF/630 V



(**a**) (**b**)

Figure 8. The experimental waveforms of the conventional converter in the step-up mode: (**a**) i_{Lb}, V_{S2}, and V_{S3}; (**b**) i_{Lb}, V_{S1}, and V_{S4}.

Figure 10 shows the experimental waveforms of the conventional converter in the step-down mode. Figure 10a shows i_{Lb}, V_{S1}, and V_{S4}. Figure 10b shows i_{Lb}, V_{S2}, and V_{S3}. i_{Lb} is negatively continuous because the converter is in the step-down mode. The on-time of S_1 (S_2) is shifted by $T_s/2$, with respect to the on-time of S_4 (S_3). As shown in Figure 10, a voltage spike is observed at the moment that each switch is turned off. This voltage spike causes the turn-on switching loss for the power switch, which eventually decreases the power efficiency. Figure 11 shows the experimental waveforms of the proposed converter in the step-down mode. Figure 11a shows i_{Lb}, i_{Lr1}, V_{S1}, and V_{S4}. Figure 11b shows i_{Lb}, i_{Lr2}, V_{S2}, and V_{S3}. i_{Lb} is negatively continuous. i_{Lr1} and i_{Lr2} flow bidirectionally with a phase-shift of $T_s/2$ with respect to each other. At the moment that each switch is turned off, the voltage across the power switch is clamped to $V_H/2$ as 185 V. Figure 11c shows V_{gs1}, V_{S1}, V_{gs4}, and V_{S4}. Figure 11d shows V_{gs2}, V_{S2}, V_{gs3}, and V_{S3}. As shown in Figure 11c,d, the switch voltage decreases to zero voltage before the gate signal is applied to the power switch. Power switches are turned on at zero voltage. Figure 11e shows i_{S1}, V_{S1}, i_{S4}, and V_{S4}. Figure 11f shows i_{S2}, V_{S2}, i_{S3}, and V_{S3}. Compared to the experimental results in Figure 10, no voltage spike is observed at the moment that each switch is turned off in Figure 11. By the operation of the auxiliary circuit, the proposed converter has eliminated the turn-on switching losses for S_1, S_2, S_3, and S_4 in the step-down mode. By eliminating the turn-on switching losses, the proposed converter increases the power efficiency for both step-up and step-down modes.

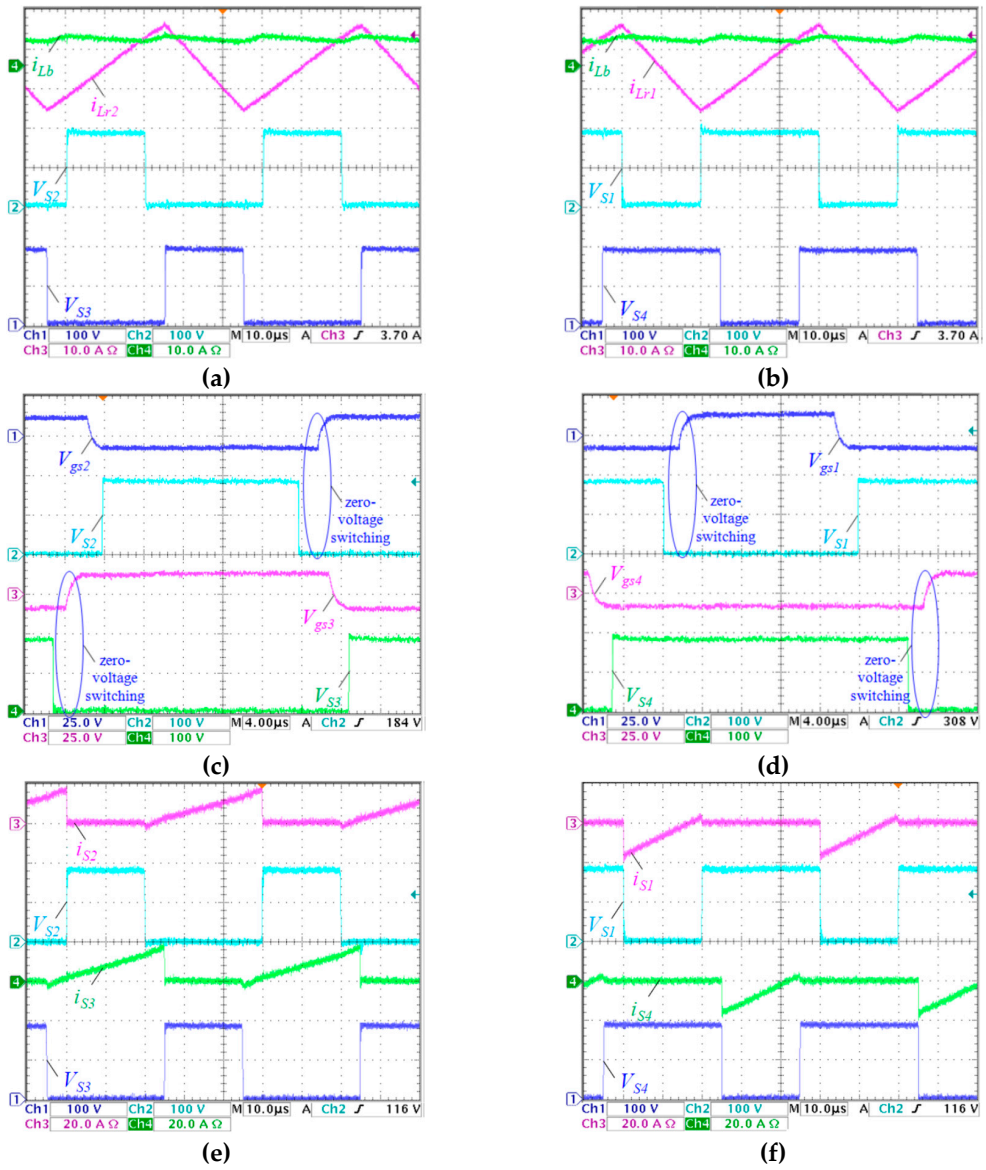


Figure 9. The experimental waveforms of the proposed converter in the step-up mode: (**a**) i_{Lb}, i_{Lr2}, V_{S2}, and V_{S3}; (**b**) i_{Lb}, i_{Lr1}, V_{S1}, and V_{S4}; (**c**) V_{gs2}, V_{S2}, V_{gs3}, and V_{S3}; (**d**) V_{gs1}, V_{S1}, V_{gs4}, and V_{S4}; (**e**) i_{S2}, V_{S2}, i_{S3}, and V_{S3}; (**f**) i_{S1}, V_{S1}, i_{S4}, and V_{S4}.

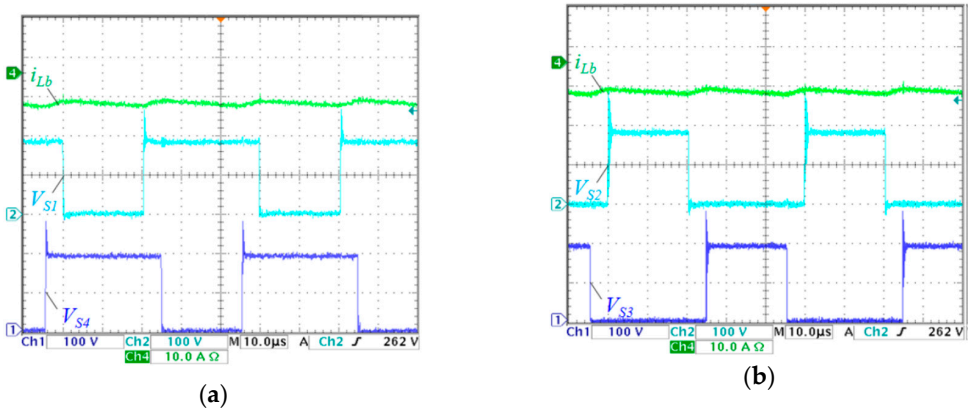


Figure 10. The experimental waveforms of the conventional converter in the step-down mode: (**a**) i_{Lb}, V_{S1}, and V_{S4}; (**b**) i_{Lb}, V_{S2}, and V_{S3}.

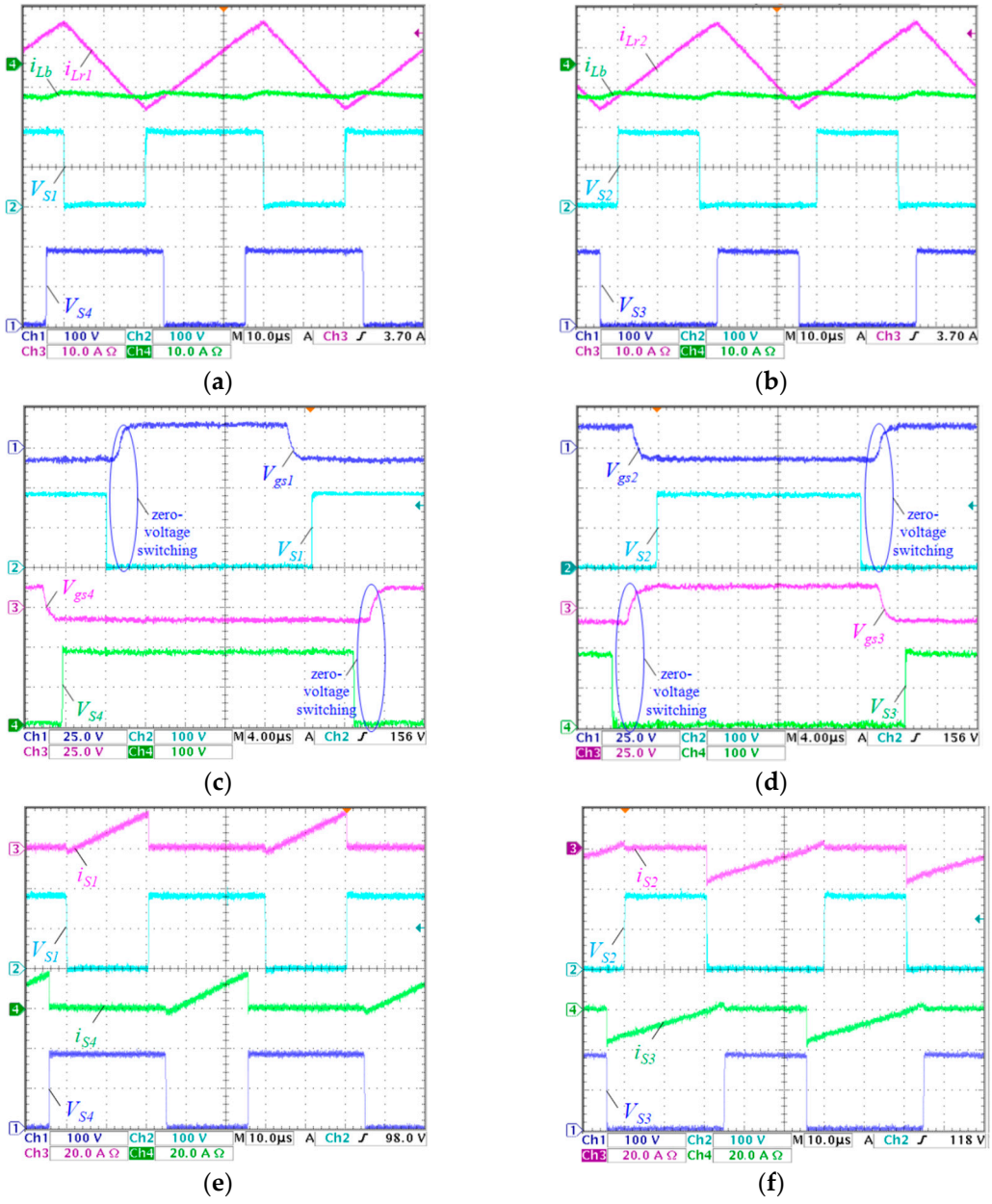


Figure 11. The experimental waveforms of the proposed converter in the step-down mode: (**a**) i_{Lb}, i_{Lr1}, V_{S1}, and V_{S4}; (**b**) i_{Lb}, i_{Lr2}, V_{S2}, and V_{S3}; (**c**) V_{gs1}, V_{S1}, V_{gs4}, and V_{S4}; (**d**) V_{gs2}, V_{S2}, V_{gs3}, and V_{S3}; (**e**) i_{S1}, V_{S1}, i_{S4}, and V_{S4}; (**f**) i_{S2}, V_{S2}, i_{S3}, and V_{S3}.

Figure 12 shows the power efficiency curves of the converters according to the operation modes. The power efficiency has been calculated by dividing the output power by the input power. The digital power meter (WT-230, YOKOGAWA) was used for the efficiency measurement. Figure 12a shows the power efficiency curves in the step-up mode. The conventional converter has an efficiency of 97.1% at 1.0 kW. The peak efficiency is 97.6% at 0.7 kW. The proposed converter has an efficiency of 97.7% at 1.0 kW. The peak efficiency is 98.1% at 0.7 kW. Figure 12b shows the power efficiency curves in the step-down mode. The conventional converter has an efficiency of 97.2% at 1.0 kW. The peak efficiency is 97.5% at 0.7 kW. The proposed converter has an efficiency of 97.8% at 1.0 kW. The peak efficiency is 98.2% at 0.7 kW. Figure 12c shows the power efficiency curves of the proposed converter for different inductor values of L_r at the rated power when C_r is 2 µF. Figure 12d shows the power efficiency curves of the proposed converter for different capacitor values of C_r at the rated power when L_r is 100 µH.

As shown in Figure 12c,d, the proposed converter shows its best performance when L_r = 100 µH and C_r = 2 µF are chosen for the resonant parameters.

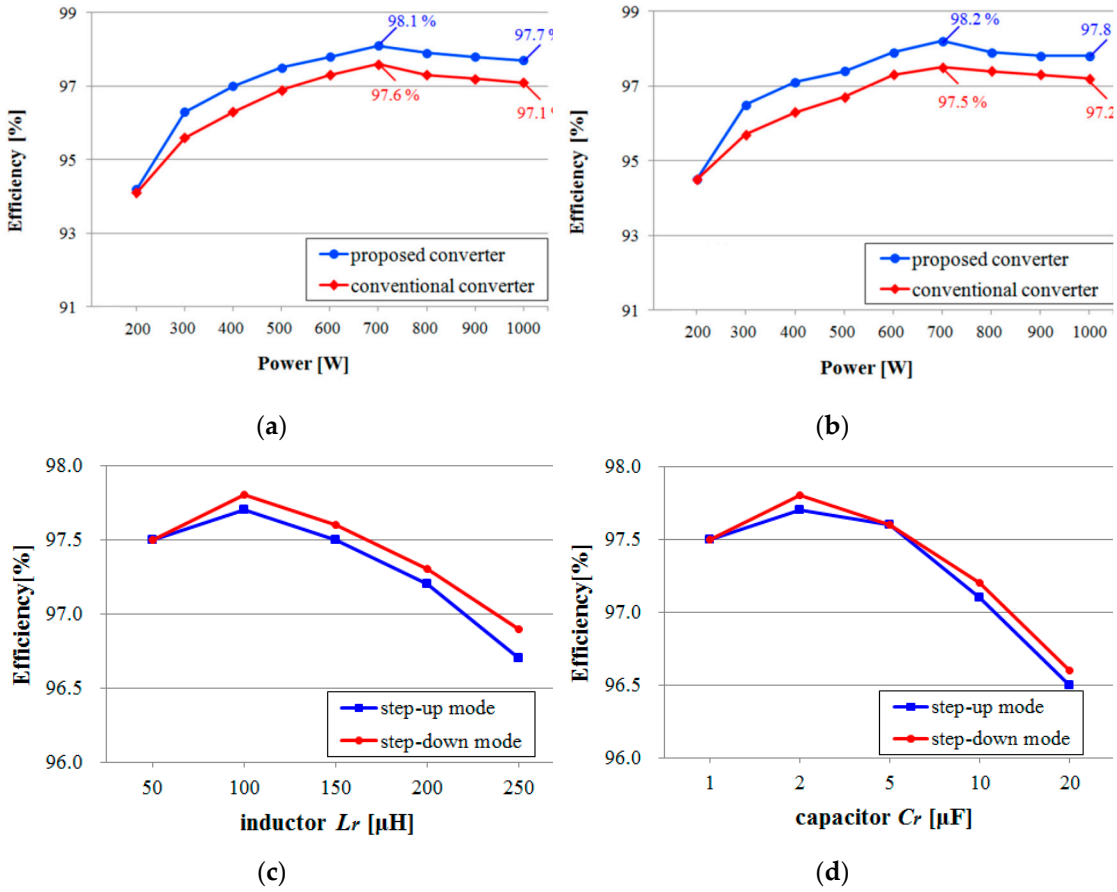


Figure 12. The power efficiency curves of the converters: (**a**) Power efficiency curves in the step-up mode; (**b**) Power efficiency curves in the step-down mode; (**c**) Power efficiency curves for different inductor values of L_r at the rated power; (**d**) Power efficiency curves for different capacitor values of C_r at the rated power.

3.3. Power Loss Analysis

The proposed converter improves the power efficiency by eliminating the turn-on switching loss P_{turn_on} of the power switch, which is the most significant part of power losses when the MOSFETs are used. The proposed converter has turn-off switching losses and conduction losses. Assuming that $\Delta i_{Lr} = \Delta i_{Lr1} = \Delta i_{Lr2}$, the average turn-off switching loss P_{turn_off} is

$$P_{turn\_off} = \frac{V_H}{4T_s}\left(\left|i_{Lb,avg}\right| + \frac{\Delta i_{Lr}}{2}\right) t_{turn\_off} \tag{21}$$

where t_{turn_off} is the turn-off moment time, including the current falling time and the voltage rising time of the switch, as described in [23]. The average conduction loss P_{cond} is

$$P_{cond} = R_{ds(on)} D \left(\left|i_{Lb,avg}\right| + \frac{\Delta i_{Lr}}{2}\right)^2 \tag{22}$$

where $R_{ds(on)}$ is the on-state resistance of the power switch. Other power losses P_{others} for L_b and switch gate-driving circuits are hardly affected by the proposed scheme, except the power losses for L_{r1} and L_{r2}. The power loss P_{res_ind} in the resonant inductor L_r includes the copper loss and the core loss. Table 2 shows the power loss distributions of the converters for the step-up mode and the step-down mode.

As the power level increases, the sum of P_{turn_on}, P_{turn_off}, and P_{cond} in the conventional converter is higher than the sum of P_{turn_off}, P_{cond}, and P_{res_ind} in the proposed converter.

Table 2. Power loss distributions of the converters.

	Step-Up Mode		Step-Down Mode	
	Conventional Converter	**Proposed Converter**	**Conventional Converter**	**Proposed Converter**
P_{turn_on}	11.0 W	0 W	10.4 W	0 W
P_{turn_off}	7.6 W	9.6 W	7.4 W	9.2 W
P_{cond}	7.4 W	9.0 W	7.2 W	8.6 W
P_{res_ind}	0 W	1.4 W	0 W	1.2 W
P_{others}	3.0 W	3.0 W	3.0 W	3.0 W
P_{total}	29.0 W	23.0 W	28.0 W	22.0 W

4. Conclusions

This paper has suggested a soft-switching bidirectional three-level DC–DC converter, which can effectively reduce the switching power losses with a simple auxiliary circuit. Two *LC* resonant circuits were used for reducing the turn-on switching power losses of main power switches. Power switches are turned on at zero voltage by the resonant operation of the *LC* resonant circuits. The proposed converter has reduced switching power losses and improves power efficiency, compared to the previous converters, which operate without any auxiliary circuits, suffering from high switching losses. The steady-state operation of the proposed converter was described. Its zero-voltage switching condition was analysed. A 1.0 kW prototype circuit was designed and tested for the experimental verifications of the proposed converter. The proposed converter achieved higher power efficiency than the conventional converter. It achieved the power efficiencies of 97.7% in the step-up mode and 97.8% in the step-down mode for the rated load condition.

The proposed converter can be utilized for a grid-tied battery energy storage system, which requires high power efficiency and high power density. Because of their three-level power conversion structure, high performance inverters, such as neutral point-clamped and three-level inverters, can be interfaced with the proposed converter. The proposed converter can be applied for the bidirectional DC–DC converter for both single-phase and three-phase grid-connected applications. The proposed converter is expected to be a good candidate for the interface between the battery and the grid-connected inverter to exchange electrical power with high efficiency and manage energy conversion.

Author Contributions: W.Y.C. managed the project, and mainly wrote the manuscript. M.K.Y. performed the experiments, analyzed the data, and edited the manuscript.

Funding: This research was supported by the National Research Foundation of Korea (NRF-2016R1D1A3B03932350).

Conflicts of Interest: The authors declare no potential conflict of interest.

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