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Parameters Design and Optimization of a High Frequency, Interleaved, Dual-Buck, Bidirectional, Grid-Connected Converter

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Abstract: In this paper, a high frequency, interleaved, dual-buck, bidirectional, grid-connected converter topology is proposed. Free from the straight-through and dead-time distortion issues, both higher switching frequency and power density can be achieved. Due to the interleaved technique, the current ripple and stress for inductors and other power devices can be effectively reduced. Moreover, a novel filter parameter design method is proposed. The method is optimized with smaller inductance, higher filtering performance, and better steady-state performance. For one thing, the performance requirements under the two states of inverter and rectifier are comprehensively considered. For another, the relationship between the performance indexes and the filter parameters is analyzed. However, the results show that the relationship between the performance indexes is contradictory. A set of optimization parameters were obtained by setting the priority of the filter performance index. The specific design process of the filter parameters is given in detail. In order to verify the rationality of the parameter design, a 5 kW prototype was built and tested. The total harmonic distortions (THDs) of the grid currents in the among grid-connected inverter, off-connected inverter, and rectifier states under full load were 2.7%, 1.2%, and 4.5%, respectively, and the power density reached 36 W/in^3.

Keywords: dual-buck; bidirectional; grid-connected converter; parameter design

1. Introduction

Energy storage units are widely used in distributed new energy, grid-connected power generation systems. On one hand, they reduce the power fluctuation of power grid systems. On the other hand, they improve the friendliness of the energy interaction between the users and grid. However, the efficiency and power density of the energy storage unit needs to be further improved [1–3]. Therefore, as the interface circuit of distributed energy storage units, the grid-connected converter needs to highlight two aspects of performance: (1) High efficiency to achieve the bidirectional flow of energy. (2) Smaller volume and lower weight. According to the research of relevant scholars, the methods of improving power density are as follows: (1) To increase the working frequency and reduce the size of the filter. (2) To design the filter parameters reasonably and to reduce the nominal value of the filter elements to achieve a higher power density [4–10].

Increasing the operating frequency of the converter can greatly reduce the size of the inductors and capacitors. Thereby, the power density of the converter is improved. However, the traditional bridge-based converter needs to inject dead-time, which limits the increase of the operating frequency. Further, the dead-time will lead to more waveform distortion. Therefore, compared with the traditional bridge circuit, the new type of grid-connected converter without straight-through (i.e., without injecting dead zone) has certain research value. References [11,12] present a dual-buck, bridge-less inverter

topology, which overcomes the problem of straight-through without injecting dead-time. It is beneficial to realize high operating frequency of the converter. Reference [13] proposes a dual-input, dual-buck, bridge-free topology without dead-zone distortion. It greatly reduces the injection of low-order harmonics and has a high power factor. Reference [14] proposes a dual-output, dual-buck converter, which improves the load capacity while retaining the advantages of the buck converter. Reference [15] introduces an interleaved technology on the basis of a dual-buck converter to further reduce the inductance current ripple. It reduces the size of the filter and improves the power density of the converter. In the above literatures, dual-buck, bridge-free topology is used to effectively eliminate the problem of straight-through, reduce the injection of low-order harmonics, and significantly improve the quality of circuit waveforms. In addition, most of the converters use SiC devices, which effectively improves the switching frequency. However, the above literatures only discuss unidirectional power flow and do not involve bidirectional power flow. Therefore, the research on bidirectional, grid-connected converters still needs to be carried out.

Moreover, a series of research work about the design method of filter parameters has been carried out. In references [16,17], the inductance and capacitance of the filter were obtained by preset ripple, reactive power limitation, and resonant frequency. The design method was simple, feasible, and easy to calculate. However, the constraints among the filter parameters were not considered, which has a certain impact on the performance of the filter. Reference [18] comprehensively considered the relationship between the attenuation of resonant peaks and circuit losses and achieved the design of filter parameters. This design method improves the stability of the converter, however the introduction of filter resistance will have a certain impact on the efficiency. Reference [19] designed the filter parameters according to the relationship between filter parameters and total harmonic distortion (THD) and achieved a better filtering effect. In reference [20], the parameters of the filter were designed by using the restriction of the resonant frequency of the filter. The design method takes into account the harmonic suppression ability and the stability of the system and has high practicability. However, references [19,20] did not fully consider the relationship between filter parameters and performance indexes. Reference [21] synthetically considered the performance indexes of the filter and drew the relationship curves between the filter parameters and the performance indexes. The design method is more intuitive, however the process is more complicated. In the above literatures, the design of the filter is based on the characteristics of the circuit and the design objectives are clear and the design method is feasible. However, most of the above literatures take single performance as the optimization target and do not consider the constraints between various performances. Thus, it is difficult to take into account multiple performance requirements at the same time. What is more, the power density of the converter is not taken as the optimization target. In addition, the above parameter design methods are discussed on the basis of unidirectional power flow, which has not been extended to the case of bidirectional power flow and has certain limitations. Therefore, it is of great importance to study the design method of bidirectional converter filter parameters.

In this paper, based on SiC power devices, a high frequency, interleaved, dual-buck, bidirectional, grid-connected converter is proposed. The topology has two states: inverter state and rectifier state. Firstly, model analysis of the two states will be carried out in Section 2. Then, a parameter design method considering the performance requirements of both the inverter and rectifier states will be proposed in Section 3. In this method, the coupling relationship between the filter parameters and performance indexes is considered comprehensively. Taking power density, filtering performance, and stability as optimization targets, a set of reasonable parameters are obtained by setting a target priority. Finally, an experimental prototype with a rated power of 5 kW is built to verify the theoretical analysis in Section 4.

2. Topology Description and Operation Principles

2.1. Topology Description

The topology of the proposed interleaved, dual-buck, bidirectional, grid-connected converter is illustrated in Figure 1, which includes the inverter state and the rectifier state. In the inverter state, the circuit consists of four identical Buck circuits: S_1, S_3, D_1, and L_{i1} form Buck1; S_1, S_4, D_2, and L_{i2} form Buck2; S_2, S_5, D_3, and L_{i3} form Buck3; and S_2, S_6, D_4, and L_{i4} form Buck4. The driving signal of switch S_3 of Buck1 leads that of switch S_4 of Buck2 by 180 degrees, which constitutes inverter interleaving unit 1. The driving signal of switch S_5 of Buck3 leads that of switch S_6 of Buck4 by 180 degrees, which constitutes inverter interleaving unit 2. In a grid line period, two groups of inverter interleaving units work alternately in each half cycle to realize the inverter function.

In the rectifier state, the circuit consists of four identical Boost circuits: S_5, L_{i3}, D_3, S_3, S_4, L_{i1}, L_{i2}, and L_g form Boost1; S_6, L_{i4}, D_4, S_3, S_4, L_{i1}, L_{i2}, and L_g form Boost2; S_3, L_{i1} D_1, S_5, S_6, L_{i3}, L_{i4}, and L_g form Boost3; and S_4, L_{i2}, D_2, S_5, S_6, L_{i3}, L_{i4}, and L_g form Boost4. The driving signal of switch S_5 of Boost1 leads that of switch S_6 of Boost2 by 180 degrees, which constitutes rectifier interleaving unit 1. The driving signal of switch S_3 of Boost3 leads that of switch S_4 of Boost4 by 180 degrees, which constitutes rectifier interleaving unit 2. In a grid line period, two groups of rectifier interleaving units work alternately in each half cycle to realize the rectifier function.

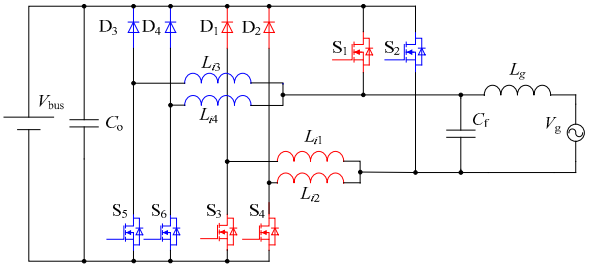


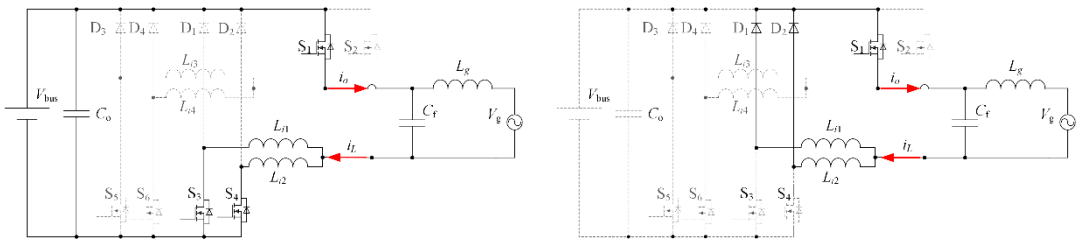
Figure 1. Topological diagram of the proposed converter.

2.2. Operation Principles

In order to simplify the analysis, the following assumptions are proposed:

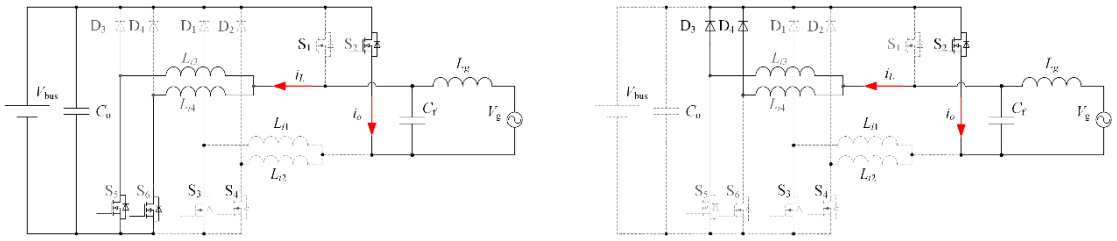
(1) All devices in the topology are ideal.
(2) Compared with the grid current, the current of output capacitor C_f is small enough to be ignored.
(3) The circuit is in a steady state.

Based on the above assumptions, each state can be divided into four intervals according to the operation of the interleaving unit. The equivalent circuits of the four intervals in the inverter state are shown in Figure 2. The equivalent circuits of the four intervals in the rectifier state are shown in Figure 3.



(**a**) (**b**)

Figure 2. *Cont.*



(**c**) (**d**)

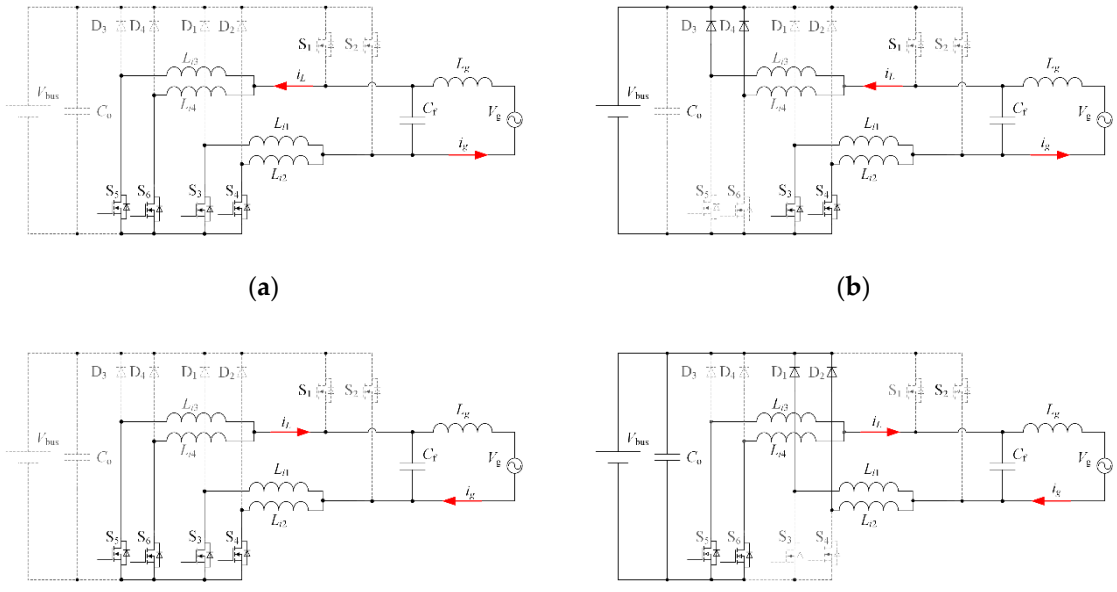
Figure 2. Equivalent circuits of the inverter state. (**a**) Inverter a, (**b**) Inverter b, (**c**) Inverter c, (**d**) Inverter d.

Inverter interval a: In the positive half period of the grid, the inverter interleaving unit 1 works. S_1 is always on and S_5, S_6, D_1, D_2, D_3, and D_4 are disconnected. There is a 180 degree phase difference between the driving signal of S_3 and that of S_4. S_3 and S_4 are interleaved turned on, and energy is supplied from the DC side to the AC side through inductors L_{i1}, L_{i2}, and L_g.

Inverter interval b: In the positive half period of the grid, the inverter interleaving unit 1 works. S_1 is always on and S_5, S_6, S_3, S_4, D_3, and D_4 are disconnected. D_1 and D_2 turn-on, and energy in inductors L_{i1}, L_{i2}, and L_g is supplied to the AC side by diodes.

Inverter interval c: In the negative half period of the grid, the inverter interleaving unit 2 works. S_2 is always on and S_3, S_4, D_1, D_2, D_3, and D_4 are disconnected. There is a 180 degree phase difference between the driving signal of S_5 and that of S_6. S_5 and S_6 are interleaved turned on, and energy is supplied from the DC side to the AC side through inductors L_{i3}, L_{i4}, and L_g.

Inverter interval d: In the negative half period of the grid, the inverter interleaving unit 2 works. S_2 is always on and S_3, S_4, S_5, S_6, D_1, and D_2 are disconnected. D_3 and D_4 turn-on, and energy in inductors L_{i3}, L_{i4}, and L_g is supplied to the AC side by diodes.



(**a**) (**b**)

(**c**) (**d**)

Figure 3. Equivalent circuits of the rectifier state. (**a**) Rectifier a, (**b**) Rectifier b, (**c**) Rectifier c, (**d**) Rectifier d.

Rectifier interval a: In the positive half period of the grid, the rectifier interleaving unit 1 works. S_3 and S_4 are always on. S_1, S_2, D_1, D_2, D_3, and D_4 are disconnected. There is a 180 degree phase difference between the driving signal of S_5 and that of S_6. S_5 and S_6 are interleaved turned on, and AC

energy flows through the switch to charge inductors L_{i1}, L_{i2}, L_{i3}, L_{i4}, and L_g, and the energy in the inductors rises.

Rectifier interval b: In the positive half period of the grid, the rectifier interleaving unit 1 works. S_3 and S_4 are always on and S_1, S_2, S_5, S_6, D_1, and D_2 are disconnected. D_3 and D_4 turn-on, energy in the inductors and AC energy are superimposed to the DC side, and the energy in the inductances decreases.

Rectifier interval c: In the negative half period of the grid, the rectifier interleaving unit 2 works. S_5 and S_6 are always on. S_1, S_2, D_1, D_2, D_3, and D_4 are disconnected. There is a 180 degree phase difference between the driving signal of S_3 and that of S_4. S_3 and S_4 are interleaved turned on, and AC energy flows through the switch to charge inductors L_{i1}, L_{i2}, L_{i3}, L_{i4}, and L_g, and the energy in the inductors rises.

Rectifier interval d: In the negative half period of the grid, the rectifier interleaving unit 2 works. S_5 and S_6 are always on and S_1, S_2, S_3, S_4, D_3, and D_4 are disconnected. D_1 and D_2 turn-on, energy in the inductors and AC energy are superimposed to the DC side, and the energy in the inductances decreases.

2.3. Ripple Analysis

According to the model analysis of the equivalent circuits, the sequence diagram of the inverter state is depicted in Figure 4. In the inverter state, the operation cycle of S_1 and S_2 is the same as that of the power grid. The operation frequencies of S_3, S_4, S_5, and S_6 are all 50 kHz. In the positive half-cycle of the grid, S_1 is always on and S_3 and S_4 are interleaved turned-on. In the negative half-cycle of the grid, S_2 is always on and S_5 and S_6 are interleaved turned-on.

By magnifying the driving waveform region marked by the arrow in Figure 4, the detailed waveforms can be obtained as in Figure 5. Moreover, the current waveforms of inductors L_{i1} and L_{i2} are drawn according to the driving waveforms. It is obvious that the sum of the inductance current ripples of the interleaving unit is lower than that of any branch of the interleaving unit. It is proved that interleaved parallel technology can reduce the requirement of inductance and reduce the circuit weight. Further, the sequence diagram analysis of the rectifier state is similar to that of the inverter state. Therefore, the description is not repeated here.

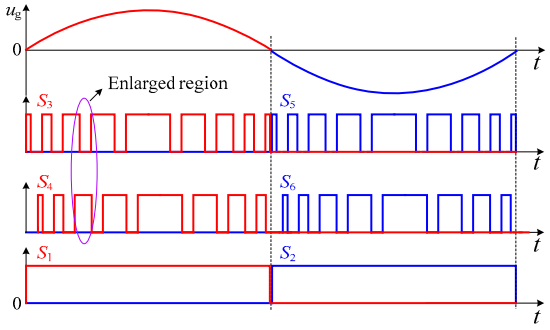


Figure 4. Equivalent circuits of the inverter state.

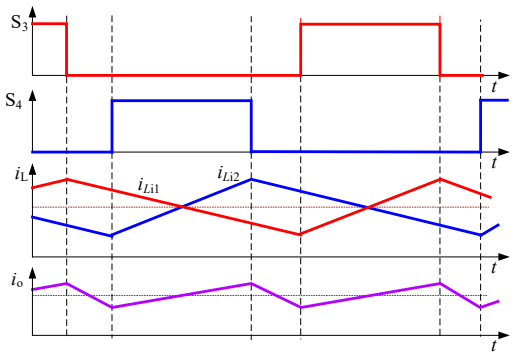


Figure 5. Amplified waveforms in the inverter state.

3. Parameter Design

The performance of the filter is directly affected by the filter parameters. Thereby, the parameters of the filter should be designed carefully to obtain the desirable performance. As for the proposed converter, the filter consists of L_{i1}, L_{i2}, L_{i3}, L_{i4}, L_g, C_f, and C_o. Among them, L_{i1}, L_{i2}, L_{i3}, L_{i4}, C_f, and L_g constitute the LCL filter in the inverter state, and L_{i1}, L_{i2}, L_{i3}, L_{i4}, L_g, and C_o constitute the LC filter in the rectifier state. It is obvious that the structures of the filter are different in the two states. In addition, the coupling relationship among the filter parameters leads to the interaction of parameters. As a consequence, the conventional parameter design method for the unidirectional converter is no longer applicable to the proposed converter.

In this paper, a novel parameter design method is proposed, which takes into account the performance requirements of the two states. The main goal is to fulfill high power density, good filtering performance, and good steady-state performance. The method can be divided into three steps. To start with, a generalized range of filter parameters is obtained according to the working principle and process of the circuit. Secondly, the range of filter parameters is optimized by analyzing the coupling relationship among the parameters. In the end, a set of reasonable parameters is obtained by setting the priority of the filter performance index. The specific design process of this method will be given in detail as follows. In order to simplify the analysis process, it is assumed that the inductance values of L_{i1}, L_{i2}, L_{i3}, and L_{i4} are equal, which are denoted by L_i. Further, the equivalent total inductance L_a in the inverter state and the total inductance L_b in the rectifier state is defined as shown in (1):

$$\begin{cases} L_a = L_i + L_g \\ L_b = 1.5L_i + L_g \end{cases} \tag{1}$$

3.1. Parameter Selection

The proposed converter has two states of inverter and rectifier. According to the equivalent circuit and operation mode, the filter parameters of the two states are calculated separately. The preliminary range of filter inductance and capacitance is obtained.

3.1.1. Preliminary Range of Filter Inductance

According to the working principle of the converter, the voltage vector diagram of the converter in different states is drawn as shown in Figure 6. In the figure, grid voltage vector is represented by $\boldsymbol{u_g}$, grid current vector is represented by $\boldsymbol{i_g}$, total filter inductance voltage vector is represented by $\boldsymbol{u_L}$, DC voltage vector is represented by $\boldsymbol{u_{dc}}$, and θ represents the angle between $\boldsymbol{u_{dc}}$ and $\boldsymbol{u_g}$. According to the different impedance angles of the power grid, the angle of $\boldsymbol{i_g}$ lagging behind $\boldsymbol{u_g}$ will change, and at the same time θ will also change.

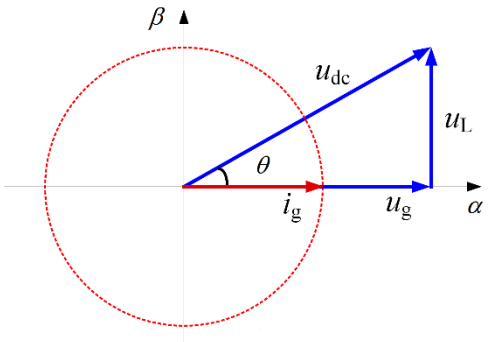


Figure 6. Voltage vector diagram of the converter.

According to the voltage vector diagram, the relationship among $\boldsymbol{u_{dc}}$, $\boldsymbol{u_g}$, and $\boldsymbol{i_g}$ can be obtained from cosine theorem as shown in (2):

$$u_L{}^2 = u_{dc}{}^2 + u_g{}^2 - 2u_{dc}u_g \cos\theta. \tag{2}$$

Formula (3) can be obtained by deriving θ from (2):

$$\frac{du_L{}^2}{d\theta} = 2u_{dc}u_g \sin\theta. \tag{3}$$

From (3), we can see that $\boldsymbol{u_L}$ is proportional to θ. When the phase of $\boldsymbol{i_g}$ and $\boldsymbol{u_g}$ is the same, θ is the largest. Therefore, the maximum inductance voltage u_{L_max} is obtained in (4). Where L represents the total inductance in the filter circuit, i_L is the filter inductance current and ω is the rated angular frequency of the grid.

$$\begin{cases} u_{L\_max} = \omega L i_L \\ u_{L\_max}^2 = u_{dc}^2 - u_g^2 \end{cases} \tag{4}$$

The filter inductances of the inverter and rectifier states are calculated respectively. According to (4), the maximum total inductance L_{a_max} of the converter in the inverter state can be expressed as (5), where V_{dc}, V_g represent DC voltage and grid voltage.

$$L_{a\_max} = L_i + L_g = \frac{\sqrt{V_{dc}^2 - V_g^2}}{\omega i_L} \tag{5}$$

In the inverter state, in order to prevent the converter from producing high current ripple, the converter should work in continuous conduction mode (CCM). The critical inductance value L_{a_min1}, which satisfies the CCM in the inverter state, can be obtained by (6). Where d represents duty cycle, i_{dc} is direct current, f_s is switching frequency, and V_{gm} is the peak value of the grid voltage.

$$\begin{cases} L_{a\_min1} = L_i + L_g = \frac{V_{dc}(1-d)d^2}{2i_{dc}f_s} \\ d = \frac{V_{gm}}{V_{dc}} \sin(\omega t) \end{cases} \tag{6}$$

The derivation of d in (6) shows that the critical inductance value is the largest when d is 2/3 in the inverter state. The duty cycle d varies sinusoidally with time in the inverter state. Therefore, in order to ensure that the converter always works in CCM, the equivalent filter inductance should be larger than the maximum critical inductance L_{a_min1}.

According to the working principle of the Buck circuit, the ripple ΔI_a of the inductance current in the inverter state is calculated as (7), where T_s represents the switching period.

$$\begin{cases} \Delta I_a = \frac{V_g(1-2d)T_s}{L_a} (d < 0.5) \\ \Delta I_a = \frac{(V_{dc}-V_g)(2d-1)T_s}{L_a} (d > 0.5) \\ d = \frac{V_{gm}}{V_{dc}} \sin(\omega t) \end{cases} \tag{7}$$

By deriving d from (7), we can see that during $d < 0.5$, the maximum inductance current ripple ΔI_{a_max1} can be obtained when d equals 0.25. During $d > 0.5$, the maximum inductance current ripple ΔI_{a_max2} can be obtained when d equals 0.75. The value of ΔI_{a_max1} is equal to I_{a_max2}, which is $V_{dc}T_s/8L_a$ and can be expressed by ΔI_{a_max}. The minimum equivalent filter inductance L_{a_min2} in the inverter state can be obtained as follows:

$$L_{a\_min2} = L_i + L_g = \frac{V_{dc}T_s}{8\Delta I_{a\_max}} \tag{8}$$

For the same reason, according to (4), the maximum total inductance L_{b_max} of the converter in the rectifier state can be obtained:

$$L_{b\_max} = 1.5L_i + L_g = \frac{\sqrt{V_{dc}^2 - u_g^2}}{\omega i_L} \tag{9}$$

Similarly, in order to prevent the converter from producing high current ripple in the rectifier state, the converter should work in CCM. The critical inductance value L_{b_min1}, which satisfies the CCM in the rectifier state, can be obtained by (10).

$$\begin{cases} L_{b\_min1} = 1.5L_i + L_g = \frac{V_{dc}(1-d)^2 d}{2i_{dc}f_s} \\ d = \frac{V_{dc} - V_{gm}\sin(\omega t)}{V_{dc}} \end{cases} \tag{10}$$

The derivation of d in (10) shows that the critical inductance value is largest when d is 1/3 in the rectifier state. The duty cycle d varies with time in the rectifier state. Therefore, in order to ensure that the converter always works in CCM, the equivalent filter inductance should be larger than the maximum critical inductance L_{b_min1}.

According to the working principle of the Boost circuit, the ripple ΔI_b of the inductance current in the rectifier state is calculated as (11).

$$\begin{cases} \Delta I_b = \frac{(V_{dc} - V_g)(1-2d)T_s}{L_b} (d < 0.5) \\ \Delta I_b = \frac{V_g(2d-1)T_s}{L_b} (d > 0.5) \\ d = \frac{V_{dc} - V_{gm}\sin(\omega t)}{V_{dc}} \end{cases} \tag{11}$$

By deriving d from (11), we can see that during $d < 0.5$, the maximum inductance current ripple ΔI_{b_max1} can be obtained when d equals 0.25. During $d > 0.5$, the maximum inductance current ripple ΔI_{b_max2} can be obtained when d equals 0.75. The value of ΔI_{b_max1} is equal to I_{b_max2}, which is $V_{dc}T_s/8L_b$ and can be expressed by ΔI_{b_max}. The minimum equivalent filter inductance L_{b_min2} in the rectifier state can be obtained as follows:

$$L_{b\_min2} = 1.5L_i + L_g = \frac{V_{dc}T_s}{8\Delta I_{b\_max}}. \tag{12}$$

3.1.2. Preliminary Range of Filter Capacitance

When the converter operates in the inverter state, to ensure high power factor to transfer energy based on the converter hardware, according to the standard IEEE-519/IEEE-1547, the output reactive power must not exceed 5% of the active power. Thus, the maximum value C_{fmax} of the filter capacitor can be obtained as shown in (13). Where S_n is the rated capacity of the converter, U_n is the rated voltage of the grid.

$$C_{fmax} = \frac{S_n}{\omega \cdot U_n^2} \cdot 5\% \tag{13}$$

When the converter operates in the rectifier state, to ensure that the output voltage meets the ripple requirement, according to the standard GB/T3797-1989, the fluctuation of the DC voltage could not exceed 15% of the rated voltage value. Thus, the minimum value of the filter capacitor is C_{o_min}, as shown in (14). Where P_o represents the output power of the converter, V_n is the rated voltage of the DC bus, and ΔV is the voltage ripple of the DC bus.

$$C_{o\_min} = \frac{P_o}{2\pi f_s \cdot V_n \cdot \Delta V} \tag{14}$$

3.2. Parameter Optimization

Since during the rectifier state, the filter was equal to a second-order system, there was no coupling relationship between the inductance parameters of the filter. Therefore, this section only focuses on the inverter state. In the inverter state, grid-connected current harmonics mainly include two aspects: (1) High-order harmonics generated by switching operation; (2) Low-order harmonics introduced under the background of the power grid. Among them, the frequency of the low-order harmonics is lower than the shear frequency of the closed loop system. Therefore, low-order harmonics can be suppressed by control [22], while high-order harmonics are difficult to suppress. In order to improve the waveform quality, it is necessary to design the filter reasonably to suppress the high-order harmonic current. Next, according to the suppression ability of the high-order harmonic current, the relationship among the filter parameters in the inverter state is decoupled. The range of the filter parameters is optimized.

From Figure 1, the transfer function between input voltage V_{dc} and harmonic current i_f can be obtained as shown in (15). Where ω_f represents the angular switching frequency, K is the ratio of L_i to L_g. Let V_{dc} be 1, draw three-dimensional curves of i_f, K, and C_f under different L_a values as shown in Figure 7. It can be seen that with the increase of the equivalent filter inductor L_a, the attenuation ability of the filter to harmonic current i_f increases gradually.

$$\begin{aligned} G_{i_f\_V_{bus}}(s) &= \frac{i_f}{V_{dc}} = \frac{Z_c}{((Z_g Z_c)+((Z_g+Z_c)\cdot Z_i))} \\ &= \frac{1}{\omega_f(\omega_f{}^2\cdot L_i\cdot L_g\cdot C_f+L_i+L_g)} \\ &= \frac{1}{\omega_f(\omega_f{}^2\cdot L_a{}^2\cdot(\frac{K}{1+K})(\frac{1}{1+K})\cdot C_f+L_a)} \end{aligned} \tag{15}$$

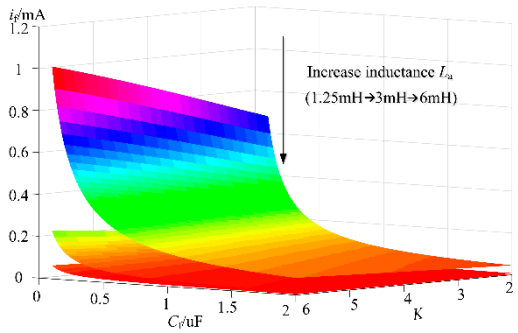


Figure 7. Three-dimensional curves of K, C_f, and i_f under different inductances.

3.2.1. Range Optimization of Inductance Ratio

When L_a is constant, the relationship between i_f and K is shown in Figure 8. When K changes from 0 to 1, the attenuation ability of the filter to harmonic current increases gradually and i_f decreases rapidly. When K = 1, the filter has the strongest attenuation ability to the harmonic current, and i_f is lowest. As K continues to increase, the attenuation ability of the filter to harmonic current decreases, and i_f increases slowly. However, too small K will result in too large L_g and too large an inductance core. Therefore, considering the size and filtering effect of the filter, K usually takes about 3–7.

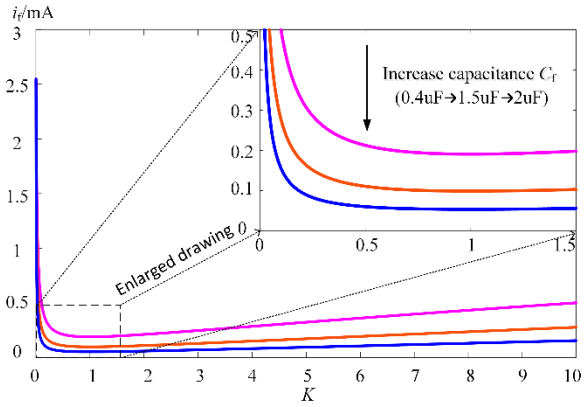


Figure 8. Curve of K and i_f under a certain inductance.

3.2.2. Range Optimization of Capacitance

Similarly, when L_a is constant, the relationship between i_f and C_f is shown in Figure 9. As the value of C_f increases from 0, i_f decreases greatly. When C_f increases to 2.5 uF, the attenuation curve of the filter to the harmonic current tends to be flat. On this basis, $C_{f\text{-}z}$ is defined as the critical filter capacitor to reduce i_f to 20% of the maximum harmonic current. Therefore, in order to make a filter with a high attenuation performance, the value of C_f should be greater than $C_{f\text{-}z}$.

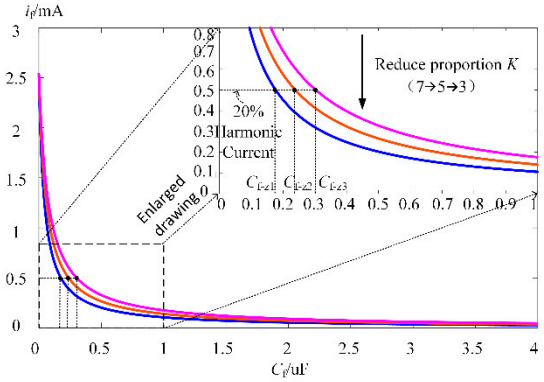


Figure 9. Curve of C_f and i_f under a certain inductance.

3.2.3. Range Optimization of Inductance

According to the above analysis, when K chooses the maximum value and C_f chooses the minimum value, the filter has the weakest ability to suppress harmonic current. Under this limit condition, the relationship between i_f and L_a is plotted as shown in Figure 10. With the increase of L_a, the suppression ability of the filter to the harmonic current is gradually enhanced. On this basis, L_Z is defined as the critical filter inductance to reduce i_f to 5% of the maximum harmonic current. When L_a reaches L_z, the filter has a strong suppression ability to the harmonic current and the suppression curve tends to be flat. Therefore, in order to reduce the volume and cost of the converter, the critical inductance L_z can be used as the maximum value of L_a.

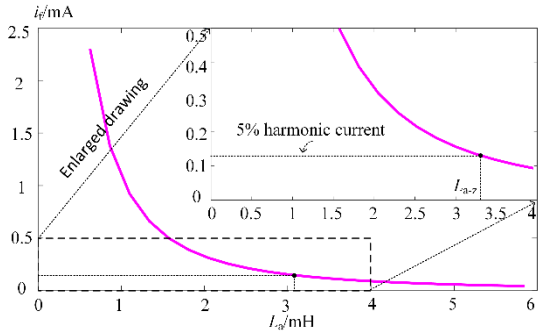


Figure 10. Curve of L_a and i_f under certain parameters.

3.3. Stability Analysis

In order to make the system run stably, the stability of the two states was analyzed. According to the stability condition, the filter parameters are further optimized.

3.3.1. Stability in the Inverter State

The filter of the converter is a third-order system in the inverter state and it is easy to lose stability during operation. To realize the smooth operation of the system, the resonant frequency f_{res} of the third-order filter should be between 1/6 and 1/3 of the switching frequency [23–25]. In this paper, the switching frequency is 50 kHz, so the resonant frequency of the filter ranges from 8.3 kHz to 16.6 kHz. The resonant frequency of the converter in the inverter state can be obtained by (16).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{L_i L_g C_f}} = \frac{1}{2\pi}\sqrt{\frac{(1+K)^2}{K \cdot L_a \cdot C_f}} \tag{16}$$

From the analysis of (16), it can be seen that f_{res} is inversely proportional to L_a, as f_{res} decreases with the increase of L_a. Therefore, by substituting the obtained limit value of L_a into (16), the three-dimensional surface of K, C_f, and f_{res} is obtained as shown in Figure 11. Surface 1 is the surface obtained by substituting the minimum value of L_a, and surface 2 is the surface obtained by substituting the maximum value of L_a. Plane 3 is a horizontal plane with a resonant frequency of 16.6 kHz. Plane 4 is a horizontal plane with a resonant frequency of 8.5 kHz.

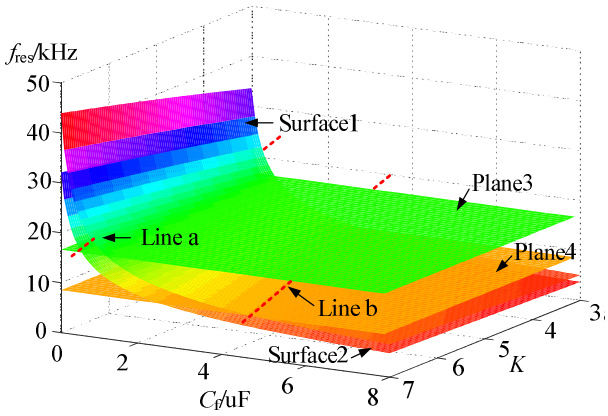


Figure 11. Three-dimensional surfaces of K, C_f, and f_{res} under different inductances.

As can be seen in Figure 11, when L_a is the maximum value, the minimum value of C_f satisfying the resonant frequency requirement can be obtained. Similarly, when L_a is the minimum value, the maximum value of C_f satisfying the resonant frequency requirement can be obtained.

Therefore, the intersection line a of surface 2 and plane 3 and the intersection line b of surface 1 and plane 4 in Figure 11 can be projected on the X-Y plane to obtain Figure 12. From Figure 12, the maximum value of C_f is at point A, which corresponds to a value of 5.1 uF. The minimum value of C_f is at point B, which corresponds to a value of 0.4 uF. A smaller range of C_f can be obtained as shown in (17).

$$0.4\,\text{uF} \le C_f \le 5.1\,\text{uF} \tag{17}$$

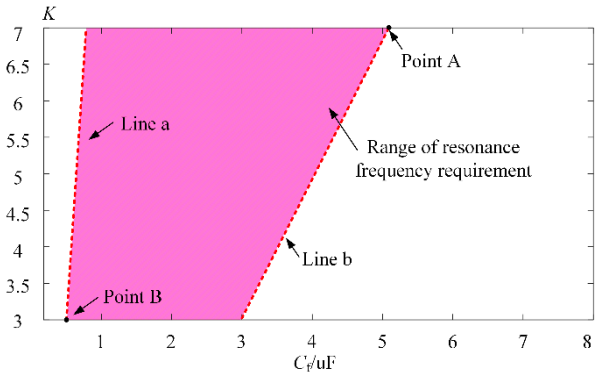


Figure 12. X-Y coordinate projection.

Similarly, from Figure 12, it can be seen that K can meet the requirements of resonant frequency f_{res} in the range of 3–7, so the range of K is still 3–7.

3.3.2. Stability in the Rectifier State

The filter of the converter is a second-order system in the rectifier state. The transfer function between the output voltage U_o and the input voltage U_{in} is shown in (18). In order to ensure the stability of the system, the damping ratio ξ of the second-order filter should be between 0 and 1, so that the system can work in an under-damped state.

$$\mathrm{G(s)} = \frac{U_o(s)}{U_{in}(s)} = \frac{1}{L_b C_o s^2 + \frac{L_b}{R} s + 1} \tag{18}$$

where ξ can be expressed as (19). R is the 10% overload value of the converter in the rectifier state.

$$\xi = \sqrt{L_b C_o}/(2RC_o) \tag{19}$$

The C_{o_min} of (14) is substituted into (19), and the maximum value of L_b can be obtained according to the range value of ξ.

3.4. Performance Index

In order for the converter to have better performance, power density, filtering performance, and stability are taken as optimization targets. The relationship between filter parameters and performance indexes in the two states is analyzed. The results show that the relationships among the performance indexes are constrained by each other. Therefore, priority setting is adopted to take into account multiple optimization targets.

3.4.1. Power Density Performance Index

According to the topology of the converter in Figure 1, the total inductance L_{all} of the converter is defined as the sum of all inductance values, which can be obtained by (20).

$$\begin{cases} L_{\text{all}} = 4L_{\text{i}} + L_{\text{g}} \\ L_{\text{i}} = L_{\text{i1}} = L_{\text{i2}} = L_{\text{i3}} = L_{\text{i4}} \end{cases} \tag{20}$$

In the inverter state, the equivalent filter inductor L_{a}:

$$L_{\text{a}} = L_{\text{i}} + L_{\text{g}}. \tag{21}$$

Substitute (21) into (20) to obtain:

$$\frac{L_{\text{all}}}{L_{\text{a}}} = \frac{4K+1}{K+1}. \tag{22}$$

In the rectifier state, the equivalent filter inductor L_{b}:

$$L_{\text{b}} = 1.5L_{\text{i}} + L_{\text{g}}. \tag{23}$$

Substitute (23) into (20) to obtain:

$$\frac{L_{\text{all}}}{L_{\text{b}}} = \frac{6K+1}{1.5K+1}. \tag{24}$$

Combining equations (22) and (24), L_{all} is proportional to K in both states. Therefore, to get the minimum inductance value, K should choose the minimum value to achieve the high power density performance.

3.4.2. Filtering Performance Index

In the inverter state, the filtering performance is expressed by γ, which is the ratio of the post-filter harmonic current $i_{\text{h\_o}}$ to the pre-filter harmonic current $i_{\text{h\_i}}$. Using the two-port principle, γ can be obtained as:

$$\gamma = \frac{i_{\text{h\_o}}}{i_{\text{h\_i}}} = \frac{Z_{21}}{Z_{22}} = \frac{Z_2}{Z_2 + Z_3} = \frac{1}{1 + w_{\text{f}}{}^2 \cdot C_{\text{f}} \cdot L_{\text{g}}}. \tag{25}$$

Formula (25) shows that the attenuation γ of the filter is inversely proportional to C_{f} and L_{g}. Therefore, to achieve the best filtering effect and minimum attenuation γ, C_{f}, and L_{g} should be maximized. Where the value of L_{g} is determined by L_{a} and K, L_{g} can be obtained by (26).

$$L_{\text{g}} = L_{\text{a}} \cdot \frac{1}{1+K} \tag{26}$$

According to (26), L_{g} is proportional to L_{a} and inversely proportional to K. That is to say that the filtering performance index is proportional to L_{a} and inversely proportional to K.

In the rectifier state, the filtering performance is expressed by h, which is the ratio of the post-filter harmonic voltage $u_{\text{h\_o}}$ to the pre-filter harmonic voltage $u_{\text{h\_i}}$. Using the circuit principle, h can be obtained as (27), where ω_{h} represents the harmonic voltage angle frequency.

$$h = \frac{u_{\text{h\_o}}}{u_{\text{h\_i}}} = \frac{1}{L_{\text{b}} C_{\text{o}} \omega_{\text{h}}{}^2 + \frac{\omega_{\text{h}} L_{\text{b}}}{R} + 1} \tag{27}$$

Formula (27) shows that the harmonic voltage ratio h is inversely proportional to C_{o} and L_{b}. Therefore, to achieve the best filtering effect and the minimum harmonic voltage ratio h, C_{o}, and L_{b} should be maximized.

3.4.3. Stability Performance Index

In the inverter state, to ensure the stable operation of the system, the resonant frequency of the filter should be between $1/6f_{\text{s}}$ and $1/3f_{\text{s}}$. However, the value of the filter inductance will decrease

with the increase of power, which will easily cause resonance frequency offset and affect the stability. Therefore, considering the variation of the filter inductance, the resonant frequency can be obtained from (28), where α represents the ratio of the changed inductance to the initial inductance, which is always less than 1.

$$f_{\text{res}} = \frac{1}{2\pi}\sqrt{\frac{\alpha L_{\text{i}} + \alpha L_{\text{g}}}{\alpha L_{\text{i}} \cdot \alpha L_{\text{g}} \cdot C_{\text{f}}}} = \frac{1}{2\pi}\sqrt{\frac{(1+K)^2}{K \cdot \alpha L_{\text{a}} \cdot C_{\text{f}}}} \tag{28}$$

As can be seen from (28), f_{res} is inversely proportional to L_{a} and C_{f}, and directly proportional to K.

In the rectifier state, to ensure the stable operation of the system, the damping ratio ξ should be between 0 and 1. Similarly, the value of the filter inductance varies with the increase of power. Therefore, considering the variation of the filter inductance, the damping ratio can be obtained by (29).

$$\xi = \sqrt{\alpha L_{\text{b}} C_{\text{o}}}/(2RC_{\text{o}}) = \sqrt{\alpha} \cdot \sqrt{L_{\text{b}} C_{\text{o}}}/(2RC_{\text{o}}) \tag{29}$$

By substituting the obtained range of filter parameters into (29), it can be seen that the damping ξ ratio is less than 1. Therefore, the parameters in this range can satisfy the stability of the system. Therefore, the stability under the rectifier state is not discussed in the later analysis.

3.4.4. Performance Index Priority

According to the previous analysis, the relationship between filter parameters and performance indexes can be known. Among them, the total inductance of the filter is proportional to L_{a}, L_{b}, and K. The filtering performance is proportional to C_{f}, C_{o}, L_{a}, and L_{b}, and is inversely proportional to K. The stability of the filter (i.e., the resonant frequency of the filter) is inversely proportional to L_{a} and C_{f}, and is proportional to K. The specific relationship is shown in Table 1 below.

Table 1. The relationship between the performance index and filter parameter.

Performance Index	Inductance ($L_{\text{a}}/L_{\text{b}}$)	Capacitance ($C_{\text{f}}/C_{\text{o}}$)	Inductance Ratio K
Power Density	Inverse proportion	\	Inverse proportion
Filtering	Proportion	Proportion	Inverse proportion
Stability	Inverse proportion	Inverse proportion	Proportion

As can be seen in Table 1, we can see that the relationship between the three performance indexes and the filter parameters is contradictory. Therefore, the three performance indexes cannot be optimized at the same time. To solve this problem, priority setting is adopted to take into account multiple optimization targets. The specific methods are as follows: (1) The power density index is taken as the first priority, and the minimum total inductance is taken as the target. The values of the equivalent filter inductor L_{a}, L_{b}, and inductance ratio K are obtained. (2) Taking the filtering performance index as the second priority, the preset attenuation γ is less than 0.08 and harmonic voltage ratio h is less than 0.1. The value of filter capacitance C_{f} and C_{o} are obtained. (3) The stability index is used as the verification condition to judge whether the obtained filter parameters are reasonable or not. If not, the value of L_{a} can be adjusted by 0.05 mH step size, and the adjusted L_{a} value can be recalculated into the filter performance index to obtain new parameter values until the parameters are reasonable. The filter parameters are optimized through the above steps, and the flow chart of the parameter design is shown in Figure 13. The specific filter parameters are obtained as shown in Table 2. So far, the parameter design process of the filter is completed.

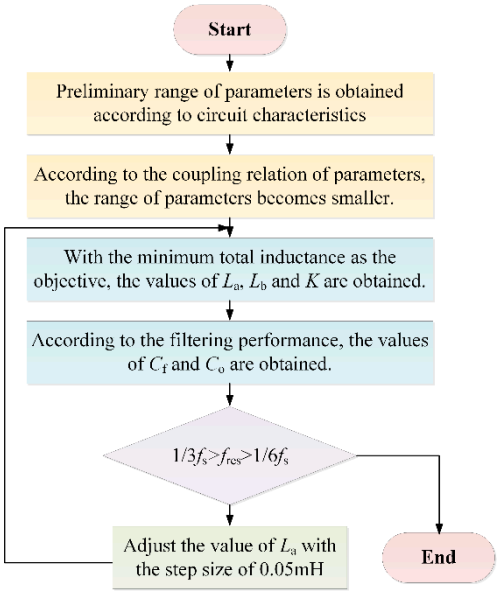


Figure 13. Flow chart of the parameter design.

Table 2. List of the main filter parameters.

Components	Values
Filter inductance L_i	0.5 mH
Filter inductance L_g	0.167 mH
Filter capacitor C_f	0.75 uF (WIMA film capacitor)
Filter capacitor C_o	880 uF(Rubycon)
Rated power	5 kW
DC voltage	400 V
AC voltage	220 V(Valid value)
Switching frequency	50 kHz
DSP	TMS320F28377D (Texas Instruments)
Power switches S_1-S_6	CREE C3M0016120K
Diodes D_1-D_4	CREE C3D30065D

4. Experimental Result

In order to verify the validity of the parameter design method for the proposed converter, a prototype with a rated power of 5 kW was built, as shown in Figure 14, with a power density that reached 36 W/in^3. The processor chip used was 28377D (Texas Instruments, Dallas, TX, USA), and the experiments were carried out under two states of inverter and rectifier, respectively.

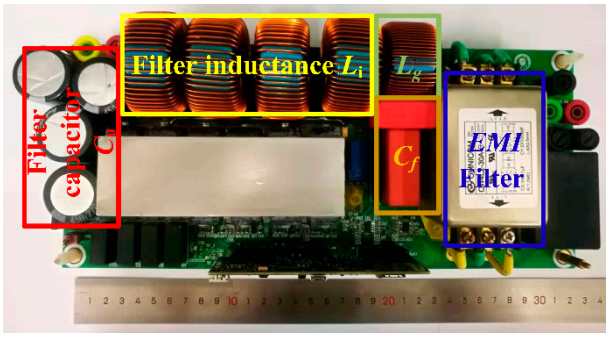


Figure 14. Photograph of the experimental prototype.

Figure 15 shows the experimental waveforms of the converter under full load in the grid-connected inverter state. Where V_{dc} denotes DC voltage, V_g denotes grid voltage, and i_g denotes grid current. In the figure, the phases of i_g and V_g are the same, and the waveform i_g has good sinusoidal degree and small distortion. Further, when the number of harmonics is calculated to be 15 times, the THD of i_g is only about 2.7%.

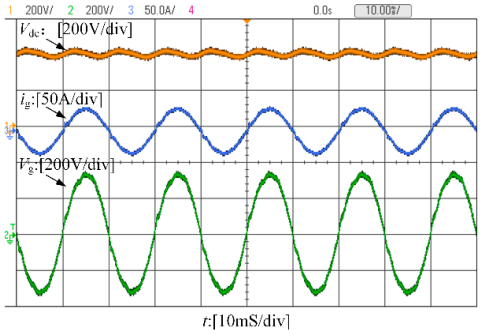


Figure 15. Full-load experimental waveform of the grid-connected inverter.

Figure 16 shows the experimental waveforms of the converter under full load in the off-grid inverter state. Where i_{go} denotes output current, V_{go} denotes output voltage. In the figure, the waveforms i_{go}, V_{go} have good sinusoidal degree and small distortion. Further, when the number of harmonics is calculated to be 15 times, the THD of i_g is only about 1.2%.

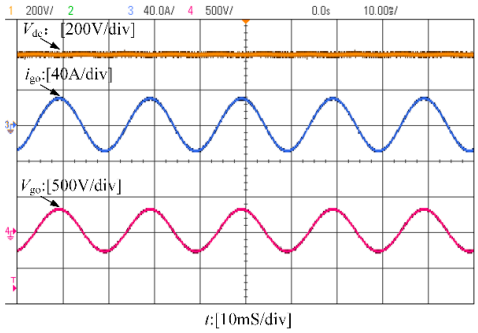


Figure 16. Full-load experimental waveform of the off-connected inverter.

Figure 17 shows the experimental waveforms of the converter under full load in the rectifier state. In the figure, the phase of i_g and V_g is the same. The fluctuation of the DC bus voltage is less than 15% of the rated voltage of 400 V, which meets the design requirements. Further, when the number of harmonics is calculated to be 15 times, the THD of i_g is 4.5%.

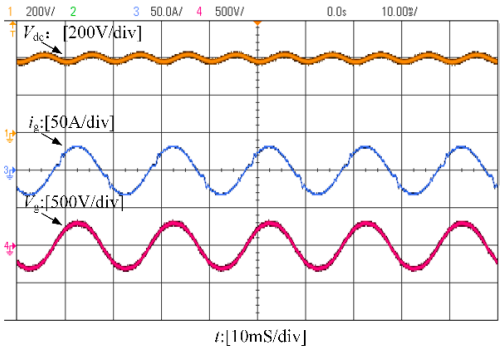


Figure 17. Full-load experimental waveform of the rectifier.

Figure 18 shows the dynamic experimental waveforms of the converter under the inverter grid-connected state. In the figure, the dynamic recovery time of the converter is shorter and the converter has better stability.

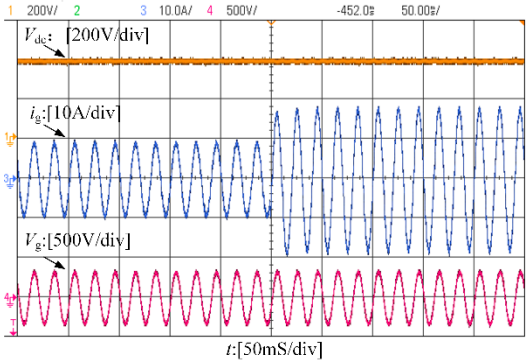


Figure 18. Dynamic experimental waveform of the grid-connected inverter.

Figure 19 shows the dynamic experimental waveforms of the converter in the rectifier state. In the figure, it can be seen that the change of the V_{dc} before and after the power dynamic conversion is small and the dynamic recovery time of the converter is shorter. The results show that the converter has high stability.

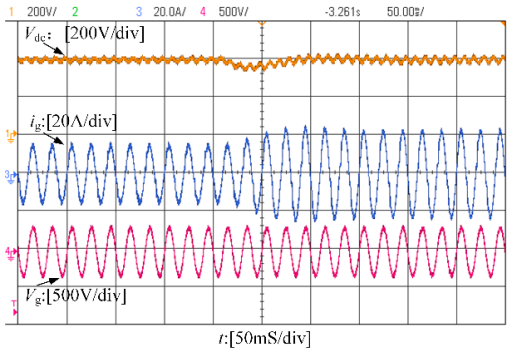


Figure 19. Dynamic experimental waveform of the rectifier.

In summary, the efficiency curves in the two states are shown in Figure 20. From the figure, the maximum efficiencies of the grid-connected inverter and rectifier are 98.8% and 98.66%, respectively. The efficiencies of the grid-connected inverter and rectifier under full load are 98.2% and 98.1%, respectively.

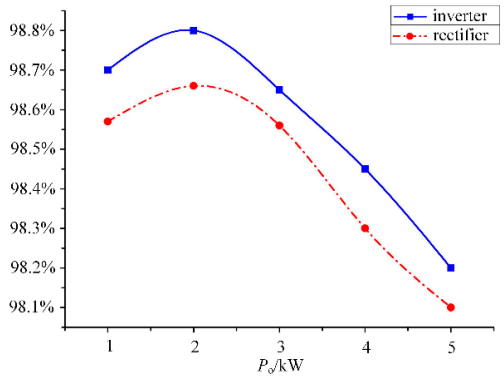


Figure 20. Operating efficiency of the converter.

5. Conclusions

This paper proposes an interleaved, dual-buck, bidirectional, grid-connected converter topology and related filter parameters optimization design method. This method has several optimization design goals, including filter inductance, filtering performance, and system stability. For one thing, the performance requirements of the filter in the inverter and rectifier states are simultaneously considered. For another, the total inductance of the converter is small enough and the steady-state performance is good. The specific design process is as follows: (1) The coupling relationship between circuit performance and filter parameters is considered, and the parameter range of the filter is continuously reduced. (2) Set the performance priority of the filter and optimize the reasonable value of the filter parameters. Thereby, beneficial properties such as higher power density, better filtering effect, and higher steady-state stability are obtained. Finally, a 5 kW experimental prototype was used to prove the validity of the theoretical analysis. Its power density was 36 W/in^3. Under full load conditions, the THDs of grid currents in among grid-connected inverter, off-connected inverter, and rectifier states are 2.7%, 1.2%, and 4.5%, respectively with 0.5 mH buck inductance. The maximum efficiencies of the converter are 98.8% and 98.66% in the grid-connected inverter state and the rectifier state, respectively.

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Conflicts of Interest: The authors declare no conflict of interest.

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