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Active Power Decoupling Design of a Single-Phase AC–DC Converter

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Abstract: The second-order ripple power of single-phase converter causes second-order ripple voltages on the DC bus. For eliminating second-order ripple components, passive power decoupling methods including DC bus electrolytic capacitors have some shortcomings, such as low power density and poor stability of converters. Thus, an active power decoupling method based on a single-phase converter is proposed in this paper. The control method, taking single-phase voltage source pulse width modulation (PWM) rectifier (single-phase VSR) as the basic converter and adopting a buck-boost power decoupling circuit, introduces second-order ripple of DC bus voltage into a power decoupling circuit. The ripple acts as compensation of the phase deviation between the command value and the actual value of the second-order ripple current. Therefore, estimation of the second-order ripple current is more accurate, the power decoupling circuit absorbs the second-order ripple power behind the H-bridge more completely, and the DC bus voltage ripple is effectively suppressed accordingly. Finally, experimental results of the single-phase VSR are given to verify the validity of the proposed method.

Keywords: single-phase converter; active power decoupling; second-order ripple reduction; DC bus voltage

1. Introduction

Single-phase voltage source pulse width modulation (PWM) converters are widely used in uninterruptible power supply, locomotive traction, DC microgrids, and renewable energy systems because of its high efficiency and reliability [1–5]. However, the unbalance of instantaneous active power between DC and AC sides of the single-phase converter puts inevitable second-order components of the voltage and power on the DC bus, which endangers the operation of equipment and system [6,7]. In order to reduce the fluctuation of voltage and power on the DC side, the most common way is to install passive power decoupling systems on the DC side, such as large capacitors or LC filters. LC filter refers to a resonant branch consisting of an inductor and a capacitor in series. A reasonable parameter design will make the resonant frequency of this branch twice the power frequency. As a result, the second-order ripple power is completely transferred to the LC filter. Nevertheless, passive power decoupling systems always need large capacitors, especially in high-voltage and high-power situations. In addition, for the specific systems pursuing a high power density or lighter weight, small capacitors are preferable. Another factor is the limited lifetime of large electrolytic capacitors, which leads to reliability problems and increases maintenance costs [8–10]. To solve the above problems, some scholars put forward the active power decoupling method [11–16]. Active power decoupling circuits include switches and storage systems. By controlling the on/off states of switches, the conversion between the second-order ripple energy of the DC bus and the energy of storage element in the power decoupling circuit is realized. This method greatly reduces system volume and prolongs the service life of the system.

In recent years, research on active power decoupling has emerged [17–19], which can be divided into dependent power decoupling circuits (DPDCs) [20–26] and independent power decoupling circuits (IPDCs) [27–33]. DPDCs ordinarily multiplex the power switches with the H-bridge arm of the converter. In [20], a buck-type DPDC is analyzed in detail, and the corresponding direct power decoupling method and automatic power decoupling method are proposed. Like other DPDCs, the applied decoupling circuit in [20] reduced the cost and volume of the system. However, due to the coupling between the control of the decoupling circuit and the H-bridge arm, this method becomes more complex. In contrast, IPDCs are more flexible to control. IPDCs refer to the topologies in which operation of the power decoupling circuits is independent of the single-phase converters. The circuits in [27–33] met this requirement. In [30,31], a boost-type IPDC is considered. The proposed estimation method of second-order ripple current ignores the probable phase deviation of AC input voltage and input current, which results in incomplete absorption of second-order ripple power. Authors in [32] consider the deviation, but estimation of the second-order ripple current of the DC side derives from the output of the converter controller; thus, control of the decoupling circuit and the converter loop is coupled. In order to obtain second-order ripple currents accurately, the pulsating current after flowing through the H-bridge is directly sampled by the authors in [33]. As a result, this method places high demands on the switching frequency and accuracy of sampling.

Considering the complexity of DPDC and the imprecision of estimation, a control strategy based on an IPDC buck-boost-type power decoupling circuit is proposed in this paper. The second-order ripple of DC bus voltage is introduced to control the decoupling inductor current. The advantage of this control method is that the phase deviations of H-bridge voltage and AC current are considered. Thus, the estimation is more accurate, and the second-order ripple of the DC bus voltage and power is effectively suppressed accordingly. The selected buck-boost-type power decoupling topology allows the voltage across the decoupling capacitor to vary depending on the output voltage range of the rectifier; the decoupling capacitance can, therefore, be flexibly changed. Authors in [33] select the same power decoupling topology. However, the decoupling loop works in continuous current mode (CCM) in this paper, while paper [33], which applied the same buck-boost-type power decoupling circuit, works in (discontinuous current mode) DCM. Control in CCM reduces the current stress of power switches. In addition, the second-order ripple current is obtained by estimation rather than sampling, as in paper [33], which avoids the difficulty of high-frequency sampling. Moreover, the closed-loop regulation can eliminate steady-state error in real time, which has a strong anti-interference ability and good dynamic characteristics. This avoids the neglect of parasitic parameters and external interference in an open-loop control circuit [33]. To simplify the experiment, the single-phase voltage source PWM rectifier (single-phase VSR) is analyzed in this paper. Though, the proposed method is also applicable to single-phase voltage source PWM inverters with front stages, such as (Photovoltaic) PV inverters.

The power distribution of the rectifier is analyzed firstly. Secondly, the characteristics of the buck-boost-type power decoupling circuit and the other two decoupling circuits are compared. The control strategy of power decoupling circuit is further introduced in the third part. Then, the parameter design of power decoupling circuit is given in CCM. Finally, the correctness of the control method is verified by simulation and experimentation.

2. Power Analysis of a Single-Phase Rectifier

Figure 1 shows the typical topology of single-phase VSR. Part I and II are the H-bridge circuit and power decoupling loop, respectively. i_{r} represents the second-order harmonic current of the line behind the H-bridge. i_{rr} is the input second-order ripple current of the power decoupling loop. The remaining second-order ripple current of the DC bus is represented by i_{rc}.

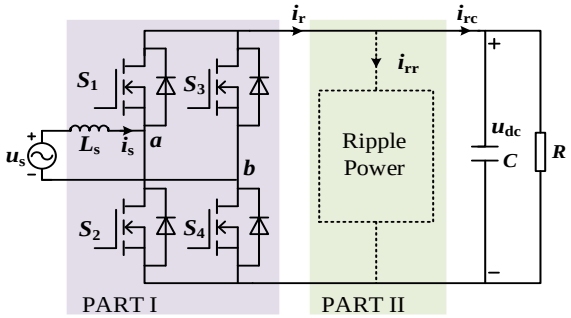


Figure 1. Topology of single-phase VSR with a power decoupling circuit.

When the rectifier is operating at unit power factor, the AC input current i_s and the voltage u_s are kept in phase. In fact, a precise unit power factor is difficult to achieve; thus, there will be a small phase difference between i_s and u_s. In this case, the two can be expressed as follows:

$$u_s = U_s \sin \omega t; \tag{1}$$

$$i_s = I_s \sin(\omega t - \beta); \tag{2}$$

where U_s and I_s represent the amplitude of the input voltage and the input current, respectively. ω is the angular frequency of the grid voltage, and β is the phase of u_s leading i_s. From Equations (1) and (2), the input power P_{in} is:

$$P_{in} = u_s i_s = \frac{U_s I_s}{2} \cos \beta - \frac{U_s I_s}{2} \cos(2\omega t - \beta). \tag{3}$$

According to Equation (2), the voltage drop u_L on the inductor L_s is:

$$u_L = L_s \frac{di_s}{dt} = \omega L_s I_s \cos(\omega t - \beta). \tag{4}$$

From Equations (3) and (4), the power P_{tr} transmitted to the DC bus can be expressed as:

$$\begin{aligned} P_{tr} &= u_s i_s - u_L i_s \\ &= \tfrac{U_s I_s}{2} \cos \beta - \left(\tfrac{U_s I_s}{2} \cos(2\omega t - \beta) + \tfrac{\omega L I_s^2}{2} \sin(2\omega t - 2\beta) \right) \end{aligned} \tag{5}$$

Equation (5) shows that P_{tr} consists of two parts: constant power P_o and second-order ripple power P_r, which are expressed, respectively, as follows:

$$P_o = \frac{U_s I_s}{2} \cos \beta; \tag{6}$$

$$P_r = -\left(\frac{U_s I_s}{2} \cos(2\omega t - \beta) + \frac{\omega L I_s^2}{2} \sin(2\omega t - 2\beta) \right). \tag{7}$$

P_0 is the output power of the rectifier. P_r is the second-order ripple power (i.e., the power to be processed in part II), which can be further expressed as follows:

$$\begin{aligned} P_r &= \sqrt{\tfrac{U_s^2 I_s^2}{4} \cos^2 \beta + \left(\tfrac{\omega L I_s^2}{2} - \tfrac{U_s I_s}{2} \sin \beta \right)^2} \\ &\quad \times \sin(2\omega t - 2\beta + \psi) \end{aligned} \tag{8}$$

$$\psi = \arctan \frac{(U_s I_s / 2) \cos \beta}{\left(\omega L I_s^2 / 2 \right) - (U_s I_s / 2) \sin \beta}. \tag{9}$$

The above deduction shows that the phase angles β and ψ cannot be measured directly, which is not beneficial for controlling the power decoupling loop by the expression. To this end, the two phase angles are combined to establish a reference coordinate system with i_s as 0 phase, as shown in Figure 2. At this time, the calculation of the power P_{tr} transmitted to the DC bus is as follows:

$$P_{tr} = u_{ab} i_s = \frac{U_{ab} I_s}{2} \cos\varphi - \frac{U_{ab} I_s}{2} \cos(2\omega t - \varphi). \tag{10}$$

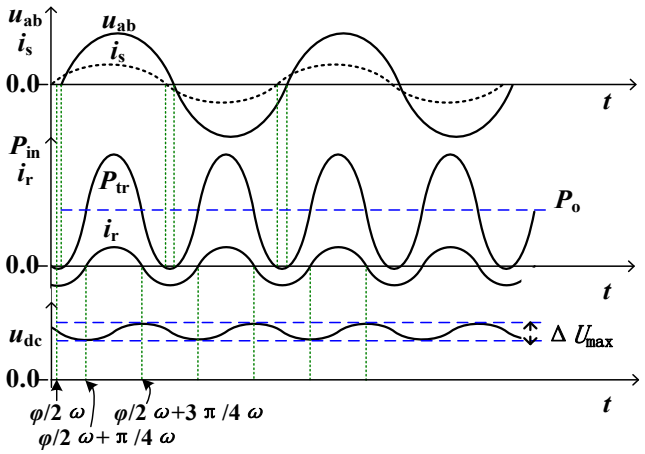


Figure 2. Waveforms of different variables in the system.

In Equation (10), u_{ab} is the voltage of the ab bridge arm. φ is the phase of i_s ahead of u_{ab}. If the power decoupling circuit is not added, the second-order ripple power in the circuit is completely absorbed by the DC bus capacitors. As shown in Figure 2, the energy ΔE of the bus capacitor C filled in the period from $\varphi/2\omega$ to t is as follows:

$$\Delta E = \int_{\varphi/2\omega}^{t} -\frac{U_{ab} I_s}{2} \cos(2\omega t - \varphi) dt = -\frac{U_{ab} I_s}{4\omega} \sin(2\omega t - \varphi). \tag{11}$$

At the same time, the energy change of capacitor in this period ΔE_c is as follows:

$$\Delta E_c = \frac{1}{2} C u_{dc}^2 - \frac{1}{2} C U_{dc}^2, \tag{12}$$

where u_{dc} is the DC bus voltage and U_{dc} is its DC component. Ignoring the power loss in the circuit, Equations (11) and (12) should be equal; thus, the DC bus voltage is as follows:

$$u_{dc} = \sqrt{U_{dc}^2 - \frac{U_{ab} I_s}{2\omega C} \sin(2\omega t - \varphi)}. \tag{13}$$

Applying Taylor's formula to Equation (13), the results are approximately as follows:

$$u_{dc} \approx U_{dc} - \frac{U_{ab} I_s}{4\omega C U_{dc}} \sin(2\omega t - \varphi). \tag{14}$$

From Equation (14), there is a second-order component in DC bus voltage. Refer to Equation (11) to calculate the capacitance C during $\varphi/2\omega + \pi/4\omega$ to $\varphi/2\omega + 3\pi/4\omega$ period:

$$C = \frac{U_{ab} I_s}{2\omega \Delta U_{max} U_{dc}}. \tag{15}$$

In Equation (15), ΔU_{max} is the maximum value of the DC bus voltage ripple. Considering the reliability of the power supply and normal operation of the equipment, the DC bus voltage ripple should be within the prescribed range, generally not more than 10%. If C is selected by Equation (15), a capacitor with larger capacitance value is needed to suppress the second-order ripple effectively. As a result, the buck-boost-type active power decoupling circuit is selected to absorb the second-order harmonic power on the DC side.

3. Analysis of an Active Power Decoupling Circuit

In this paper, a buck-boost-type power decoupling circuit is adopted [33]. Similarly, bidirectional buck-boost circuits can be used for power decoupling, such as the decoupling circuits in reference [27,32]. The characteristics of the three circuits are compared in Table 1, where d is the duty cycle of the bidirectional decoupling circuit. As shown in the table, the voltage stress and current stress of the buck-boost-type decoupling topology are not dominant. However, the choice of decoupling capacitance and capacitor voltage is more flexible, which will bring broad application prospects. Assuming that the second-order ripple power is constant, if the DC bus voltage is high, in order to avoid excessive voltage stress on the power device, a decoupling capacitor voltage lower than the DC bus voltage can be selected. From Equation (14), the ripple of the capacitor voltage is large at this time. In addition, if the voltage across the decoupling capacitor is high, the capacitance can be selected to be very small, thereby achieving an increase in power density. As a result, a buck-boost-type power decoupling circuit was selected in this paper.

Table 1. Comparison of three circuits.

Parameters	Buck Type	Boost Type	Buck-Boost Type
Voltage u_z of decoupling capacitor	$<u_{dc}$	$>u_{dc}$	adjustable
Decoupling capacitance C_z	relatively large	relatively small	adjustable
Voltage stress	u_{dc}	u_z	$u_{dc+}u_z$
Current stress	i_r/d	i_r	i_r/d
efficiency	—	higher	—

The buck-boost-type power decoupling topology is shown in Figure 3a, in which capacitance acts as the energy storage element, while inductance acts as the energy transmission element. When the instantaneous power of the AC side is larger than that of DC side, that is, when the power decoupling circuit is in the charging mode (hereinafter referred to as charging mode), the switching modes of CCM are shown in Figure 3b. i_r denotes the second-order ripple current processed in each switching cycle, i_L denotes the instantaneous value of the inductor current in the decoupling loop, and v_{Q1} represents the voltage stress sustained by Q_1. During t_0–t_1 period, Q_1 is on, and the pulsating power is transferred to the inductor. During the period from t_1 to t_2, Q_1 is off, and the pulsating power flows through diode D_2 to transfer energy to the capacitor.

Similarly, when the instantaneous power of the AC side is less than that of DC side, that is, when the power decoupling circuit is in discharging mode (hereinafter referred to as discharging mode), Q_2 is on, and the pulsating power is transferred to the inductor. When Q_2 is turned off, the pulsating power flows through the diode D_1, and the energy is transmitted to the DC side.

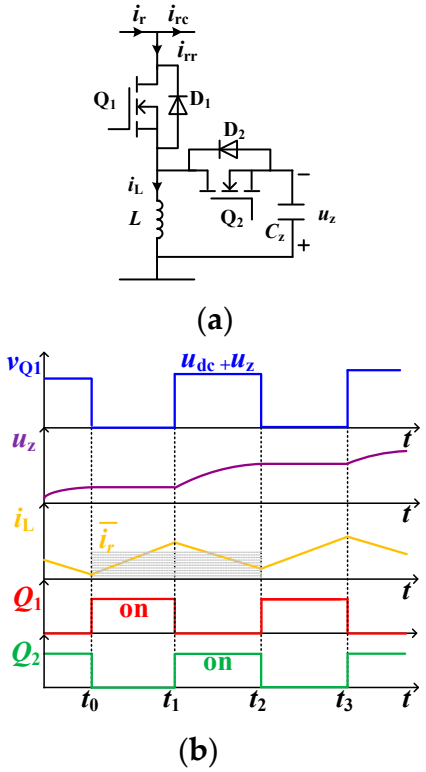


Figure 3. The buck-boost-type power decoupling circuit and the modal diagram in continuous current mode (CCM): (**a**) the buck-boost-type power decoupling topology; (**b**) the modal diagram in CCM.

4. Control System Design

In order to eliminate the second-order ripple power on the DC bus, the precondition is to accurately obtain i_r in Figure 1. If i_{rr} is controlled to equal i_r, the DC bus voltage will be constant. Generally, there are two methods to obtain the second-order ripple current [32,33]. The first method is to sample i_r directly and get its second-order component through the second-order resonant controller [33]. However, since the change of zero and nonzero values of pulsating current are consistent with the switching frequency, a higher sampling frequency is required. Only in this case can the signal be undistorted. It greatly increases the difficulty of the system's hardware design. As a result, this paper selected the second method, which is to estimate i_r by other variables in the circuit.

Ideally, the second-order ripple energy needs to be fully absorbed by the power decoupling circuit. According to Equation (10), the output power P_{tro} is as follows:

$$P_{tro} = \frac{U_{ab}I_s}{2}\cos\varphi = U_{dc}I_{dc}, \tag{16}$$

where I_{dc} is the DC component of the load current on the DC side. The second-order harmonic power P_{trr} is:

$$P_{trr} = -\frac{U_{ab}I_s}{2}\cos(2\omega t - \varphi) = U_{dc}i_r. \tag{17}$$

Combining Equations (16) and (17), i_r is obtained as follows:

$$i_r = -\frac{I_{dc}}{\cos\varphi}\cos(2\omega t - \varphi). \tag{18}$$

From Figure 3, the second-order ripple current i_L on the inductor of the decoupling circuit is:

$$i_L = \frac{1}{d}i_r, \tag{19}$$

where d is the duty cycle of Q_1 in the buck-boost circuit. According to the control method in [30,31], the command value i_{Lc} is set to:

$$i_{\mathrm{Lc}} = -\frac{I_{\mathrm{dc}}}{d}\cos(2\omega t + \beta). \tag{20}$$

The duty cycle d in Equation (20) is calculated by the DC component of DC bus voltage u_{dc} and decoupling capacitor voltage u_z. Figure 4 shows the control block diagram of the power decoupling circuit. From Equation (20), part 1 in Figure 4 can be obtained. This command value is only an approximation of i_{r}. Since the phase difference φ is ignored, there is a deviation between the command value i_{Lc} and the actual value i_{L}. To this end, this paper introduced DC bus voltage u_{dc} to participate in the estimation of i_{r}.

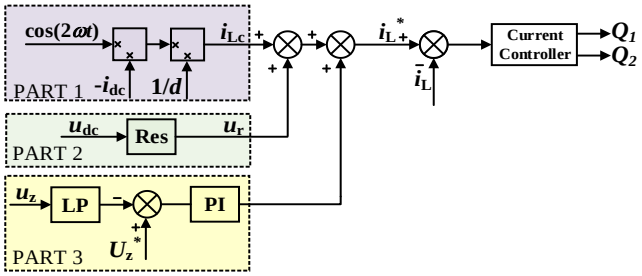


Figure 4. Control block diagram of the power decoupling circuit.

The function of DC bus voltage in the power decoupling circuit is shown in part 2 in Figure 4. Res represents the second-order resonant controller, which extracts the second-order component of u_{dc} (i.e., u_{r}). Because most of the second-order ripple energy in the circuit is absorbed by the power decoupling circuit, according to Equation (14), the second-order ripple component of the DC bus voltage can be expressed as:

$$u_r = -E'\sin(2\omega t - \varphi). \tag{21}$$

Referring to Equations (11) and (14), E' represents a value proportional to the second-order ripple energy of the DC bus. It is a constant to characterize u_{r}. Equation (21) is based on the fact that the second-order ripple component of the DC side is completely absorbed by the DC bus capacitor (i.e., the ripple current does not flow through the output). In fact, this condition is only valid when the DC bus capacitance is large enough. However, after the power decoupling circuit is added, the DC bus capacitance decreases, and the second-order ripple component also exists in the load current. At this time, the second-order component of the DC bus voltage should be expressed as:

$$u_r = -E'\sin(2\omega t - \varphi - \theta). \tag{22}$$

Equation (22) shows that the DC bus capacitor is also considered as the load, and θ is the impedance angle of the RC load. Expressing the command values i_{Lc} and u_{r} by phasors gives:

$$i_{\mathrm{Lc}} + u_r = \frac{I_{dc}}{d}\angle(\beta + \pi) + E'\angle(\pi/2 - \varphi - \theta). \tag{23}$$

Equation (23) can be rewritten as:

$$i_{\mathrm{Lc}} + u_{\mathrm{r}} = M\angle Q; \tag{24}$$

$$M = \sqrt{\left(\frac{I_{dc}\cos\beta}{d} - E'\sin(\varphi+\theta)\right)^2 + \left(\frac{E'\cos(\varphi+\theta)}{d} - I_{dc}\sin\beta\right)^2}\ ; \tag{25}$$

$$Q = \pi/2 + \arctan\frac{I_{dc}\cos\beta - dE'\sin(\varphi+\theta)}{dE'\cos(\varphi+\theta) - I_{dc}\sin\beta}. \tag{26}$$

Plotting the phasor form of the above variables in a vector diagram is shown in Figure 5. The figure will present the function of u_{dc} in the control circuit more intuitively. There is a phase difference between the command value i_{Lc} and the actual inductor current i_L. Since the output amplitude of u_r is small, if u_r is superimposed on i_{Lc}, the estimated command value of the second-order current is basically unchanged. Moreover, the superimposed phase approaches the phase of i_r. As a result, the control of the second-order ripple absorption is more accurate.

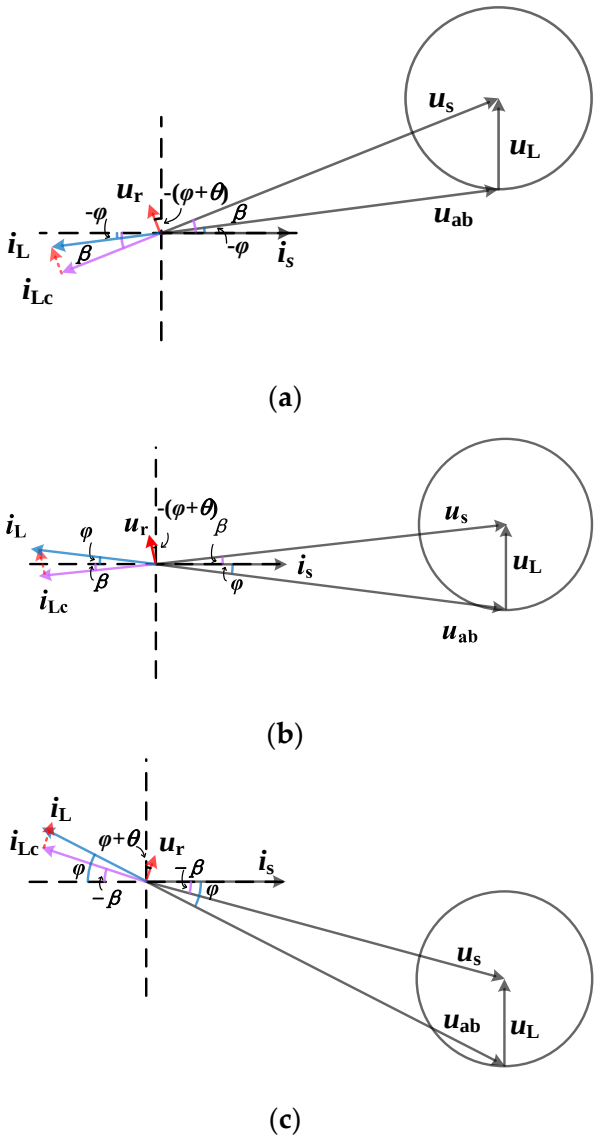


Figure 5. Phasor diagram of different variables in the rectifier: (**a**) Case 1 in quadrant I, the angle between u_L and u_{ab} is acute; (**b**) Case 2 in quadrant I, the angle between u_L and u_{ab} is obtuse; and (**c**) Quadrant II.

At the same time, this method is highly applicable because the phase can be compensated in four quadrants. The phasors in the first and second quadrants are shown in Figure 5. The same applies to the third and fourth quadrants.

Part 3 in Figure 4 shows the control of u_z. LP represents the low-pass filter, which extracts the DC component of u_z. The superposition of part 1, part 2, and part 3 serves as the given value of i_L.

5. Parameter Design

5.1. Inductance Design of the Power Decoupling Circuit

The inductance of the power decoupling circuit was designed in CCM. In charging mode, the following can be seen from Figure 3b:

When Q_1 is on, the inductor charges:

$$K_1 = \frac{u_{\mathrm{dc}}}{L}, \tag{27}$$

where K_1 indicates the rise rate of the inductor current during charging. When Q_1 is off, the inductor discharges:

$$K_2 = -\frac{u_{\mathrm{z}}}{L}, \tag{28}$$

where K_2 represents the drop rate of the inductor current during discharging. In this process, the second-order ripple energy is transferred to the inductor and then to the capacitor.

Ignoring the energy storage on the inductor in a switching period, that is, the second-order ripple energy injected into the inductor is approximately equal to the average value of second-order ripple energy processed by decoupling loop in a switching period:

$$i_{\mathrm{r}} T \approx \frac{1}{2} K_1 T_1^2, \tag{29}$$

where T_1 indicates the time when Q_1 is turned on in one switching cycle, and T represents one switching period. Combining Equations (27) and (28) with (29), the duty cycle d_{c} of Q_1 is:

$$d_{\mathrm{c}} \approx \sqrt{\frac{2 i_{\mathrm{r}} f_{\mathrm{r}} L}{u_{\mathrm{dc}}}}, \tag{30}$$

where f_{r} is the switching frequency of power decoupling circuit, which is equal to the switching frequency of rectifier circuit in this paper. Similarly, in a switching cycle, the second-order ripple energy flowing from the inductor is approximately equal to the average value of second-order ripple energy processed by the decoupling loop. As a result, the duty cycle d_{d} of Q_2 is:

$$d_{\mathrm{d}} \approx \frac{\sqrt{2 i_{\mathrm{r}} f_{\mathrm{r}} L u_{\mathrm{dc}}}}{u_{\mathrm{z}}}. \tag{31}$$

At the peak current of the inductor, the current ripple is the largest. Thus, the peak current value of the inductor is taken to calculate the minimum value of the required inductance. From Equation (20), the peak value i_{Lmax} of the inductor current is approximately as follows:

$$i_{\mathrm{Lmax}} = \frac{I_{\mathrm{dc}}}{d}. \tag{32}$$

Since the current only plays the role of energy transmission, the ripple index is not strictly required; therefore, the ripple is calculated by 1.5 times.

According to the given ripple index, when Q_1 is on or off, L must be met respectively:

$$\frac{\frac{u_{\mathrm{dc}}}{L} d_c T}{2 i_{\mathrm{Lmax}}} \leq 1.5; \tag{33}$$

$$\frac{\frac{u_{\mathrm{z}}}{L} d_{\mathrm{d}} T}{2 i_{\mathrm{Lmax}}} \leq 1.5. \tag{34}$$

The range of L is obtained as follows:

$$L \geq \frac{2u_{\mathrm{dc}}u_{\mathrm{z}}^2}{9I_{\mathrm{dc}}f_{\mathrm{r}}(u_{\mathrm{dc}}+u_{\mathrm{z}})^2} = L_1. \tag{35}$$

Moreover, the peak current ripple value of the inductor should be less than the maximum value I_{p} allowed to flow through the inductor. When the average current value of the inductor reaches i_{Lmax} in a switching cycle, L is calculated as follows:

$$i_{\mathrm{Lmax}} + \frac{U_{\mathrm{dc}}}{2L}d_{\mathrm{c}}T \leq I_{\mathrm{p}}; \tag{36}$$

$$i_{\mathrm{Lmax}} + \frac{U_{\mathrm{z}}}{2L}d_{\mathrm{d}}T \leq I_{\mathrm{p}}. \tag{37}$$

The range of L is obtained as follows:

$$L \geq \frac{u_{\mathrm{dc}}i_{\mathrm{r}}}{2f_{\mathrm{r}}\left(I_{\mathrm{p}}-i_{\mathrm{Lmax}}\right)^2} = L_2. \tag{38}$$

The calculation of inductance selection in discharging mode is the same. By Equations (27)–(38), the selection of inductance should follow:

$$L > (L_1 \cup L_2). \tag{39}$$

That is, the selected inductance L should be greater than the maximum values of L_1 and L_2.

5.2. Capacitance Design of the Power Decoupling Circuit

From Equation (15), the selection of capacitance in the decoupling circuit is related to the average value and the ripple of decoupling capacitor voltage. Therefore, the maximum value of capacitor voltage ripple ΔU_{zmax} is obtained:

$$\Delta U_{\mathrm{zmax}} = \frac{U_{\mathrm{ab}}I_{\mathrm{s}}}{2\omega C_{\mathrm{z}}u_{\mathrm{z}}}, \tag{40}$$

In order to ensure the continuity of capacitor voltage and normal operation of the decoupling circuit, the following conditions should be satisfied:

$$\Delta U_{\mathrm{zmax}} \leq 2u_{\mathrm{z}}. \tag{41}$$

A combination of Equations (40) and (41) can be further expressed as:

$$\frac{U_{\mathrm{dc}}I_{\mathrm{dc}}}{2\omega C_{\mathrm{z}}} \leq u_{\mathrm{z}}^2. \tag{42}$$

The relationship of capacitance, capacitor voltage. and output power is plotted in Figure 6 based on Equation (42). From the figure, if the capacitance C_{z} is larger, the capacitor voltage u_{z} can be made smaller; thus, the voltage stress of the decoupling loop can be reduced. If u_{z} is higher, C_{z} can be reduced accordingly. If the output power increases, C_{z} needs to increase to maintain effective operation.

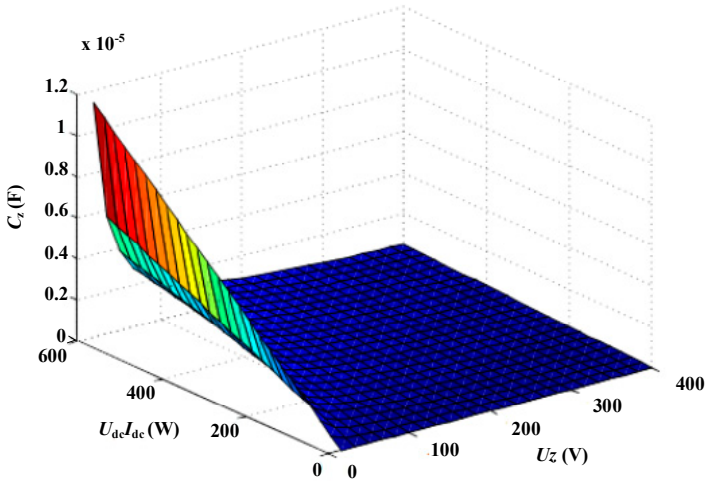


Figure 6. Selection range of capacitance in the power decoupling circuit.

6. Simulation and Experiment

6.1. Simulation Verification

In order to verify the feasibility of the control method, two sets of simulation models were built for comparison. The first group adopted the control method in [30,31]. This method estimated i_r without phase compensation, and the power decoupling circuit was in CCM, which is called the estimation method for short. The second group adopted the control method proposed in this paper. The two sets of control methods were based on the same rectifier and power decoupling topology. Their simulation parameters are shown in Table 2.

Table 2. Simulation and experiment parameters.

Parameters	Values (Estimation Method and the Proposed Method)
Input voltage U_s (Root mean square)	110 V
DC bus rated voltage U_{dc}	200 V
Supply frequency	50 Hz
Switching frequency of rectifier f	10 KHz
Switching frequency of decoupling circuit f_r	10 KHz
AC side inductance L_s	3.3 mH
DC bus capacitor C	100 μF
Rated resistor load R	75 Ω
Inductance of decoupling loop L	1.2 mH
Capacitance of decoupling loop C_z	150 μF

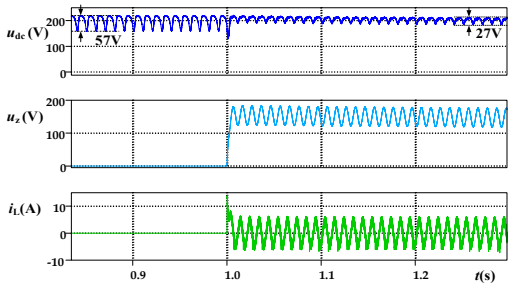
The steady-state simulation waveforms of the estimation method and the proposed method are compared. Under the estimation method, the simulation waveforms before and after the power decoupling loop was connected are shown in Figure 7a. Before 1 s, the power decoupling circuit was not connected. At this time, the second-order ripple energy in the system was all processed by the DC bus capacitor. From the figure, the peak-to-peak value of the voltage ripple reached 57 V, the capacitor voltage and inductor current in the decoupling circuit were both 0 V. After the power decoupling circuit was connected at 1 s, the circuit gradually restored to steady state. The fluctuation of DC bus voltage was greatly reduced compared with that before 1 s, but the DC bus voltage still had a ripple of 27 V.

Under the proposed method, the simulation waveforms before and after the power decoupling circuit was connected are shown in Figure 7b. The power decoupling circuit was also connected at 1 s. After the system was stable, the DC bus voltage ripple was 10 V, which was 17 V less than that in the estimation method. It can be seen that the DC bus voltage ripple was smaller, and the second-order ripple power processing was more effective by the proposed method. Although 150 μF capacitance was introduced into the circuit, if the power decoupling circuit was not connected, a DC bus capacitance C

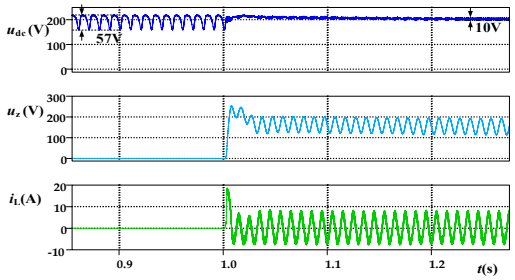
of 1400 μF was needed to achieve the same effect. The waveforms of the power decoupling circuit in two ripple periods are shown in Figure 7c. The average voltage of the decoupling capacitor C_z was stable at 150 V; the voltage ripple was 74 V. In the charging mode, the average value of the inductor current was greater than 0 in each switching cycle; thus, the capacitor voltage u_z rose. The waveform in the discharging mode was similar. The control method was validated by simulation.

6.2. Experiment Verification

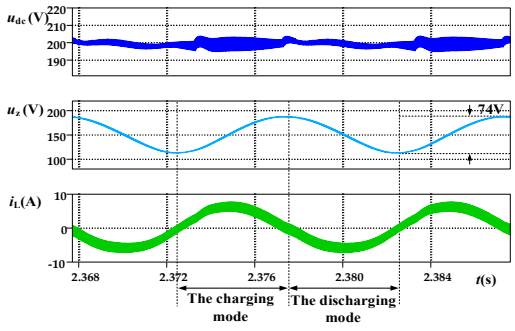
Similar to simulations, two groups of experiments were carried out based on the same experimental prototype. Figure 8 is a picture of the prototype, the parameters of which are selected as in Table 2. The experiment waveforms without a power decoupling circuit are shown in Figure 9. When the power decoupling loop was not connected, the DC bus capacitor was selected to be 250 μF, which is the sum of the DC bus capacitor C and the decoupling capacitor C_z in Table 2. As the figure shows, the voltage and current were in phase, but the voltage fluctuated greatly, and the ripple reached 56 V. A large harmonic component was introduced into the AC input current; thus, the inductor's current waveform was not ideal.



(**a**)



(**b**)



(**c**)

Figure 7. Comparison of steady-state simulation waveforms of the estimation method and the proposed method: (**a**) the estimation method; (**b**) the proposed method; and (**c**) the proposed method in two ripple periods.

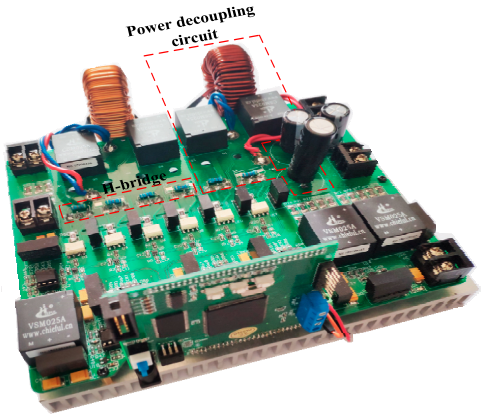


Figure 8. Picture of the experiment prototype.

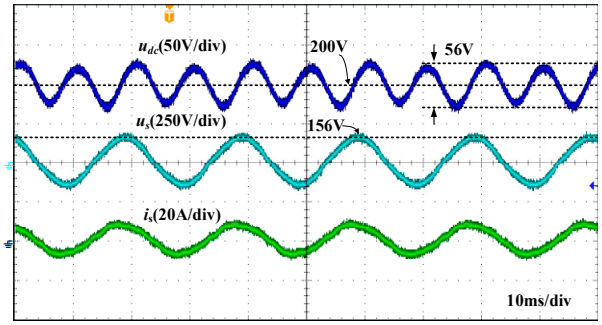


Figure 9. Experiment waveforms of input voltage u_s, input current i_s, and output voltage u_{dc} without the power decoupling circuit.

When the power decoupling circuit was connected, the experiment waveforms obtained by the estimation method and the proposed method are shown in Figure 10. The average voltage of the decoupling capacitor C_z was 150 V. As shown in Figure 10a, the voltage ripple obtained by the estimation method was 34 V, which was 11% less than that without the power decoupling loop. Eleven percent represents the ripple ratio of the DC bus voltage; it was derived from the formula: $\Delta U_{max}/U_{dc}$*×100%. It was proved that this method was effective for second-order ripple power absorption, but the calculation was not accurate enough; thus, the second-order ripple content of the DC bus voltage was still large. As shown in Figure 10b, the voltage ripple of the bus obtained by the proposed method was 13 V within the prescribed range of 10%, which was 20% less than that without the power decoupling loop. Thus, the validity of the proposed control method was verified. The capacitor voltage ripple of the decoupling loop was 90 V, and the inductor current presented a second-order sinusoidal curve with a peak value approximating 6.2 A, which was basically consistent with the simulation results.

Experiment waveforms of the ripple of i_L and the ripple of u_{dc} in each switching cycle are shown in Figure 11. Because of the time axis of the oscilloscope, u_{dc} was approximately constant over the field of view. L was charged and discharged in each switching cycle with the opening and closing of Q_1.

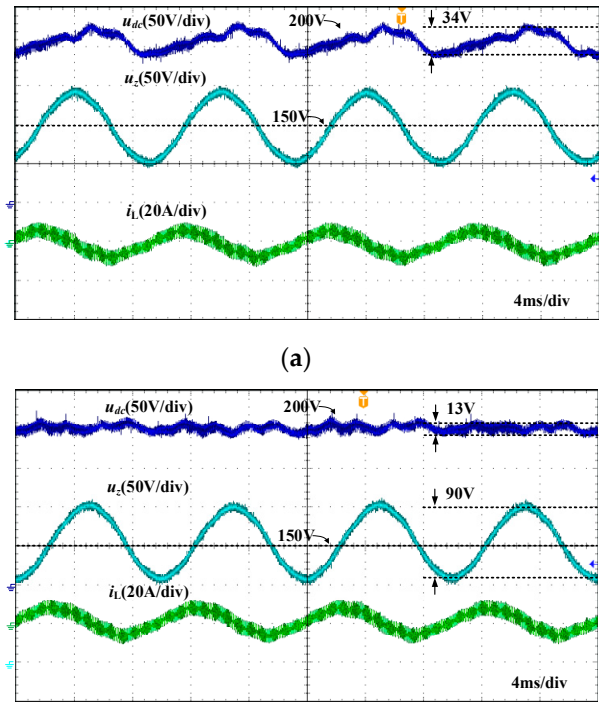


Figure 10. Experiment waveforms of the estimation method and the proposed method at steady state: (**a**) the estimation method; (**b**) the proposed method.

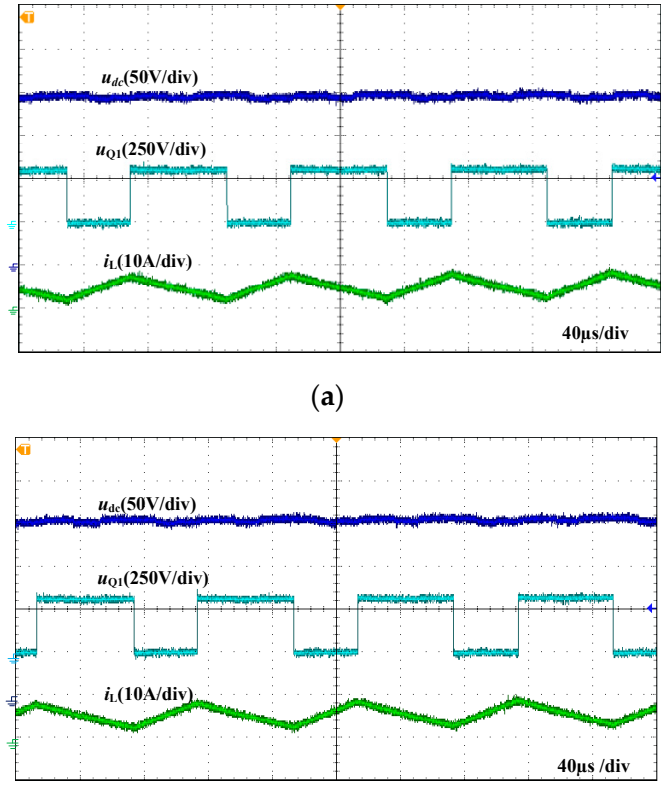


Figure 11. Experiment waveforms of the ripple of i_L and the ripple of u_{DC} in each switching cycle: (**a**) the estimation method; (**b**) the proposed method.

At this time, the operation of the whole system is observed. The experiment waveforms of the input voltage, input current, and output voltage are shown in Figure 12 by the proposed method. As shown in the figure, the input voltage and current were approximately in phase. The input current had a higher sinusoidal degree and a lower harmonic content, which was notably better than that without power decoupling, as shown in Figure 9. As a result, the goal of power decoupling is achieved.

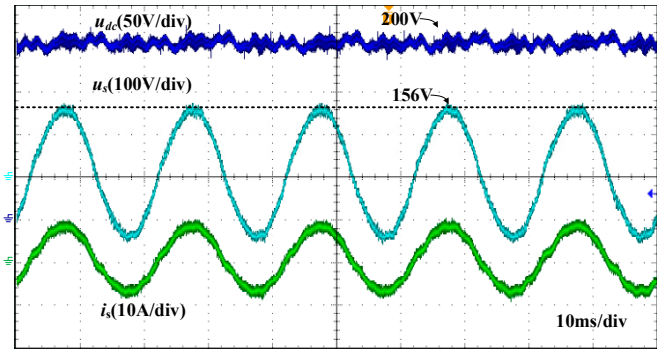


Figure 12. Experiment waveforms of input voltage u_s, input current i_s, and output voltage u_{dc} in the proposed method.

Taking full advantage of the buck-boost circuit's step-up and step-down advantages, the capacitor voltage u_z of the decoupling circuit can be controlled to be higher than that of the DC bus, with an average value of 250 V instead of the average value of 150 V above. Figure 13 shows the experiment waveforms of the proposed method under this voltage level. As shown in the figure, the bus voltage ripple was 14 V within the prescribed range of 10%. The capacitor voltage ripple of the decoupling circuit was 65 V, which is smaller than that when the average value of u_z was 150 V. Therefore, under the condition of maintaining the same DC bus voltage ripple, if the capacitor voltage u_z of the decoupling loop is increased, the voltage ripple will be reduced. The capacitance C_z can be taken to a smaller value accordingly.

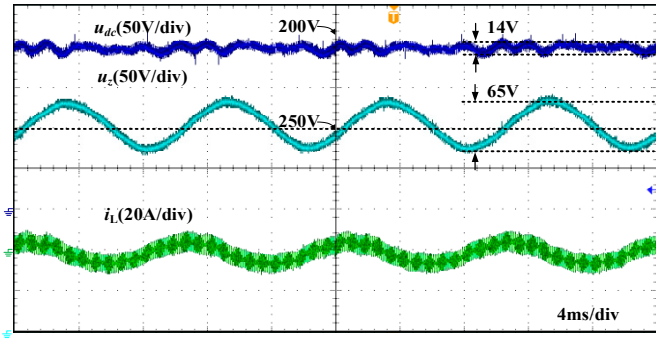


Figure 13. Experiment waveforms when the decoupling capacitor voltage is 250 V.

In order to verify the good dynamic characteristics of the system, a load switching experiment was carried out. Figure 14a shows the experiment waveforms when the full load was switched to 75% load and then switched to full load. The 75 % load indicated that the output power was 75% of the rated power. Figure 14b,c shows the experiment waveforms in load reduction and load increase, respectively. It can be seen that the rise and fall of voltage did not exceed 10 V, and the response time was short. Within 0.1 s after load switching, the system reached steady-state quickly, indicating that the system has good dynamic performance during load switching.

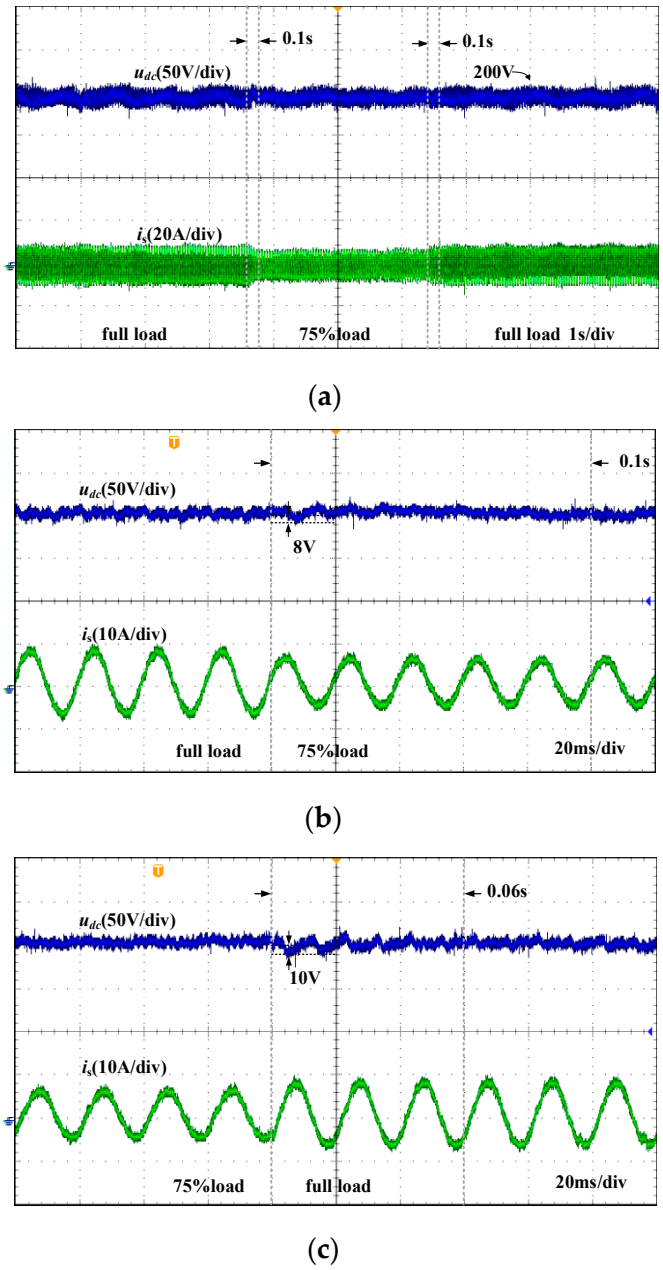


Figure 14. Experiment waveforms for load switching: (**a**) in scanning view; (**b**) in load reduction; and (**c**) in load increase.

7. Conclusions

Based on buck-boost-type power decoupling circuit of the single-phase VSR, an independent power decoupling control strategy with second-order ripple current estimation was proposed in this paper. The second-order ripple component of the DC bus voltage was introduced in the control, which compensated the phase deviation between the command value and the actual value of the second-order ripple current. Thus, the power decoupling circuit can effectively absorb the second-order ripple power, and the DC bus voltage ripple is controlled within the allowable range. Finally, an experimental prototype of 533 W rated power was built for the experiment. With the proposed control method, the DC bus voltage ripple was controlled within 7% in steady state, the voltage overshoot was not more than 10 V in load switching, and the transition time was not more than 0.2 s, which verifies the effectiveness of the control method with a good dynamic response and stable characteristics.

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