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A Charge-Sharing-Based Two-Phase Charging Scheme for Zero-Crossing-Based Integrator Circuits

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Abstract: As an effort to improve the energy efficiency of switched-capacitor circuits, zero-crossing-based integrators (ZCBI) that consist of zero-crossing detectors and charging circuits have been proposed. To break the trade-off between accuracy and speed, ZCBI typically employs a two-phase charging scheme that relies on an additional threshold for zero-crossing detection. This paper proposes a simpler realization method of the two-phase charging scheme by means of charge sharing. To demonstrate feasibility of the proposed method, we designed and fabricated a second-order delta-sigma modulator in 180-nm complementary metal–oxide–semiconductor (CMOS) technology. The measurement results show that the modulator exhibits a peak signal-to-noise-and-distortion ratio (SNDR) of 46.3 dB over the bandwidth of 156 kHz with the power consumption of 684 µW. We also designed the same modulator in 65-nm CMOS technology and simulation results imply that the proposed circuit is able to achieve a much better energy efficiency in advanced technology.

Keywords: delta-sigma modulator; switched-capacitor; low-power design; zero-crossing-based integrator

1. Introduction

In conventional switched-capacitor integrators, the negative feedback around an operational transconductance amplifer (OTA) with a high DC gain forces the two input terminals to have the same potential, controlling the charge transfer from the sampling capacitor to the feedback capacitor. In advanced technology with a reduced supply voltage, however, achieving the high DC gain is not straightforward. In addition, conventional OTAs are not power efficient due to their typical class-A operation [1–4]. As an alternative, zero-crossing-based integrator (ZCBI) circuits have been proposed (Figure 1a) [5–16], where zero-crossing-detectors (ZCD) and current sources are used to control the charge transfer.

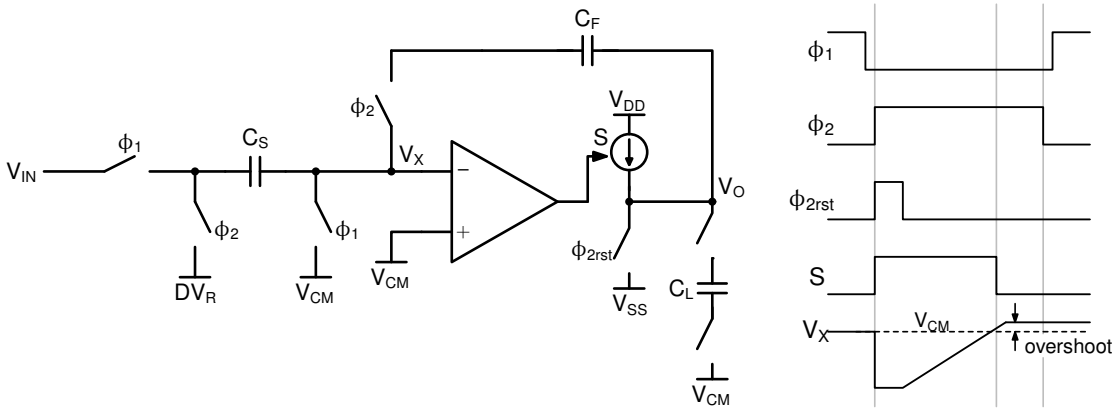
As the timing diagram in Figure 1b shows, the finite delay of the ZCD causes an overshoot at the input of ZCD and consequently at the integrator output. If the current source charges the load with the constant current I, the overshoot voltage at the output of the integrator is given by

$$V_{\mathrm{OVS}} = \frac{I \times t_{\mathrm{d}}}{C_{\mathrm{LD}}}, \tag{1}$$

where t_{d} is the delay of the ZCD and C_{LD} is the total capacitance at the output of the integrator [11]. The overshoot voltage manifests itself as a DC offset at the integrator output, which is not detrimental. However, if the charging current is governed by a resistor R_{S}, whether it be the output resistance of a transistor current source or a kind of current source itself, the overshoot voltage has the additional gain error component as expressed in

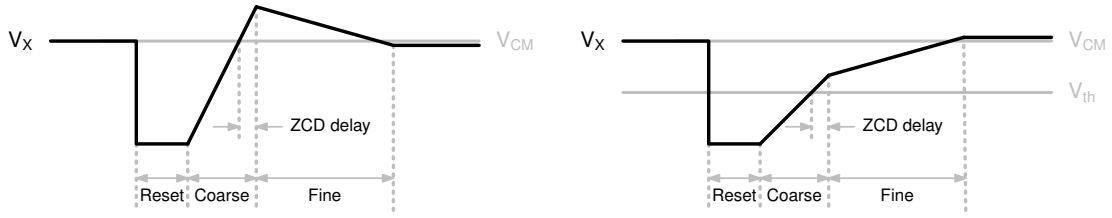
$$V_{\mathrm{OVS}} = (V_{\mathrm{DD}} - V_{\mathrm{O}})(1 - e^{-\frac{t_{\mathrm{d}}}{\tau}}), \tag{2}$$

where $\tau = R_S C_{LD}$ is the time constant. The gain error term modifies the gain and the pole location of the integrator transfer function. More importantly, the current value at the zero-crossing moment and thus the delay t_d become signal-dependent causing nonlinearity in the overshoot voltage [11]. The nonlinearity due to signal-dependent t_d can be reduced by increasing the time constant, but it comes at the cost of reduced speed of the integrator. The trade-off relationship between speed and accuracy can be alleviated by two-phase charging schemes [5,6,10–14]. In a two-phase charging scheme, the charge transfer phase is divided into two phases: coarse and fine. During the coarse phase, a high current is used to make V_X approach V_{CM} quickly; then, during the fine phase, a low current is used to reduce the overshoot. Depending on the direction of charging during the fine phase, the two-phase charging scheme can be bidirectional or unidirectional (Figure 2). If the charging scheme is bidirectional, the coarse phase ends when the ZCD detects zero-crossing through the threshold V_{CM}. During the fine phase, the overshoot voltage is compensated for by the low current of the opposite direction. The unidirectional two-phase charging scheme, on the other hand, introduces an additional threshold V_{th} that is lower than V_{CM} to decide when to make a transition from the coarse phase to the fine phase. The bidirectional scheme is simpler in a sense that it needs only one ZCD. However, it requires greater headroom to accommodate the large overshoot at the end of the coarse phase. With a low supply voltage, therefore, the unidirectional scheme is preferred over the bidirectional scheme.



(**a**) (**b**)

Figure 1. Conventional zero-crossing-based switched-capacitor circuit. (**a**) Schematic diagram. (**b**) Timing diagram.



(**a**) (**b**)

Figure 2. Two-phase charging schemes. (**a**) Bidirectional. (**b**) Unidirectional.

In [15], we have shown that charge sharing can be used to implement the unidirectional two-phase charging scheme without an explicit additional ZCD. This paper presents, in more detail, the design of a second-order ΔΣ analog-to-digital convertor (ADC) that employs the proposed two-phase charging scheme and discusses its effectiveness with measurement results. This paper is organized as follows. Section 2 describes the ZCBI structure that employs the proposed two-phase charging scheme. Section 3 presents the circuit implementation of the fabricated second-order ΔΣ modulator and its measurement results. Effectiveness of the proposed scheme is also discussed. In Section 4, conclusions are drawn.

2. Proposed ZCBI Circuit

Unlike the clocked comparator in most ADCs, the ZCD in Figure 1 needs to continuously monitor whether V_X crosses the threshold V_{CM} or not. Therefore, there is a possibility that the ZCD consumes a great deal of static power. In order to reduce the static power consumption of ZCD, an inverter-based ZCD can be used in lieu of conventional comparator circuits as illustrated in Figure 3 [16]. The ZCD consists of an inverter and an auto-zeroing capacitor (C_Z). During the sampling phase (ϕ_1 is on), the auto-zeroing capacitor samples the voltage difference between V_{CM} and the threshold voltage of the inverter. As a result, the inverter output flips when V_X crosses V_{CM} in the charge transfer phase (ϕ_2 is high). Unfortunately, the inverter output may not be large enough to immediately turn off the current source resulting in a long ZCD delay, especially when the charging current is small. To address this issue, an additional inverter chain is added at the output of the ZCD. However, the inverter chain may increase the effective time delay of the ZCD and it is therefore imperative to make sure that the inverter chain is fast enough to keep the delay as small as possible.

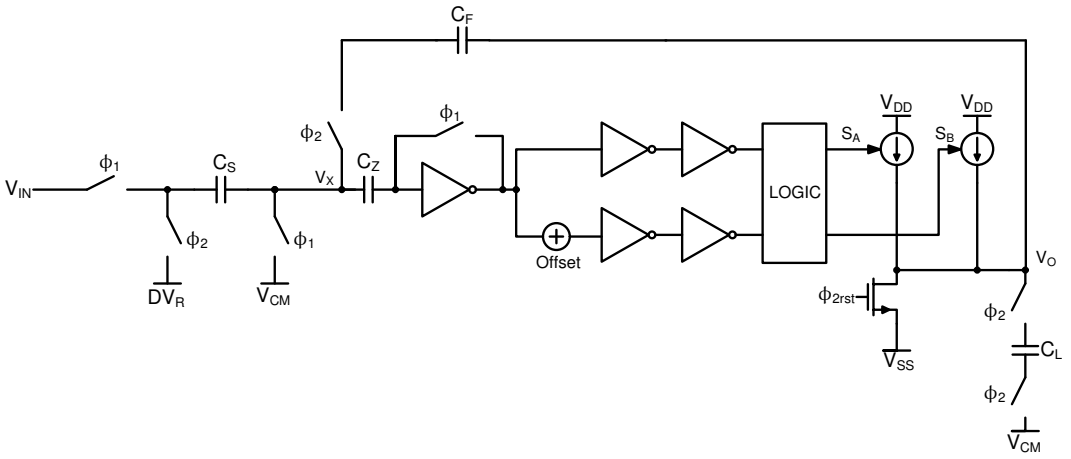
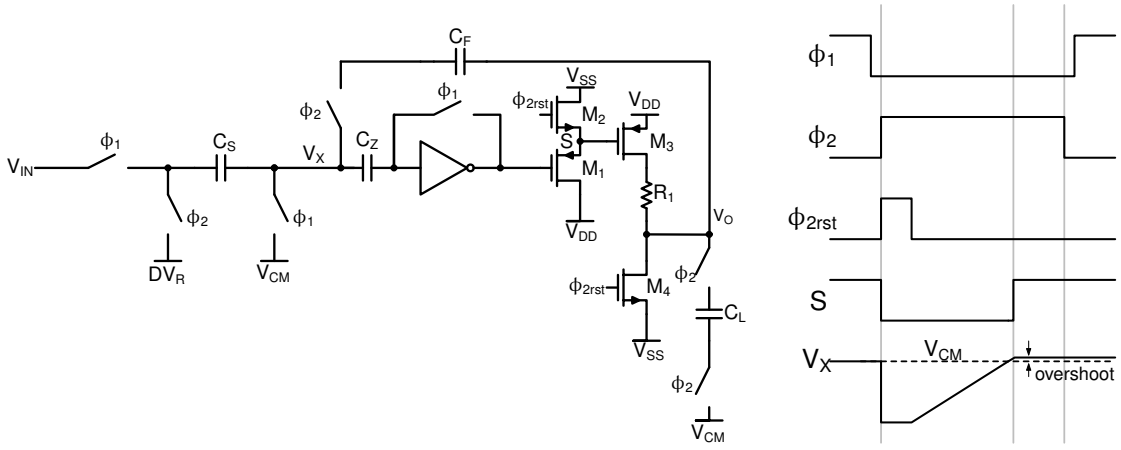


Figure 3. A switched-capacitor circuit using an inverter-based zero-crossing-detectors (ZCD) [16].

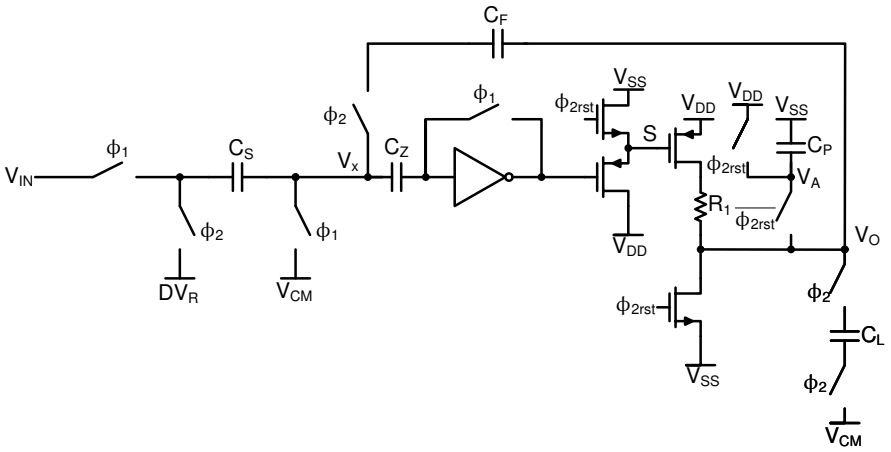
Figure 4 shows our implementation of the inverter-based ZCD, where the inverter is followed by a dynamic buffer. When ϕ_{2rst} goes high for a short period of time at the beginning of the charge transfer phase, M_2 is turned on and the gate terminal of M_3 is pre-charged to V_{SS} thus turning on M_3. The output node is also reset to V_{SS} making V_X lower than V_{CM} in all circumstances. As a result, the inverter output becomes high turning off M_1. When V_X crosses V_{CM}, M_1 is turned on and it can quickly charge the gate of M_3 to turn it off since M_2 is already in the off state.

Although the ZCD delay can be reduced to some degree by the use of a dynamic buffer, a two-phase charging scheme still needs to be implemented to break the speed-accuracy trade-off. Figure 5 illustrates the proposed ZCBI circuit that implements a simple unidirectional two-phase charging scheme. The basic idea behind the proposed scheme is to supply a fixed amount of charge during the coarse phase by using a capacitor rather than a current source. It is equivalent to charging by a current source for a fixed duration of the coarse phase. However, the proposed method does not require either an additional ZCD with a different threshold or an additional control signal to make a transition from the coarse to the fine phase. In Figure 5a, C_P is pre-charged to V_{DD} during the reset phase. When the charge transfer phase starts, C_P is connected to the output node and the charges stored on C_P are shared with other capacitors that are connected to the output node, thus the output voltage being raised instantaneously. After charge sharing, the circuit operates the same way as a conventional two-phase charging scheme in the fine phase. In effect, the charge sharing serves as the coarse phase in a conventional two-phase charging scheme.

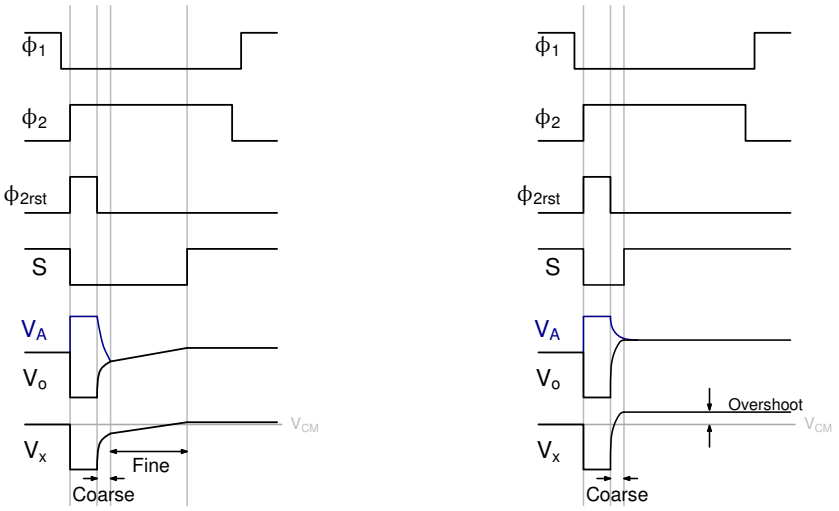


(**a**) (**b**)

Figure 4. The inverter-based zero-crossing-based integrators (ZCBI) using a dynamic buffer. (**a**) Schematic diagram. (**b**) Timing diagram.



(**a**)



(**b**) (**c**)

Figure 5. The ZCBI employing the charge-sharing-based two-phase charging scheme. (**a**) Schematic diagram. (**b**) Normal operation. (**c**) Erroneous operation.

For proper operation of the proposed two-phase charging scheme, however, the amount of charge to be shared must be well controlled. If V_X is greater than V_{CM} at the end of charge sharing, there is

no way to discharge the capacitors, ending up with overshoot (Figure 5c). Therefore, the capacitance of C_P should be carefully chosen so that V_X is lower than V_{CM} under all circumstances when charge sharing is completed. The voltage at the end of charge sharing is expressed as

$$V_X = V_{X|\,reset} + \frac{C_P C_F}{C_P C_F + C_L C_F + C_S C_F + C_S C_P + C_S C_L} V_{DD}, \tag{3}$$

where $V_{X|\,reset}$ is the value of V_X at the end of reset phase and is given by

$$V_{X|\,reset} = \frac{C_S}{C_S + C_F} DV_R - \frac{C_S}{C_S + C_F} v_i[n] - \frac{C_F}{C_S + C_F} v_o[n-1]. \tag{4}$$

In Equation (4), DV_R is the value of the feedback DAC; v_i and v_o are small-signal input and output voltages of the integrator, respectively. Substituting the full-scale value for DV_R, v_i, and v_o gives us the upper bound of $V_{X|\,reset}$, but it is only a loose bound and places more constraint on the size of C_p than required. Alternatively, a more practical value of C_p can be found using the distribution of $V_{X|\,reset}$, which can be obtained as outlined in the next section.

3. Circuit Implementation and Measurement Results

In order to demonstrate feasibility of the proposed technique, a second-order ΔΣ modulator has been fabricated in 180-nm complementary metal–oxide–semiconductor (CMOS) technology. As shown in Figure 6, the modulator is a low-distortion feedforward structure [17] with a 1-bit quantizer. Figure 7 shows the schematic diagram of the modulator. The half-delay integrators are realized with the proposed ZCBI circuits in pseudo differential form, which include switched-capacitor common-mode feedback circuits [18]. The integrator outputs are combined with the modulator input by the adder in front of the 1-bit quantizer. The adder is realized as a switched-capacitor passive adder for low power consumption. The 1-bit quantizer consists of a dynamic latch, which is basically cross-coupled inverters, and C^2MOS buffers [19]. The internal clock generator (not shown in Figure 7) creates various non-overlapping clock signals. The nominal clock frequency is 10 MHz and the intended oversampling ratio (OSR) is 32. Figure 8 shows the chip micrograph. The modulator core occupies 0.3 mm^2. Table 1 shows the summary of the modulator design.

Table 1. Summary of design.

Technology	180-nm CMOS
Sampling Frequency	10 MHz
V_{DD}	1.8 V
V_{CM}	0.9 V
DV_R	0.4 V or 1.4 V
$C_{S,1st}$, $C_{S,2nd}$	25 fF
$C_{F,1st}$, $C_{F,2nd}$	50 fF, 100 fF
*$C_{Ltot,1st}$, $C_{Ltot,2nd}$	300 fF, 500 fF

* C_S and C_F are excluded.

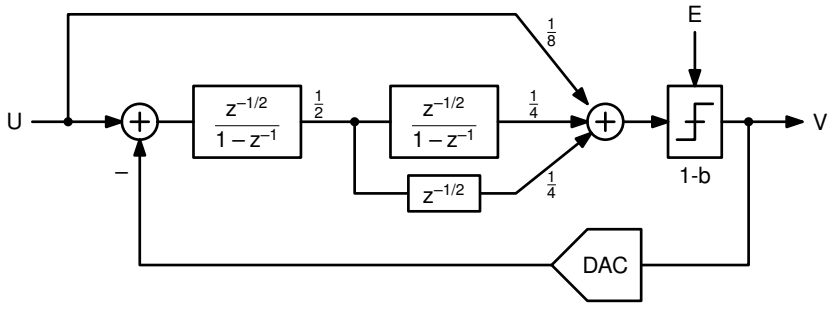


Figure 6. The structure of the designed second-order ΔΣ modulator.

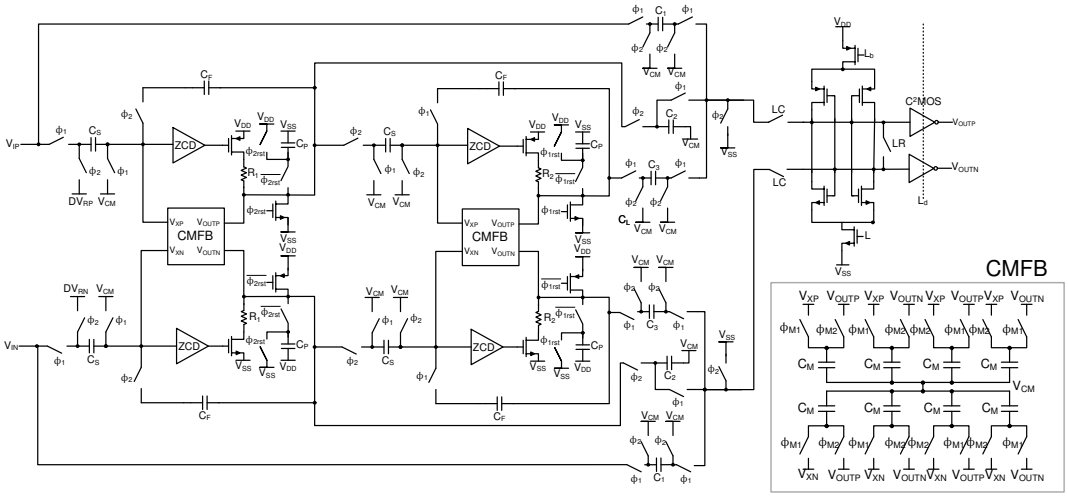


Figure 7. Schematic diagram of the modulator.

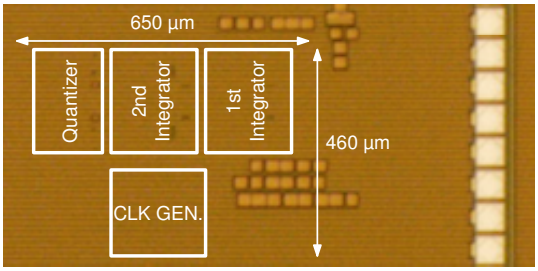


Figure 8. Chip micrograph. The core size is 650 µm × 460 µm.

As described in Section 2, the capacitance for charge sharing should be judiciously chosen for proper operation of the ZCBIs. The modulator in Figures 6 and 7 was simulated with behavioral and transistor-level models for various amplitudes and frequencies of single-tone and multi-tone inputs. Figure 9 shows one instance of the distribution of $V_{X|reset}$. In this simulation, V_{DD} is 1.8 V and DV_R is either 0.4 V or 1.4 V. It is shown that $V_{X|reset}$ hardly exceeds 0.6 V. Substituting 0.6 V for $V_{X|reset}$ in Equation (3) and solving for the condition that V_X is never larger than V_{CM} at the end of charge sharing yields the constraint on the value of C_P. For instance, C_F is $2C_S$ for the first integrator and the condition for C_P is given by

$$C_P \leq \frac{11}{9} C_S. \tag{5}$$

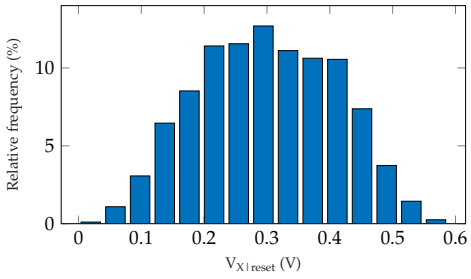


Figure 9. Distribution of $V_{X|reset}$.

The fabricated chip was tested using the measurement setup shown in Figure 10. The PCB includes a single-ended-to-differential conversion circuit, reference voltage generators, and a crystal oscillator for the clock signal. Figure 11a shows the measured power spectral density of the modulator output with a 9.76-kHz 507-mVpp input signal, and Figure 11b shows signal-to-noise ratios (SNRs) and signal-to-noise-and-distortion ratios (SNDRs) for various input amplitudes. From the power spectral

density, the second-order noise shaping is clearly seen. Unfortunately, high harmonic tones are also evident. These harmonic components are probably due to a couple of errors in the design: (1) the clock signals for bottom-plate sampling are connected in a wrong way, and (2) the fabricated modulator lacks reference buffers inside the chip. These errors are also believed to have raised the noise floor by about 3 dB. The second-order harmonic is probably due to the unbalanced reference voltages that are externally supplied to the chip. The mismatch between the pseudo-differential signal paths might have also contributed to the even-order harmonics. The measured peak SNR and SNDR are 50.1 dB and 46.3 dB, respectively. The dynamic range is about 56 dB. From process corner simulations, it is expected that the peak SNDR may drop by about 2.4 dB over the process variations. As suggested in Figure 12, the peak SNR and SNDR are also expected to deteriorate as the temperature increases.

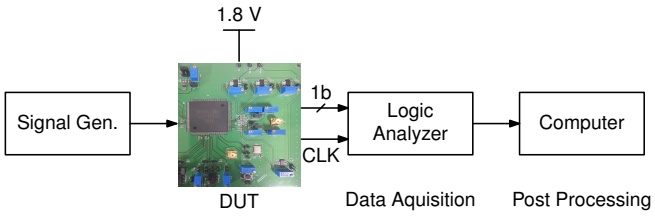
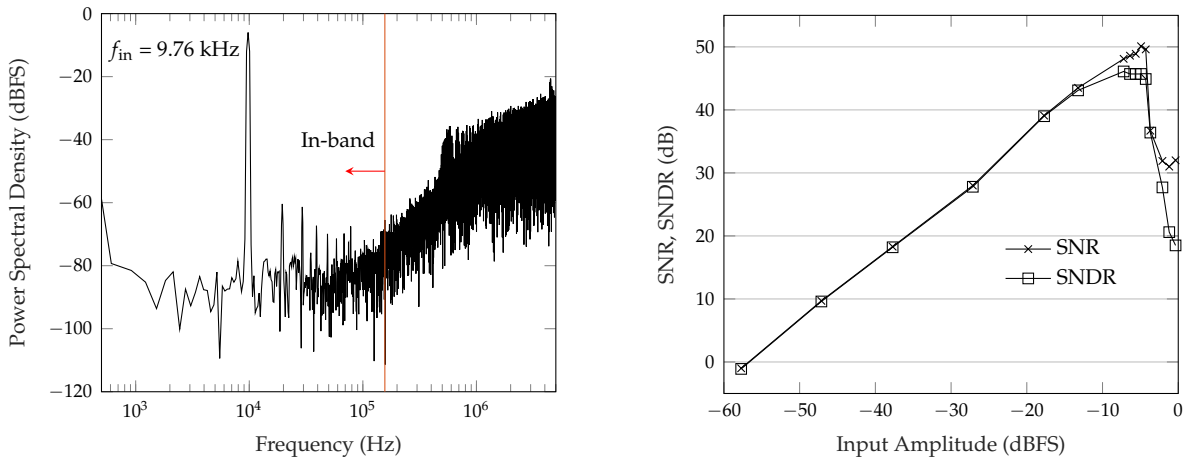


Figure 10. Test setup.



(**a**) (**b**)

Figure 11. Measured results. (**a**) Power spectral density (# of fast Fourier transform (FFT) bins: 32768). (**b**) Signal-to-noise ratio (SNR) and signal-to-noise and distortion ratio (SNDR) versus input amplitudes.

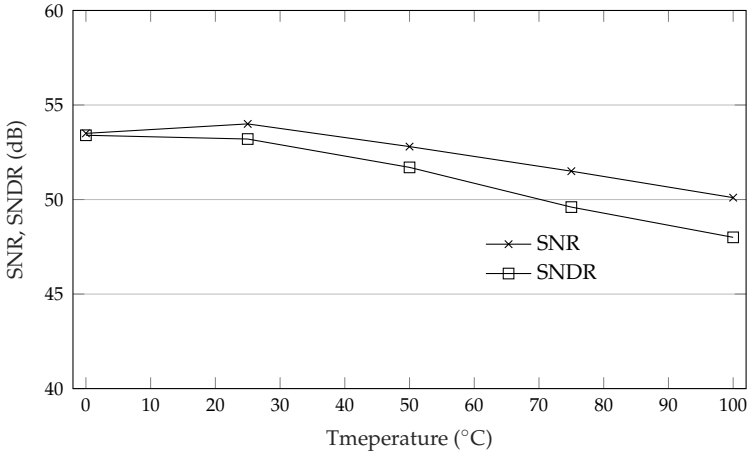


Figure 12. Simulated SNR and SNDR over temperature.

The total power consumption is 684 µW from a 1.8-V supply voltage. Table 2 shows the power consumed in each sub-block. The most power-hungry blocks are integrators, and the clock generator also dissipates a considerable amount of power.

Table 2. Power consumption breakdown.

Sub-Block	Power Consumption (µW)	Percentage (%)
1st Integrator	235	34.3
2nd Integrator	229	33.5
Adder	5.6	0.8
Quantizer	5.7	0.8
DAC	0.9	0.1
Clock Genrator	151	22.1
Ref. buffers, etc.	56.8	8.4
Total	684	100

Table 3 summarizes the measured performance in comparison with related works. The figure-of-merit (FoM) of the fabricated modulator is not impressive owing to the aforementioned design errors and the rather high supply voltage. We redesigned the same modulator in 65-nm technology and its performance is also summarized in Table 3. With the lowered supply voltage and improved design, the power consumption is drastically reduced from 684 µW to 274 µW. Furthermore, the sampling frequency can be increased to 50 MHz without degradation of SNR or SNDR, resulting in better FoMs. Even if the SNDR discrepancy of about 5 dB is taken to account between schematic simulation and measurement, the proposed modulator is expected to achieve competitive performance.

Table 3. Performance comparison with other work.

	[11]	[13]	[14]	[16]	This Work		
Technology (nm)	45	180	65	160	180	65[(1)]	65[(1)]
Supply Voltage (V)	1.1	1.8	1.2	1.0	1.8	1.2	1.2
Sampling Frequency (MHz)	50	2.56	40	0.014[(2)]	10	10	50
Oversampling Ratio	30	64	8	1	32	32	32
Bandwidth (kHz)	833	20	2500	0.7	156	156	781
Peak SNDR (dB)	47.7	65.3	70.4	N/A	46.3	53.2	53.7
Peak SNR (dB)	52.5	N/A	N/A	81.8	50.1	56.3	56.5
Dynamic Range (dB)	54.3	71	71.3	N/A	56	N/A	56.5
Power Consumption (µW)	630	420	3730	20	684	274	312
$\mathrm{FoM_S}$[(3)] (dB)	139	142	159	157	130	140.8	148
$\mathrm{FoM_W}$[(4)] (pJ/conv-step)	1.91	6.98	0.276	1.48	13.2	2.35	0.5

[(1)] Simulation results. Others are from measurements. [(2)] Self-timed incremental ADC. Translated from the longest conversion time. [(3)] $\mathrm{FoM_S} = \mathrm{SNDR(dB)} + 10\log_{10}(\mathrm{Bandwidth/Power})$. [(4)] $\mathrm{FoM_W} = \mathrm{POWER}/(2^{(\mathrm{SNDR}\,-\,1.76)/6.02} \times 2 \times \mathrm{Bandwidth})$.

4. Conclusions

ZCBI is an attractive alternative to the conventional power-hungry switched-capacitor integrator because the ZCD can be implemented using a simple inverter circuit and auto-zeroing techniques. However, ZCBI is prone to errors caused by the overshoot, and reducing the overshoot results in lower speed in general. In order to break the trade-off between speed and accuracy, a two-phase charging scheme is needed, but it is not straightforward to apply the conventional two-phase charging scheme to the inverter-based ZCD. This paper proposes the use of charge sharing to implement the two-phase charging scheme. The proposed technique is readily applicable to the inverter-based ZCD and is able to reduce the power consumption and the circuit complexity. The proposed charging scheme was applied to a second-order ΔΣ modulator designed in 0.18-µm CMOS technology. The modulator consists of

two proposed ZCBIs, a 1-bit quantizer, a 1-bit DAC, and a clock generator. The ZCD for ZCBIs makes use of a dynamic buffer to reduce the delay. Measurement results show that the modulator achieves a 56-dB dynamic range and a 46.3-dB peak SNDR over a 156-kHz in-band bandwidth with a 684-µW power consumption. We also designed the modulator in 65-nm CMOS technology and simulation results suggest that the proposed modulator is likely to achieve better energy efficiency in advanced technology.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

OTA	Operational Transconductance Amplifier
ZCBI	Zero-Crossing-Based Integrator
ZCD	Zero-Crossing Detector
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
CMOS	Complementary Metal-Oxide-Semiconductor
OSR	Over-Sampling Ratio
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
FoM	Figure of Merit

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