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# A High-Accuracy Ultra-Low-Power Offset-Cancelation On-Off Bandgap Reference for Implantable Medical Electronics

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**Abstract:** An ultra-low-power and high-accuracy on-off bandgap reference (BGR) is demonstrated in this paper for implantable medical electronics. The proposed BGR shows an average current consumption of 78 nA under 2.8 V supply and an output voltage of 1.17 V with an untrimmed accuracy of 0.69%. The on-off bandgap combined with sample-and-hold switched-RC filter is developed to reduce power consumption and noise. The on-off mechanism allows a relatively higher current in the sample phase to alleviate the process variation of bipolar transistors. To compensate the error caused by operational amplifier offset, the correlated double sampling strategy is adopted in the BGR. The proposed BGR is implemented in 0.35 µm standard CMOS process and occupies a total area of 0.063 $mm^2$. Measurement results show that the circuit works properly in the supply voltage range of 1.8–3.2 V and achieves a line regulation of 0.59 mV/V. When the temperature varies from −20 to 80 °C, an average temperature coefficient of 19.6 ppm/°C is achieved.

**Keywords:** bandgap reference; ultra-low power; high accuracy; switched-RC; correlated double sampling

## 1. Introduction

Along with the continuous development of modern society and growing demand for high-quality life, implantable medical electronics are increasingly adopted in healthcare medical devices such as cardiac pacemakers [1–3]. These devices are usually battery powered and need to have ultra-low power consumption of a few microwatts or less [4–8]. Since they would probably be placed where they are not easily removed or recharged, they have to continue working for a relatively long time. A number of important analog circuits for high-precision signal processing, such as voltage regulators, analog to digital converters (ADCs) and digital to analog converters (DACs), are used in almost every biomedical system. All of them demand an accurate bandgap reference (BGR) [9]. In these devices, BGRs provide the voltage references for other important functional blocks and are supposed to be working all the time. Thus, the required average current dissipation of BGR is in the range of several tens of nano-ampere [10–12].

To meet the requirement for low power, subthreshold voltage references without bipolar transistors have been developed and used widely [10–12]. However, these $V_{TH}$-based references often suffer from degraded performance in accuracy since the threshold voltage ($V_{TH}$) of MOSFET changes too much (about 50–100mV) with process variation. Trimming is usually employed to solve this issue. However, the temperature coefficient would be worse after trimming [12]. A conventional bipolar junction transistor (BJT)-based BGR can provide a fairly precise reference voltage, but it requests

larger power consumption. When we try to budget a lower current consumption for BJT-based BGR, resistors with very large values are needed, and the $V_{BE}$ of BJT also varies dramatically. $V_{BE}$ variation introduces large fluctuations to the output reference voltage. Even for relatively larger budgeted power consumption, trimming is still generally required for BJT-based BGR because of the existence of mismatch and offset [13].

In this paper, an ultra-low power, high accuracy BGR is presented. The proposed reference provides a 1.17 V output under 2.8 V supply voltage with 78 nA average current consumption. An on-off bandgap combined with sample-and-hold switched-RC filter is developed to reduce power consumption and noise. The on-off mechanism increases the working current of the BJT-based BGR during the sample period, which decreases $V_{BE}$ spread. A correlated double sampling (CDS) strategy is adopted to cancel the offset of the operational amplifier (Opamp), which is fulfilled by a sampling capacitor block combined with chopper mechanism. The conflict between low power and high accuracy is preliminarily settled. The theoretical foundation and specific circuit design are described in Section 2. Section 3 presents the simulation and measurement results as well as a performance comparison. Finally, conclusions are summarized in Section 4.

## 2. Proposed Bandgap Reference

### 2.1. Error Analysis of the BJT-Based BGR

The key point of this paper is to utilize the techniques of offset cancelling, correlated double sampling and switched-RC to improve the accuracy of the raw BGRs under stringent power consumption constraints. A conventional BJT-based BGR is employed here for demonstration. The core circuit of the BJT-based BGR is shown in Figure 1. The reference voltage generated by it is given by:

$$V_{REF} = V_{BE2} + \frac{R_2}{R_1}\Delta V_{BE}. \quad (1)$$

When considering non-ideal factors relevant with $V_{BE}$ and Opamp offset, Equation (1) can be approximately rewritten as

$$V_{REF}' = V_{BE2}' + \frac{R_2}{R_1}(\Delta V_{BE} + V_{os}) \quad (2)$$

where the superscript $'$ denotes the erroneous quantity. High mismatch characteristic of MOS transistors can introduce considerate offsets to Opamp especially under extreme low power consumption. The $V_{BE}$ spread is also critical because it directly translates an error in $V_{REF}$. The proposed circuit concentrates on canceling these two sources of errors which have large magnitudes of effects on the accuracy of BGR output voltage.

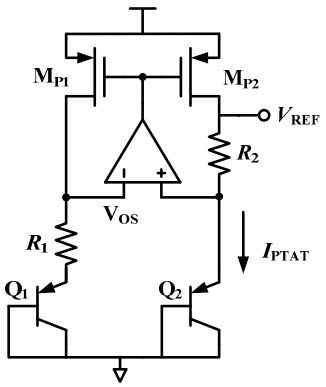



**Figure 1.** The basic topology of the bipolar junction transistor (BJT)-based bandgap reference (BGR) core circuit.

### 2.2. Architecture of the Proposed BGR Circuit

The systematic architecture of the proposed BGR is shown in Figure 2, which consists of an on-off $V_{BE}$-based BGR with chopper mechanism, a sampling-capacitor block, and a sample-and-hold switched-RC filter. Also, there is a digital block to generate the low-duty-cycle clocks used in the on-off BGR, which is manually designed as the analog circuits to reduce the turnover rate of the clocks and thus save power. The on-off BGR takes advantages of the conventional $V_{BE}$-based BGR topology. When consuming dozens of microampere (μA), the conventional $V_{BE}$-based BGR operates reliably and has little process variation spread. During the hold period, the on-off BGR is turned off to save power. The sampling-capacitor block is based on the technique of correlated double sampling (CDS), which samples twice in a working (on) period, before and after the conversion of the chopper connection state in the on-off BGR, respectively. Therefore, the offset of the Opamp $V_{os}$ is cancelled out. When the BGR block entered the off state, the switched-RC filter takes the average of the last twice sampled voltages, holds it until next working (on) state, and gets rid of the out-of-band noise through the function of filtering.

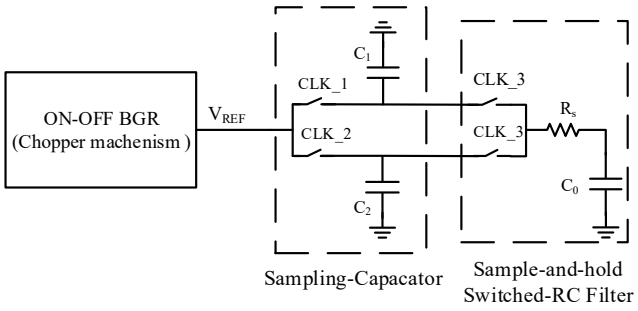



**Figure 2.** Block diagram of the proposed BGR.

### 2.3. Chopper Mechanism and Correlated Double Sampling

Figure 3 shows the implementation of the on-off BGR which employs chopper mechanism. A near-zero power consumption start-up structure is adopted. The parameter values of the main components in the BGR core circuit are as follows. The emitter area of $Q_1$ and $Q_2$ is 2 × 2 μm. $R_1$ = 10 kΩ and $R_2$ = 80 kΩ. The size of $MP_{1/2}$ is 8 μm/16 μm × 6 while the size of the switch transistors is 4 μm/1 μm × 1. The sizes of the transistors are designed to be large for good matching and low flicker noise. Considering the low speed characteristic of the designed circuit, the lengths of the transistors are selected at least 3 times of the 350 nm minimum channel length for lower static leakage current.

Under phase $\Phi_1$ and $\Phi_2$, the BGR power cycle is controlled by the clock ON/OFF CLK as shown in Figure 3b. With the duty cycle D = 0.25% ($T_{ON}$ = 250 us, $T_{ON}$ + $T_{OFF}$ = 100 ms), a working current of 16 uA is budgeted for the BGR block to achieve an average power consumption as low as 40 nA. The base-emitter voltage of transistor $Q_2$ is given by

$$V_{BE2} = V_T \ln(\frac{I_C}{J_S A}), \tag{3}$$

where $I_C$ and $J_S$ are the working collector current and reverse saturation current per unit area of the transistor, respectively, and A is the emitter area. We assume the current variation is $I_X$. Then the relative error can be deduced as in Equation (5).

$$V_{BE2}' = V_T \ln(\frac{I_C + I_X}{J_S A}) \tag{4}$$

$$\varepsilon = \frac{V_{BE}' - V_{BE}}{V_{BE}} = \frac{\ln(\frac{I_C+I_X}{J_S A})}{\ln(\frac{I_C}{J_S A})} - 1 \approx \frac{1}{\ln(\frac{I_A}{J_S A})} \cdot \frac{I_X D}{I_A}, \tag{5}$$

where $\varepsilon$ represents the relative error, and $I_A = I_C$. $D$ is the average current. When the working collector current $I_C$ is increased by an on/off duty cycle of 0.25%, the relative error spread of $V_{BE}$ is 400 times less.

The chopper blocks are controlled by the 10Hz CH_CLK to cancel the offset of the Opamp under phases $\Phi_3$ and $\Phi_4$. In the middle of the on-phase of BGR, the chopper blocks convert connection status from ($X_2$—A, $X_1$—B) to ($X_1$—A, $X_2$—B). In the next on-phase, the connection status changes back. Another chopper block is introduced in the signal path of the designed Opamp to assure that a negative feedback loop be formed according to the chopper status in the on-off BGR.

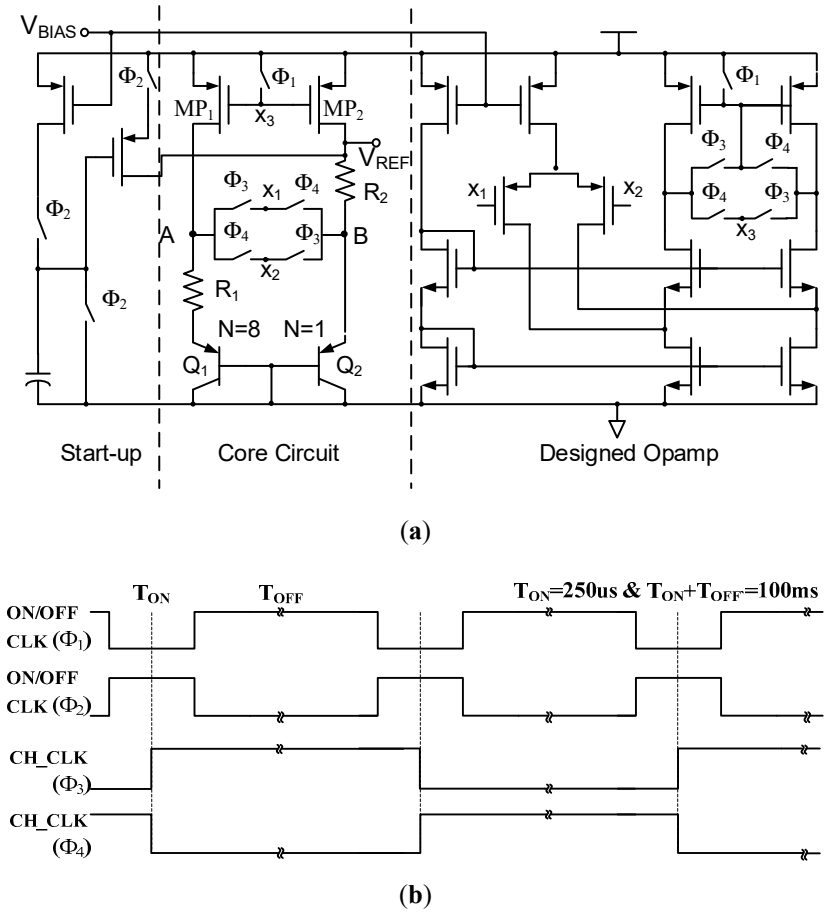



**Figure 3.** (**a**) Proposed on-off BGR with chopper mechanism; (**b**) Control clocks for BGR power cycle and chopper blocks.

Figure 4 shows the sampling-capacitor circuit using the technique of correlated double sampling (CDS) [14,15]. The values of the sampling capacitors are selected as $C_1 = C_2 = C_0 = 40\ \mu m \times 40\ \mu m$ (1.6 pF). In the control of double sampling clocks CLK_1 and CLK_2, whose clock timings are shown in Figure 4b, $C_1$ and $C_2$ sample the output of the on-off BGR $V_{REF}$ before and after the chopper connection state conversion during $T_{S1}$ and $T_{S2}$, respectively, in a working (on) period. $C_0$ samples during the interval $T_S$ and sums up the two sampled voltages in it. Using Equation (2), only the Opamp offset is considered,

$$V_1' = V_{BE2} + \frac{R_2}{R_1}(\Delta V_{BE} + V_{os}) = V_{des} + \frac{R_2}{R_1}V_{os} \tag{6}$$

$$V_2' = V_{BE2} + \frac{R_2}{R_1}(\Delta V_{BE} - V_{os}) = V_{des} - \frac{R_2}{R_1}V_{os} \tag{7}$$

$$V_1'C + V_2'C + V_0C = V_0' * 3C \qquad \text{If, } V_0' = V_0 \quad \text{So, } V_0' = \frac{V_1' + V'_2}{2} = V_{des}, \tag{8}$$

where $C_1 = C_2 = C_0 = C$, $V_1'$ is the voltage on $C_1$ which is sampled before the connection state conversion, $V_2'$ is the voltage on $C_2$ sampled after the conversion, $V_0$ is the current voltage on $C_0$ and $V_0'$ is the sample voltage in next cycle on $C_0$. Eventually, $V_{des}$ is the original design value of $V_{REF}$. When the stable condition is reached, $V_0$ is the average value of $V_1'$ and $V_2'$, canceling the error of $V_{REF}$ caused by the Opamp offset.

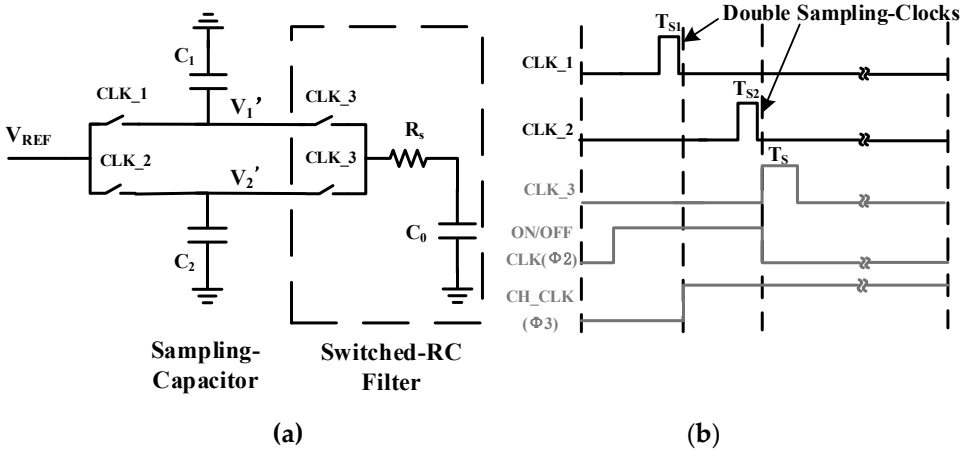



**Figure 4.** (**a**) Proposed sampling-capacitor circuit along with switched-RC block; (**b**) Control clocks for sampling switches.

### *2.4. Sample-and-Hold Switched-RC Filter*

Figure 5 shows the circuit implementation of the sample-and-hold switched-RC filter. A MOS-R is used to achieve a high RC filtering resistance of 25 MΩ with small chip area. To alleviate the effect of injection and clock feedthrough, a dummy MOS switch $M_2$ is added in series with the actual switch $M_1$ [13].

Since the drain-bulk and drain-source leakage is critical to the accuracy and stability of $V_{REF}$ output, especially during a long hold time of 100 ms, a simple feedback buffer $A_1$ is used to reduce the voltage drop. In the hold phase, the bulk and source nodes of $M_1$ are buffered to $V_{REF}$ through $M_7$, eliminating charge leakage at $C_S$.

Moreover, the filter emulates a much lower filter pole frequency by pulse-switching them. Compared to the RC filter in Figure 2, the effective pole frequency in Figure 5 is given by [13]:

$$f_{LPF} = \frac{D}{2\pi R_S C_S} \tag{9}$$

with $C_S$ = 10 pF, $R_S$ = 25 MΩ, and $D$ = 0.06% ($T_S$ = 60 us, $T_H + T_S$ = 100 ms), a filter pole of 0.4 Hz can be achieved, which is about two decades lower than the noise integration bandwidth. Consequently, out-of-band noise could be filtered more thoroughly.

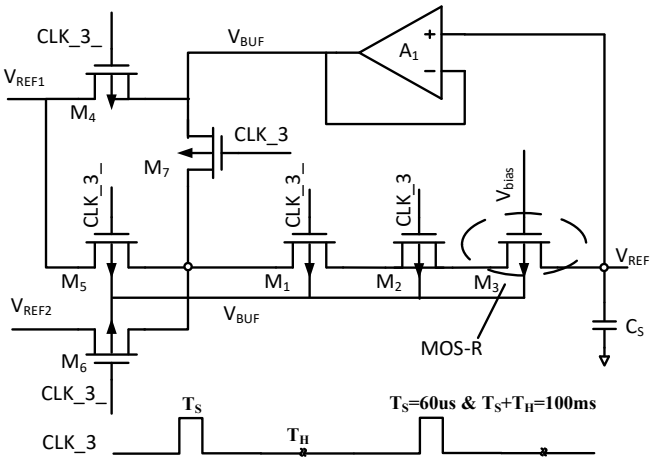



**Figure 5.** Proposed sample-and-hold switched-RC filter circuit and control clock timing.

## 3. Simulation and Measurement Results

The Offset-Cancelation Switched-RC Bandgap Reference presented in this paper has been applied in an implanted cardiac pacemaker ASIC, featured with low power, high reliability and low speed. Consequently, 0.35 μm CMOS technology is employed, which is not advanced but adequately qualified for such applications [1,2]. Also, a lithium-iodine battery with a typical supply voltage of 2.8 V is usually used for cardiac pacemakers, which has a sufficient level of safety and good discharging characteristics [4].

For on-off BGRs with small duty cycles, the settling time for start-up is usually concerned. Figure 6 shows the transient output voltage of the proposed circuit at the supply voltage of 2.8 V and temperature of 27 °C. It takes about 0.6 ms to reach steady state. Monte Carlo 200 simulation runs have been done after layout parasitic extraction, considering the process variation and mismatch. The results are presented in Figure 7a. The mean value (μ) of the proposed BGR is 1.1689 V with the standard deviation (σ) of 4.6 mV, and the coefficient of variation is calculated to be about 0.39%. The simulated temperature dependence of the output reference voltage $V_{REF}$ is plotted in Figure 7b. The temperature coefficient (TC) of the proposed BGR is 9.43 ppm/°C with temperature ranging from −20 to 80 °C.

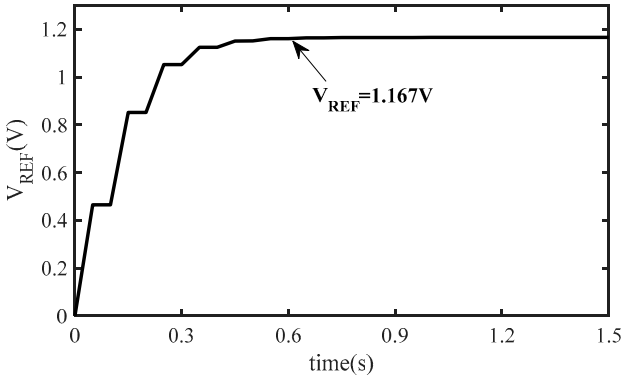
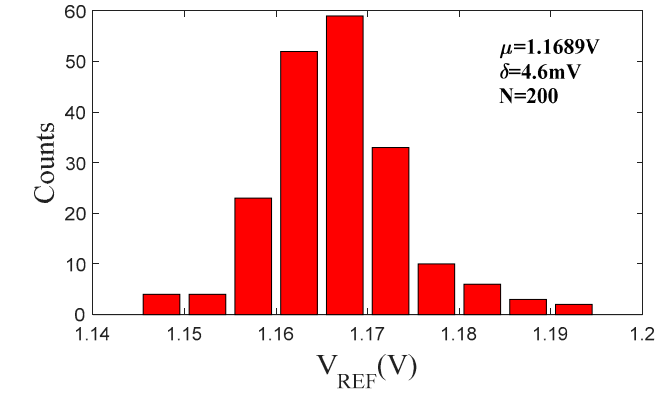
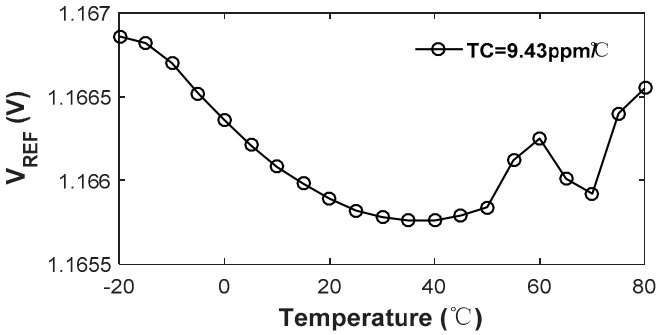



**Figure 6.** The output voltage of the proposed circuit.




(**a**)




(**b**)

**Figure 7.** (**a**) 200 Monte Carlo simulation results. (**b**) Temperature coefficient simulation at 2.8 V supply.

The proposed BGR circuit is implemented in 0.35 μm standard CMOS process. Figure 8 shows the BGR micrograph of the die. The core circuit occupies an area of 0.063 $mm^2$, which could be optimized after an elaborate layout design. The total current consumption is measured as 78 nA on average from 30 samples. The digital clock generation block consumes 26 nA average current, which means that the percentage of the overhead power consumption by the clock generation block is 33.3% or one third. Figure 9 shows the distribution of the measured output voltage in 30 samples with 2.8 V supply voltage at 27 °C. The mean value (μ) is 1.167 V with the standard deviation (σ) of 8.1 mV. The proposed BGR can achieve an accuracy of 0.69% in the measurement. The accuracy of 0.69% is achieved without trimming and could be considered to be adequate for most implantable biomedical electronics. The low power feature is obtained due to the low duty cycle (D = 0.25%) operation of the on-off BRG. Moreover, the following correlated double sampler and the switched-RC filter just consume about 12 nA average current and occupy about 0.03 $mm^2$ chip area of the total 0.063 $mm^2$ chip area, but guaranteed the good performance of the on-off BRG. The on-off BGR achieves an untrimmed measured accuracy of 0.69%, which is comparable with the accuracy of BGRs with current consumptions of hundreds of times larger, just at a small price.

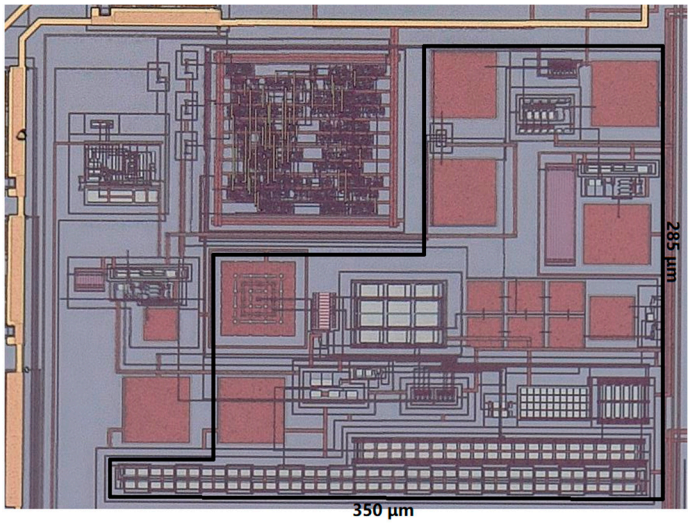



**Figure 8.** Microphotograph of BGR chip.

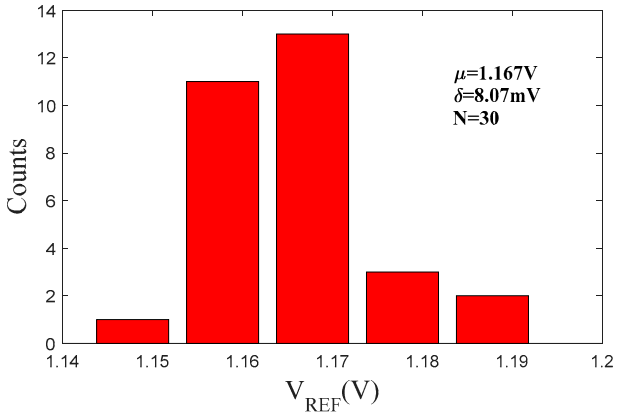



**Figure 9.** Measured results for 30 samples.

Figure 10 shows $V_{REF}$ versus temperature ranging from −20 to 80 °C and the measured TC ranges from 13.7 ppm/°C to 38.2 ppm/°C with an average TC of 19.6 ppm/°C. Figure 11 shows the measured reference voltage versus the supply voltage at 27 °C. When the supply voltage changes from 1.8 V to 3.2 V, the BGR voltage variation is less than 0.83 mV. The reference voltage can achieve the line regulation of 0.59 mV/V. For measurement convenience, when measuring the power supply rejection ratio (PSRR), the on-off period is set at 10 ms instead of 100 ms, which will not affect the authenticity of the measured results. Figure 12 shows the PSRR results, which is better than 58.6 dB before 200 kHz. There are peaks at multiples of 100 Hz (1/10 ms) due to the characteristic of sampling. When the frequency of the fluctuation on the supply is the same as the sampling rate, the effect of the supply fluctuation on the sampled output voltage is also the same during the on phase in every sampling period and thus will be attenuated.

The performance of the proposed BGR circuit is summarized in Table 1, and these results are compared with other published references. From Table 1, it is observed that this work has the best line regulation and temperature coefficient in the untrimmed voltage references, while it also has advantages in the aspects of current consumption and untrimmed accuracy. However, the limitations of such on-off BGR are analyzed as follows. First, a small ripple at the switching moment still exists after switched-RC filtering. For continuous-time applications, this issue should be considered. Second, because the BGR output voltage is sampled in the capacitor, it has limited driving ability.

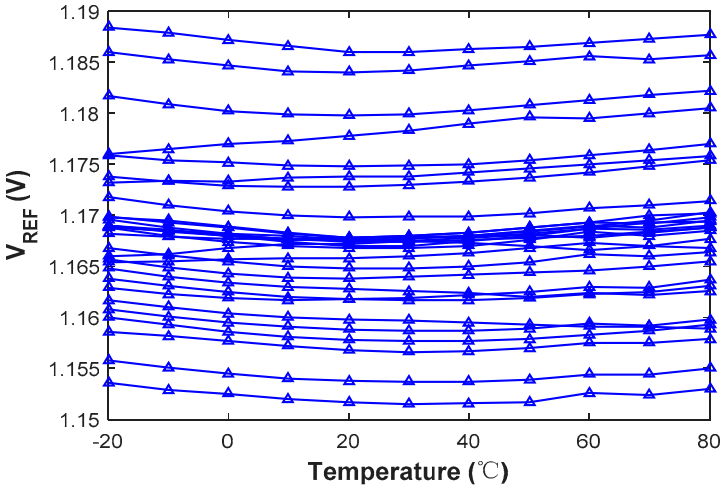



**Figure 10.** Measured reference voltage versus temperature for 30 samples.

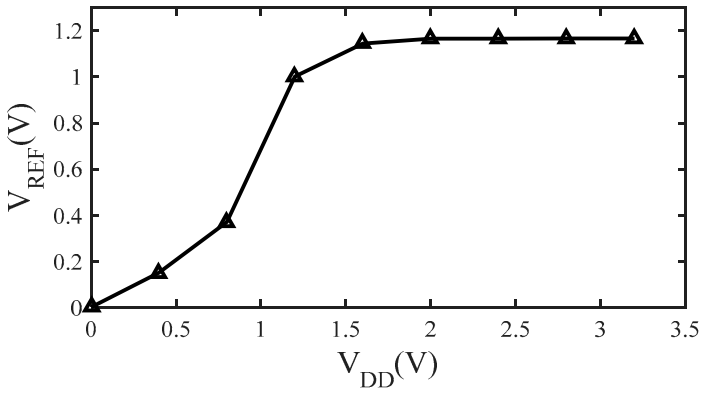



**Figure 11.** Measured reference voltage versus the supply voltage.

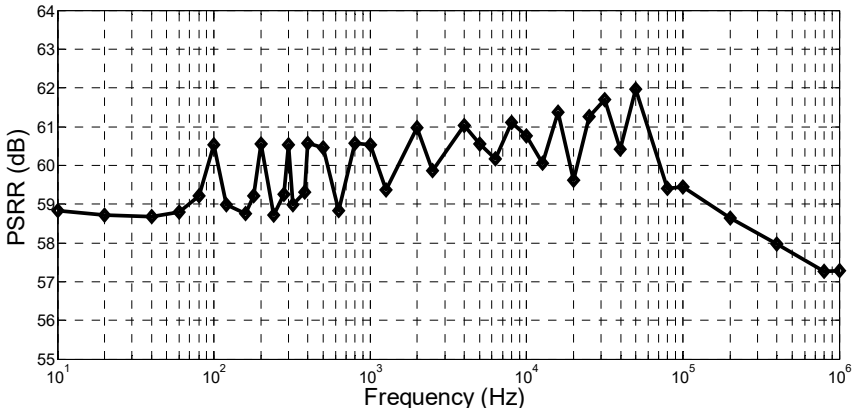



**Figure 12.** Measured power supply rejection ratio (PSRR).

**Table 1.** Comparison table.

| Parameter | [16] | [17] | [18] | [19] | This Work |
|---|---|---|---|---|---|
| Process | 65 nm | 180 nm | 130 nm | 180 nm | 350 nm |
| Publication Year | JSSC 2017 | TCAS-II 2015 | ISSCC 2015 | TCAS-II 2017 | 2019 |
| Accuracy (σ/μ) | $0.39\%^{(T)}$ | $3.9\%^{(UT)}$ | $0.67\%^{(UT)}$ | $2\%^{(T),1}$ | $0.69\%^{(UT)}$ |
| Type | $V_{TH}$ | $V_{TH}$ | $V_{BE}$ | $V_{TH}$ | $V_{BE}$ |
| TC (ppm/°C) | $5.6^{(T)}$ | $64^{(T)}$ | $75^{(UT)}$ | $84.5^{(UT)}$ | $19.6^{(UT)}$ |
| Supply | 0.8 V | 0.45 V | 0.5 V | 0.4 V | 2.8 V |
| Output Voltage | 428 mV | 120 mV | 500 mV | 212 mV | 1.17 V |
| Current Consumption | 16.3 μA | 32.4 nA | 64 nA | 480 nA | 78 nA |
| Line regulation | 1 mV/V | 1.2 mV/V | 10 mV/V | 2 mV/V | 0.59 mV/V |

$^{(T)}$: trimmed. $^{(UT)}$: untrimmed. $^{1}$: 3σ.

## 4. Conclusions

An ultra-low power, high accuracy BGR designed for implantable medical electronics is presented in this paper. To solve the conflict between low power and high accuracy, an on-off bandgap combined with sample-and-hold switched-RC filter is developed. A higher working current is allowed to alleviate $V_{BE}$ spread, which directly causes error to output voltage, but also keeps the average power consumption as low as 220 nW with the voltage supply of 2.8 V. Furthermore, to improve the accuracy ulteriorly, the error brought by the Opamp offset is eliminated by applying correlated double sampling strategy. As a result, the measured voltage accuracy of 0.69% is achieved without trimming, which is adequate for most implanted medical electronics. The circuit shows a line regulation of 0.59 mV/V in the supply voltage range of 1.8–3.2 V and a TC of 19.6 ppm/°C in the temperature ranging from −20 to 80 °C. The proposed BGR circuit meets all the requirements of implantable medical electronics. It is very suitable for application in biomedical systems.

**Author Contributions:** Conceptualization, J.X. and R.Z.; investigation, M.W. and S.W.; writing—original draft preparation, J.X. and Y.W.; writing—review and editing, G.Z. and C.-F.Y.; project administration, R.Z.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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