Shunt Active Power Filter: A Review on Phase Synchronization Control Techniques

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Abstract: Owing to the destructive impacts of harmonic currents, the topic of reducing their impacts on power system has attracted tremendous research interests. In this regard, a shunt active power filter (SAPF) is recognized to be the most reliable instrument. It performs by first detecting the harmonic currents that are present in a harmonic-contaminated power system, and subsequently generates and injects corrective mitigation current back into the power system to cancel out all the detected harmonic currents. This means that other than the ability to generate corrective mitigation current itself, it is actually more important to make sure that the SAPF is able to operate in phase with the operating power system, so that the mitigation current can correctly be injected. Hence, proper synchronization technique needs to be integrated when designing the control algorithms of SAPF. This paper critically discusses and analyzes various types of existing phase synchronization techniques which have been applied to manage operation of SAPF; in terms of features, working principle, implementation and performance. The analysis provided can potentially serve as a guideline and provision of information on selecting the most suitable technique for synchronizing SAPF with the connected power system.

Keywords: active filter; control technique; harmonics mitigation; phase synchronization; power quality issues

1. Introduction

Broad utilizations of nonlinear loads have caused alarming power quality issues, notably current harmonic contamination to the electrical power system. Generally, the injected harmonic currents deteriorate power quality by increasing total harmonic distortion (THD) of a power system. Moreover, they are also the main culprit to reduction of overall power system efficiency (indicated by low power factor), overheating of equipment, failure of sensitive devices, and even blown capacitor [1–3]. As a result, it is obligatory to limit harmonic contents in power system and maintain it within an acceptable level.

In conjunction with the mitigation efforts, IEEE standard 512-1992 has been formulated (presently revised as IEEE standard 519-2014 [4]) to strictly limit level of harmonic distortion within 5% THD and also harmonic filters are installed in the polluted power system to minimize power quality issues due to harmonic currents. Conventionally, the harmonic filters are developed based on passive elements

such as inductors and capacitors to deal with specific harmonic issues (i.e., they only have fixed mitigation ability) [5]. However, due to their inherent weaknesses of inflexibility, instability, and large size, they are soon replaced by active power filters (APFs) which offer versatile solution to harmonic problems [6–8].

Owing to their superior mitigation capabilities, technology of APF continues to advance. Presently, APFs are available in a number of forms which can be classified into several distinct categories. As reported in [6–8], APF can be classified according to (1) the ways it is connected to the power system (i.e., series or shunt), (2) power rating (i.e., low-power, medium-power or high-power), (3) types of power converter employed (i.e., current-source or voltage-source converters), (4) circuit topology of the power converter employed (such as inverter, switch-capacitor, or hybrid-topology), (5) power system characteristic (i.e., two-wire for single-phase system, three-wire or four-wire for three-phase system), and (6) the targeted mitigation variables (such as current/voltage harmonics, reactive power, power factor, balancing of three-phase system, or any combinations of them). Nevertheless, as can be concluded from the literature [6], to deal with harmonic currents issues, shunt-typed active power filter (SAPF) is revealed to be most reliable.

A typical SAPF is able to measure degree of harmonic current contamination of a power system and based on that measured data, it generates and injects corrective mitigation currents back into the polluted power system to directly cancel out harmonic currents, thus minimizing severity of harmonic current contamination. This is attainable when all the control techniques applied in its control system are functioning as desired. Nonetheless, many technical issues and challenges remained to be addressed for effective installation of SAPF into the polluted power system. One of the most critical issues is synchronization of the SAPF, where its generated output voltage needs to be properly synchronized with the grid voltage to achieve stable and continuous mitigation operation. The problems will be increasingly difficult when the grid voltage is subjected to faults such as harmonic contamination and unbalanced faults. Failure to synchronize leads to incorrect mitigation and may eventually worsen the harmonic issues which are supposed to be reduced.

Phase synchronization in this aspect can be regarded as a process to minimize phase differences between the output voltage of SAPF and the connected grid voltage and at the same time matching their operating frequency. This process has to be achieved before connecting the SAPF to the designated power system, thereby allowing the power system and the synchronized SAPF to work together. As reported in [9,10], an effective synchronization technique should be able to track phase angle of the grid voltage, detect frequency variations, filter out higher order harmonics, and respond to variations in the grid voltage.

In regard to the difficulties and problems in phase synchronization, various techniques with unique merits have been proposed for synchronizing grid-tied converters. As reported in [10,11], grid-tied devices that are required to be precisely synchronized with the grid voltage can distinctively be classified into four groups based on their intended applications: (1) Renewable energy system (RES); (2) flexible ac transmission system (FACTS); (3) custom power system (CUPS); and (4) loads. It is worth noting that SAPF falls under the group of CUPS. Published literature reviews on synchronization techniques exist but most of them focus on the application of RES, such as in [9,10]. Meanwhile, specifically on the topic of SAPF, published reviews on its control techniques are also available such as in [12–15]. However, the trend has thus far focused on the three main control processes of its control system, i.e., reference current generation, voltage regulation, and current control. The methodology and behavior of its synchronization process have not yet been thoroughly discussed. Hence, it clearly indicates that there is a lack of published material that provides details regarded to the implementation of synchronization techniques for SAPF application. This study will bridge such research gap.

In this study, a comprehensive review focusing on features, working principle, performance, and implementation of phase synchronization technique in the controller of SAPF, is presented. The findings of this study should be able to help researchers in selecting the most suitable synchronization technique for their respective SAPF and may eventually inspire them to generate fresh

ideas in enhancing the synchronization process of SAPF. The organization of this manuscript is as follow: Section 2 presents working principle of a typical SAPF and its control system; Section 3 provides and critically discusses the details of various synchronization techniques proposed to date for grid synchronization of SAPF; Section 4 provides comparisons and analyses of the discussed techniques; and Section 5 concludes the review.

2. Shunt Active Power Filter: Working Principle and Control Scheme

Figure 1 shows the overall circuit configuration of a typical voltage source inverter (VSI)-based SAPF (used as main example in this manuscript) and illustrates the four main control algorithms that constituted its control system. Generally, SAPF is connected to a harmonic-polluted power system at point of common coupling (PCC), between voltage supply and harmonic-producing load (or more commonly known as nonlinear load). In the literature, the harmonic-producing load is commonly developed by using an uncontrolled bridge rectifier which is further connected to a combination of resistor (R), inductor (L), and capacitor (C) elements [16,17].
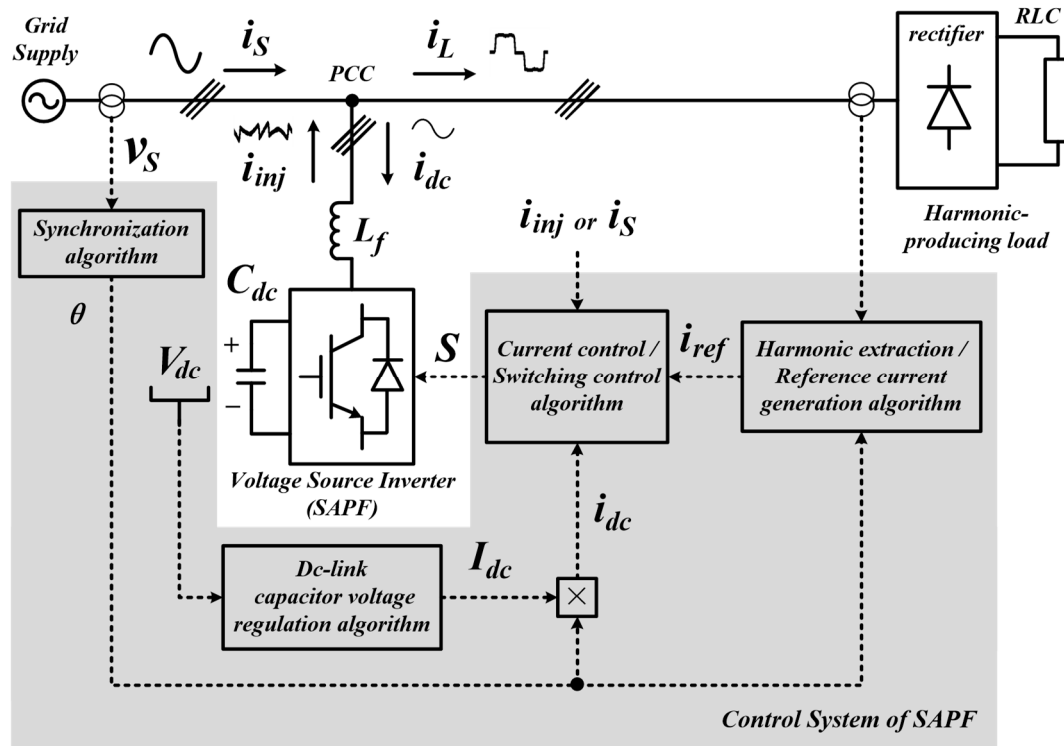

Figure 1. Typical power circuits connection of voltage source inverter (VSI)-based shunt active power filter (SAPF) and the associated control algorithms in its control system.

The structure of SAPF can distinctively be separated into two parts: power circuits which comprises of power semiconductor switches, capacitors, inductors, power diodes (in some SAPF topologies); and a control system that is designed to control switching operation of the switches.

The operation of SAPF is rather simple. One can easily grasp the basic idea by looking at the current flow in a SAPF-installed power system. Referring to Figure 1 and by applying Kirchhoff's current law (KCL) at PCC, current flow in a harmonic-polluted power system before connecting a SAPF can be written as

$$i_S = i_L = i_{1L} + i_H \tag{1}$$

where i_S indicates the source current, and i_L is the load current which potentially contained i_{1L} (fundamental current) and i_H (harmonic current existed due to connection of harmonic-producing

loads). It is worth noting that i_S at this moment is distorted and not working in-phase with the source voltage v_S due to the impact of i_H. Hence, the main purpose of installing a SAPF is to eliminate i_H.

After installing SAPF at PCC, two additional current flows are introduced into the power system (as illustrated in Figure 1). First, to cancel out i_H, mitigation current (named as injection current i_{inj} in this manuscript) is injected by the SAPF into the power system via PCC. The injected mitigation current has magnitude which is equal and phase which is opposite to that of i_H. Second, a small amount of current (named as dc-link charging current i_{dc}) is utilized by the SAPF to maintain a constant dc-link voltage V_{dc} (voltage across its dc-link capacitor C_{dc}) at desired level. In this manner, its switching losses are regulated and thus ensuring continuous and stable operation of SAPF. In terms of mathematical expression, Equation (1) can be re-written according to KCL as

$$i_S = [i_{1L} + i_H] - i_{inj} + i_{dc}. \tag{2}$$

Theoretically, the magnitude of the generated i_{inj} is influenced by the voltage level across the dc-link capacitor. When voltage across the dc-link capacitor has been reached and is continuously maintained at the desired level, the generated i_{inj} will be exactly equal to i_H where they will cancel out each other. As a result, Equation (2) can further be simplified as

$$i_S = i_{1L} + i_{dc}. \tag{3}$$

At this moment, with removal of i_H, i_S regained its sinusoidal characteristic with fundamental frequency and work in-phase with v_S.

To better demonstrate operation of SAPF, Figure 2 is provided to show an example waveform consisting of source voltage v_S, load current i_L, injection current i_{inj}, and source current i_S, that can be observed in a harmonic-polluted power system with a SAPF installed. Note that the example provided is considering a balanced-sinusoidal source voltage and an inductive-typed nonlinear load (comprises of a three-phase uncontrolled bridge rectifier feeding a RL element). The use of other scenarios of source voltage and types of nonlinear loads may result in different shape of waveforms.
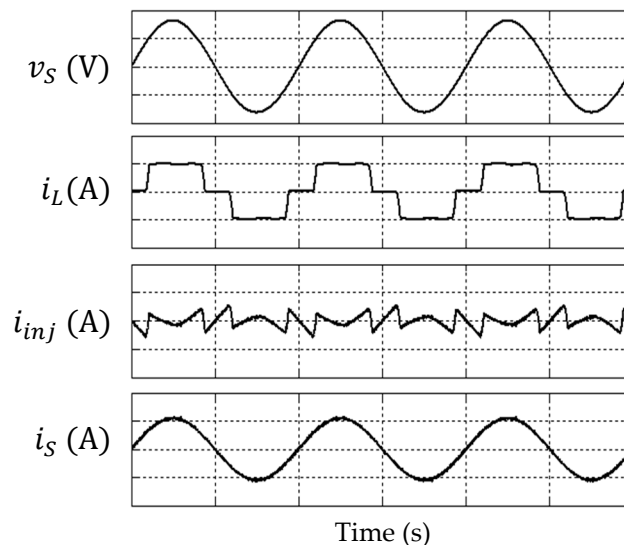

Figure 2. Theoretical voltage and current waveforms showing the condition of power system with a SAPF installed.

To effectively control the operation of SAPF, its control system must be designed with four types of control algorithms, each with a specific function listed as follows:

(1)　Harmonic Extraction Algorithm. The main function of this algorithm is to extract harmonic information from a harmonic-polluted power system and applied the extracted information

to form a reference current signal i_{ref}. In this aspect, the distorted load current signal i_L is processed in a way that allows its harmonic i_H and fundamental i_{1L} elements to be separated. After separating the elements, i_{ref} can be derived by using either the harmonic or fundamental elements, each having its own derivation setting. Note that quality of the reference current signal will mainly determine how well the SAPF is going to work, thus it must be generated in a quick and accurate manner. This algorithm is also referred as reference current generation algorithm in some literature, such as in [18,19] due to the reason that reference current is being generated as the final output of this algorithm. Few examples of commonly applied techniques for this algorithm include synchronous reference frame (SRF) or *dq* theory [20–22], instantaneous power *pq* theory [23–25], fast Fourier transform (FFT) [26,27], discrete Fourier transform (DFT) [28,29] and artificial neural network (ANN) [30–32].

(2) Synchronization Algorithm. The main function of this algorithm is to track angular position of source voltage signal v_S and subsequently generate a phase synchronization angle θ to match the phase of the generated i_{ref} with the phase of the operating power system. Many harmonic extraction algorithms do not possess a phase tracking feature and are fully dependent on an explicit synchronization algorithm to provide them with an effective synchronization angle. Nevertheless, there are some harmonic extraction algorithms that are inherited with phase tracking ability, for example, the algorithm designed based on instantaneous power *pq* theory technique [25,33]. In this case, an explicit synchronization algorithm can be omitted. Further details on the available techniques for this algorithm are presented in the next section.

(3) DC-link Capacitor Voltage Regulation Algorithm. The main function of this algorithm is to estimate the amount of dc-link charging current i_{dc} needed by the SAPF to constantly maintain dc-link voltage V_{dc} at a desired level. This algorithm continuously compares the measured V_{dc} with a predetermined set-point value and minimizes the resulted error by using either proportional-integral (PI) [34–36] or fuzzy logic control (FLC) [37–39] techniques, via a voltage control loop. When the error between the measured V_{dc} and the predetermined set-point value has been minimized, the effective magnitude I_{dc} of i_{dc} will be generated. Subsequently, by utilizing the phase synchronization angle θ, i_{dc} can be coordinated in-phase with the operating power system.

(4) Current Control Algorithm. The main function of this algorithm is to convert i_{ref} delivered by harmonic extraction algorithm and i_{dc} delivered by dc-link capacitor voltage regulation algorithm into gate switching pulses S via a pulse-width modulation process, while ensuring that the feedback signal i_{inj} or i_S is able to track i_{ref} via a current control loop. This algorithm is also commonly referred as switching algorithm due to its function in generating gate switching pulses. Few examples of commonly applied techniques for this algorithm include hysteresis control [40–43], sinusoidal pulse-width modulation (SPWM) [44–46] and space vector PWM (SVPWM) [47–50].

The four control algorithms are linked to one another systematically, and they perform in a closed-loop manner in which the actual output (it could be either i_{inj} or i_S) is monitored and fed back to be compared with the desired i_{ref} until the monitored output achieve its desired response. Even if subjected to disturbances such as dynamic conditions, the algorithms have been practically proven to be able to respond quickly to once again bring the monitored output back to its desired form.

3. Phase Synchronization Techniques

This section discusses about the phase synchronization techniques which have so far been integrated in the control system of SAPF. It includes the two common techniques in the literature namely zero-crossing detection (ZCD) [19,51,52] and phase-locked loop (PLL) [53–55], and the more recent techniques such as artificial neural-network (ANN) or adaptive linear neuron (ADALINE) [56–58], fundamental component extraction [59,60], and unit vector generation [61–63]. In this manuscript, the synchronization techniques are classified according to the intended application of SAPF, i.e., either for single-phase or three-phase power system, as illustrated in Figure 3. Over the years, works on

SAPF for three-phase system are more popular compared to single-phase system particularly due to wider applications of power electronics devices and nonlinear loads in three-phase environment [64–66]. However, to avoid redundancy, this manuscript will examine the synchronization technique itself and subsequently, suitability of each technique for single-phase and three-phase system applications will be highlighted.
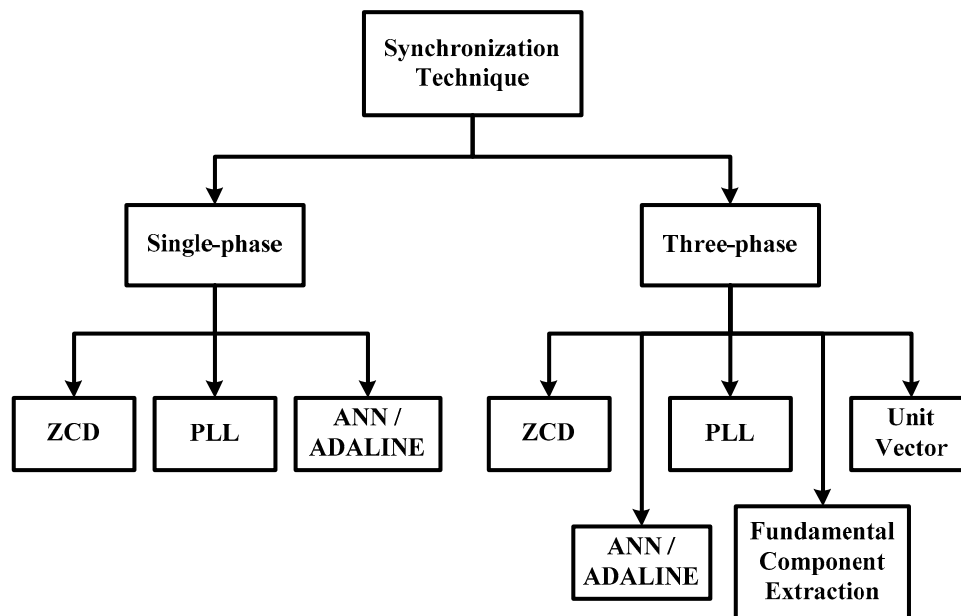

Figure 3. Overview of synchronization techniques applied to SAPF. ZCD: zero-crossing detection; PLL: phase-locked loop; ANN: artificial neural network; ADALINE: adaptive linear neuron.

3.1. Zero-Crossing Detection (ZCD) Technique

Zero-crossing detection (ZCD) technique is the simplest and one of the early approaches proposed for synchronization purposes [19,51,52]. According to ZCD technique, a circuit is designed to detect zero-crossing point of ac voltage and generate a pulse accordingly [51]. It offers the best advantage in terms of implementation requirements, but poor performances are reported in is application especially when the source voltage is subjected to noises and harmonics [67]. In such cases, multiple zero crossings can occur and this makes difficult for the zero-crossing detector to detect the original zero crossing, thus increases the possibility of inaccurate detection. Nonetheless, some form of filtering can be applied to reduce the distortion before feeding it to the zero-crossing detector [68]. However, pre-filtering may introduce phase lead or lag into the filtered waveform, and this issue is quite difficult to avoid as ZCD is an analog-based technique. Hence, once again its accuracy is degraded. Moreover, zero crossing point can only be detected at every half-cycle of utility fundamental frequency, thus causes poor dynamic performance [69]. Furthermore, this technique requires development of additional hardware circuit (one for each operating phase) which increases the size and cost. For instance, in [51], a ZCD hardware circuit is built to generate an initiating pulse to the controller of SAPF (developed on a digital signal processor (DSP) board) when a zero-crossing voltage is detected at the PCC. The initiating pulse serves as a switch that initiates operation of the controller. This technique is applicable for both single-phase [51] and three-phase system [19]. Nevertheless, owing to its weaknesses, this technique is still the least preferred to be implemented for SAPF's applications, as compared to the others available techniques.

3.2. Phase-Locked Loop (PLL) Technique

Among the five techniques presented in this manuscript, phase-locked loop (PLL) technique is the most recognized and commonly applied approach, due to its uncomplicated control structure,

and effectiveness in handling various grid conditions. PLL is actually an old technology which appeared in the literature in the 1930s, and it has successfully been applied over the past decades in various areas, such as in communication, control systems, and instrumentation [70,71]. The basic concept of PLL has been revealed in [72]. Its structure contains three basic functional blocks known as phase detector (PD), loop filter (LF), and voltage-controlled oscillator (VCO), as illustrated in Figure 4. In a closed-loop control operation, PD will first compare the two input signals (a reference phase signal θ_{ref} and a feedback signal θ) and generate a phase error signal $\Delta\theta$. The generated error is then filtered by LF (typically a low-pass filter (LPF)) which suppresses noise and other high-frequency elements from PD. The filtered signal is subsequently processed by VCO to generate an updated output phase θ which is then feedback to the PD. As the looping process continues, the error generated will continuously be reduced and when it reaches zero value, the output phase will be locked and matches the desired reference phase signal θ_{ref}.
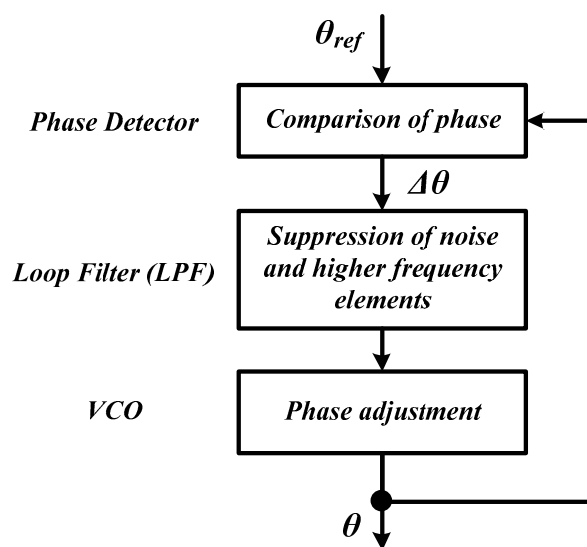
Figure 4. Control structure of a basic phase-locked loop (PLL) technique [72]. VCO: voltage-controlled oscillator.

Subsequently, for the application of SAPF, the basic PLL has further been enhanced as synchronous reference frame (SRF)-based PLL (or simply SRF-PLL) [53–55]. SRF-PLL technique has successfully been applied in both single-phase [55,73,74] and three-phase systems [10,53,54,73]. Figure 5 shows the basic control structure of SRF-PLL technique. As can be seen from Figures 4 and 5, the obvious difference between SRF-PLL and the basic PLL techniques is on the implementation approach for the PD block. As its name implies, SRF-PLL is a technique that utilizes SRF theory for the implementation of its PD block, in which three-phase voltage in *abc* natural reference frame is first transformed into two-phase $\alpha\beta$ stationary frame (by means of Clarke-transformation) and then into *dq* rotating reference frame (by means of Park-transformation), as shown in Equations (4) and (5), respectively. Note that constant *k* refers to sampling rate. A proportional-integral (PI) is then applied to manipulate the resulting *q* variable and eventually the angular frequency ω of the utility will be generated as the output. The utility phase angle θ can be obtained by integrating the angular frequency, and the looping process continues by feeding the phase angle back to the $\alpha\beta - dq$ transformation block until the phase angle is locked at a fixed value.

$$\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa}(k) \\ v_{Sb}(k) \\ v_{Sc}(k) \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} v_d(k) \\ v_q(k) \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} \tag{5}$$

SRF-PLL technique is initially developed for the application in three-phase system. However, with a little modification on the initial signal processing approach, it can also be used in single-phase system. For single-phase application, there is a need to transform single-phase signal to $\alpha\beta$ stationary frame by means of other approach due to the facts that Clarke-transformation (the usual transformation approach) is not applicable in single-phase system. One interesting approach is revealed in [55,73,74] where the single-phase signal is directly treated as α frame signal and meanwhile β frame signal is created by introducing a phase delay of $\pi/2$ to the actual single-phase signal (as illustrated in Figure 5b). The subsequent phase locking processes for single-phase SRF-PLL is basically similar to that of three-phase SRF-PLL.
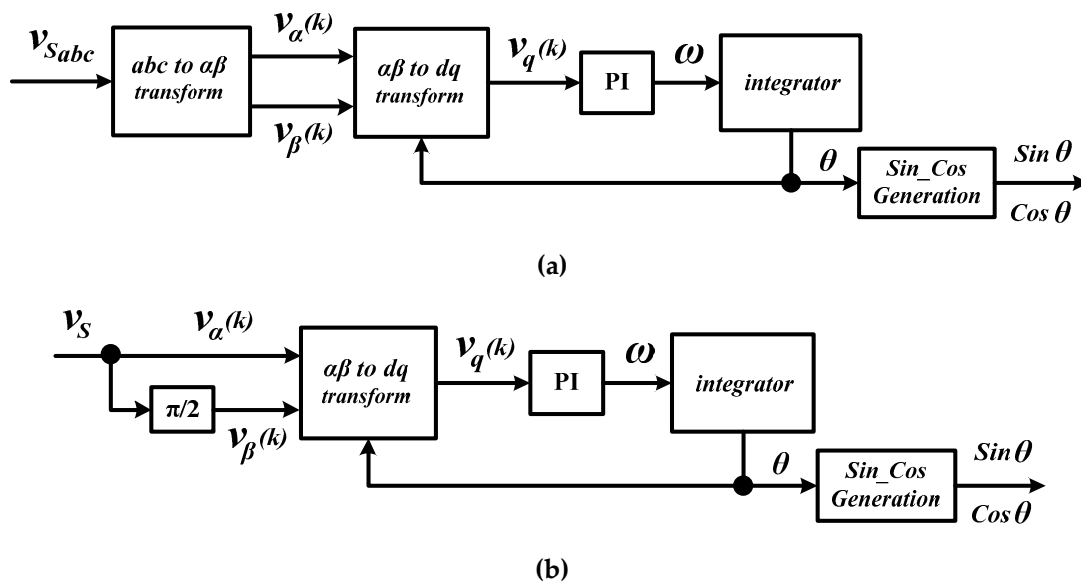

Figure 5. Control structure of synchronous reference frame (SRF)-PLL technique for (**a**) three-phase [10,53,54,73] and (**b**) single-phase [55,73,74] applications.

The main advantage of SRF-PLL technique is that it allows accurate and quick tracking of utility frequency and phase angle for the case when the source voltage is free from any distortions and unbalances. Unfortunately, it fails to work appropriately when the source voltage is unbalanced (for a three-phase system) and/or distorted due to presence of harmonics. One good way to alleviate this inherent issue is by applying additional low-pass filter (LPF) in the control loop after the $\alpha\beta - dq$ transformation block [75]. However, there is a need to carefully match the order and cutting frequency of the LPF via heuristic manner, to provide satisfactory compromise between its distortion rejection performance and speed. The good news is that the traditional SRF-PLL has been improved as self-tuning filter (STF)-based PLL (or simply STF-PLL) [55] and decoupled double (DD) SRF-PLL (or simply DDSRF-PLL) [53] to ensure its effectiveness when it is required to work under unbalanced and/or distorted utility grid.

Basically, STF-PLL works in a similar manner to that of a traditional SRF-PLL. However, its input signal in $\alpha\beta$ frame will be pre-filtered by a STF which suppresses noise and other high-frequency elements before transforming into dq rotating reference frame. This approach allows distortion-free signal to be processed in the phase-locking loop, thus ensuring accurate detection of utility phase angle

and frequency. The basic structure of a STF is shown in Figure 6 and meanwhile its working principle can be summarized as the following approach:

$$\begin{bmatrix} x_{\alpha(fund)}(s) \\ x_{\beta(fund)}(s) \end{bmatrix} = \frac{K}{s} \begin{bmatrix} x_\alpha(s) - x_{\alpha(fund)}(s) \\ x_\beta(s) - x_{\beta(fund)}(s) \end{bmatrix} + \frac{2\pi f_c}{s} \begin{bmatrix} -x_{\beta(fund)}(s) \\ x_{\alpha(fund)}(s) \end{bmatrix} \tag{6}$$

where $x_{\alpha\beta(fund)}(s)$ is the extracted distortion-free (fundamental) element of input signal in $\alpha\beta$ frame, $x_{\alpha\beta}(s)$ is the actual input signal in $\alpha\beta$ frame, K is a constant gain parameter and f_c is the cutting frequency. Despite its strong points, this technique has one disadvantage where capability of the applied STF is dependent on the selection of its gain parameter. An analysis to study the effect of the gain parameter on the performance of STF has been reported in [59,76]. From the analysis, as an overall, a smaller gain value improves accuracy of STF but at the same time reduces its dynamic responses. The opposite effect holds if a higher gain value is applied. Hence, for a balance between accuracy and speed, the gain value should carefully be selected.
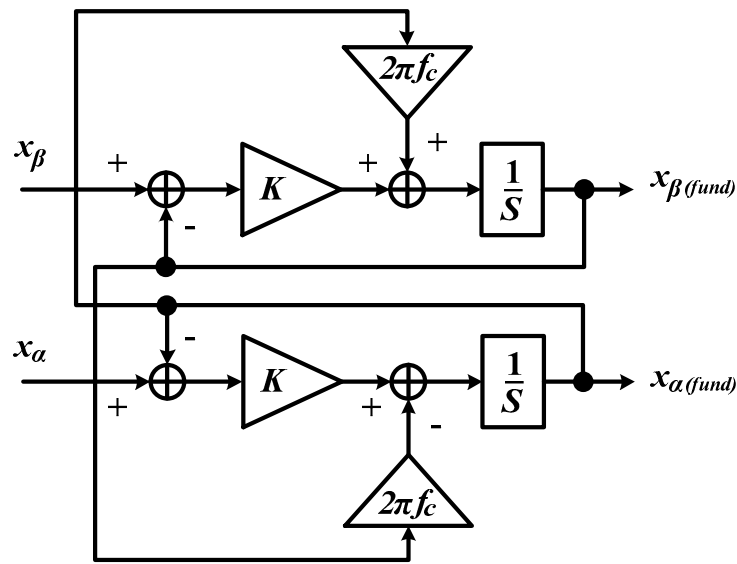

Figure 6. Basic structure of self-tuning filter tuned at specific f_c [76,77].

On the other hand, in DDSRF-PLL, instead of applying a STF to suppress high-frequency elements contained in the distorted input signal, the positive-sequence and negative-sequence elements existed due to unbalanced and distorted source voltage conditions are distinctively separated and transformed into double SRF loop, and a decoupling network is then integrated to extract the positive-sequence element with fundamental-frequency before applying it in the phase-locking loop. A block diagram of the decoupling network applied in DDSRF-PLL technique is shown in Figure 7 to illustrate the aforementioned process.

As presented in Figure 7, the initial processing stage of this technique is similar to the conventional PLL technique shown in Figure 5 where it involves signal transformation of three-phase voltage in *abc* natural reference frame into two-phase $\alpha\beta$ stationary frame and then into *dq* rotating reference frame. However, in *dq* rotating reference frame, the positive-sequence v_{Sdq}^{+1} and negative-sequence v_{Sdq}^{-1} elements are separated. Subsequently, fundamental-frequency elements (positive-sequence $\bar{v}_{Sdq}^{+1}$ and negative-sequence $\bar{v}_{Sdq}^{-1}$) are extracted from each decoupling cell. The extracted positive-sequence element with fundamental-frequency will then be applied in phase-locking loop until the desired phase angle θ is generated. Although this enhanced technique is revealed to completely eliminate detection error of the traditional SRF-PLL and precisely worked even under the influence of unbalanced and distorted utility conditions, its detection process is rather complex due to the necessity of an additional SRF loop.
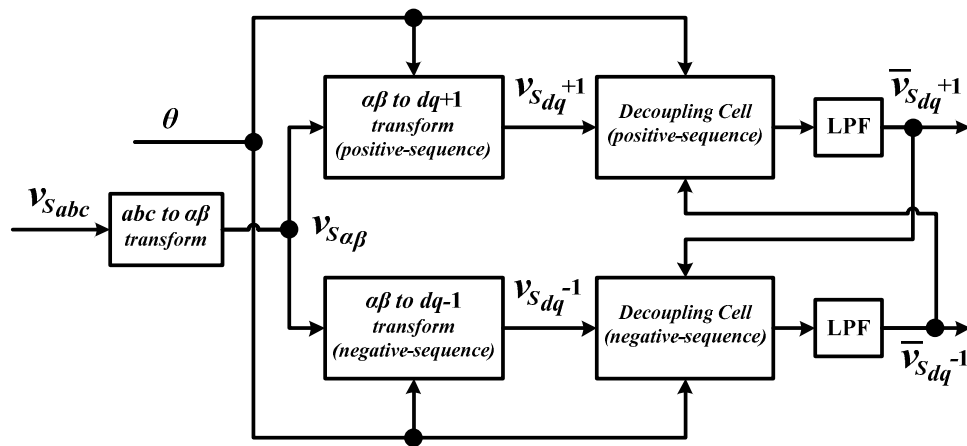
Figure 7. Block diagram of decoupling network in decoupled double SRF (DDSRF)-PLL [53].

Other than different modifications of conventional PLL techniques, another phase-tracking technique which can provide comparable performance to a robust PLL has been reported in [78–80]. The method is named as D-estimation method. It is not based on a conventional PLL approach, but instead it works based on a simple filtering approach named D-filter [78]. It can actually provide instant estimation of phase and frequency similar to that of a PLL. Note that this method is not yet applied in SAPF applications. However, it has been experimentally verified to be stable and robust even operating under the influence of harmonics distortion and contaminated noise [78–80]. This is an important feature of phase-tracking/synchronization technique that make it suitable for SAPF applications. Hence, study on the adaptability of D-estimation method in SAPF applications can be a potential research for future work.

3.3. Adaptive Linear Neuron (ADALINE) Technique

One recent synchronization technique is developed based on adaptive linear neuron (ADALINE) concept. Originally, the ADALINE technique is introduced for the purpose of harmonic extraction or generating reference current [30,81,82]. However, with appropriate consideration, the same ADALINE technique for harmonic extraction has been reported to be applied for synchronizing purposes as well. In this regard, a technique that combined both the ADALINEs function which is named as unified ADALINEs is proposed [58]. Figure 8 shows control structure of ADALINE-based synchronization technique.

In operation, the source voltage $v_S(k)$ is first measured and compared with an estimated voltage $v_{Fund\_est}(k)$. Note that constant k refers to the sampling rate, for digital implementation. The resulting error $e(k)$ is processed by a weight updating algorithm as shown in Equation (7) to update the weight $\overline{W}$ or the amplitude (coefficient) W_{11} and W_{21} of sine $sin(k\omega\Delta t)$ and cosine $cos(k\omega\Delta t)$ vectors.

$$W(k+1) = W(k) + \frac{\alpha e(k)Y(k)}{Y(k)^T Y(k)} \qquad (7)$$

where,

$W = \begin{bmatrix} W_{11} \\ W_{21} \end{bmatrix}$ is the weight factor,

$Y = \begin{bmatrix} sin(k\omega\Delta t) \\ cos(k\omega\Delta t) \end{bmatrix}$ is the fundamental sine and cosine components,

$e(k) = v_S(k) - v_{Fund\_est}(k)$ is the error between the measured and estimated voltage signal, and α is the learning rate.
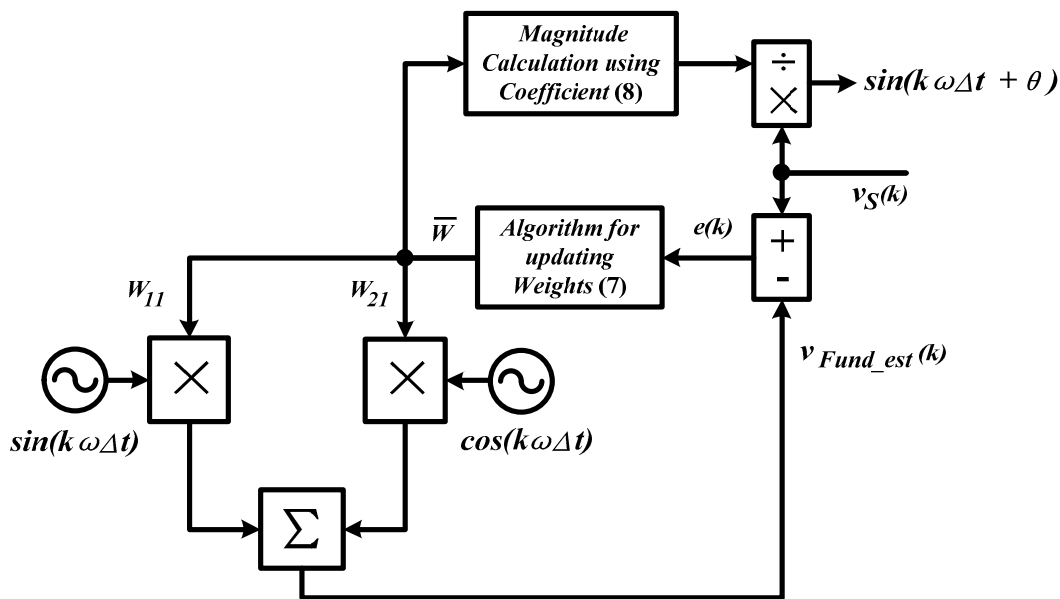
Figure 8. Control structure of adaptive linear neuron (ADALINE)-based synchronization technique [58].

At the same time, W_{11} and W_{21} will be utilized to compute instantaneous magnitude $V_{Fund\_mag}(k)$ of $v_S(k)$ according to the following approach.

$$V_{Fund\_mag}(k) = \sqrt{W_{11}^2 + W_{21}^2}. \tag{8}$$

The iteration is repeated until $v_{Fund\_est}(k) = v_S(k)$. At this moment, the effective magnitude of $v_S(k)$ is produced and eventually being divided from the measured $v_S(k)$, thus generating the desired synchronization signal $sin(k\omega\Delta t + \theta)$. It is worth noting that the desired synchronization signal generated in this manner is unity representation of the instantaneous source voltage.

This synchronization technique has been verified to work effectively for both single-phase [56,57] and three-phase system [58], provided that the source voltage applied is balanced and sinusoidal. It is worth noting that a single unit of ADALINE-based synchronization technique (as illustrated in Figure 8) is only capable of generating synchronization signal for one single operating phase. Hence, for a three-phase system, it would obviously require three similar units (one for each operating phase). One main disadvantage of this technique is that it cannot work appropriately when the source voltage is subjected to harmonic distortion and/or unbalance condition. Another inherent weakness of this technique is that its effectiveness is strictly dependent on its learning rate α value, which is normally obtained via heuristic approach.

3.4. Fundamental Component Extraction Technique

Another recent alternative technique to grid-synchronization of SAPF is the fundamental component extraction technique where the target is to extract fundamental component (sinusoidal characteristic) of the source voltage with unity magnitude. In other words, the end product of this technique is actually similar to the ADALINE-based technique discussed previously in Section 3.3. However, in comparison to the ADALINE-based technique, this technique is designed with one important advantage where it is effective even when the source voltage is distorted and/or unbalanced, as reported in [59,60]. This is simply because the technique is integrated with a self-tuning filter (STF) [76,77,83] which has the ability to effectively filter out any distortion from a distorted signal. Figure 9 shows the control structure of fundamental component extraction technique with an integrated STF.
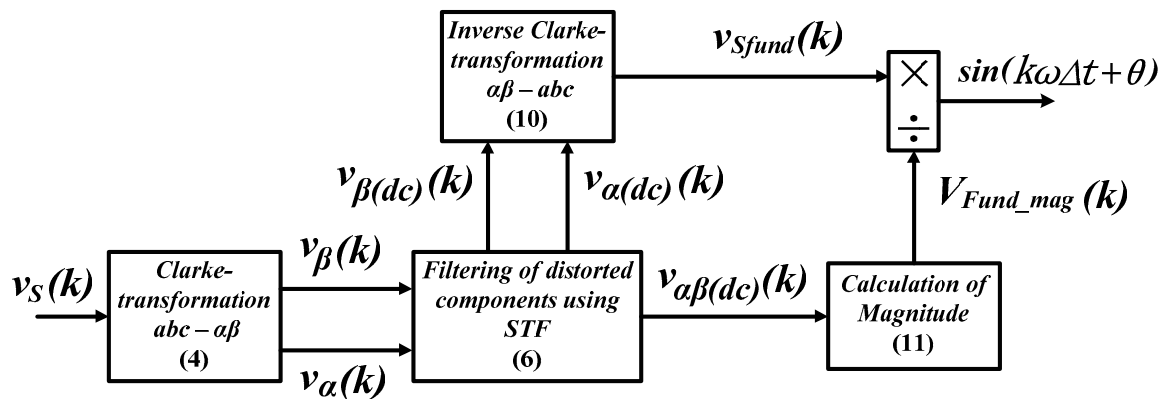
Figure 9. Control structure of fundamental component extraction technique with an integrated self-tuning filter (STF) [59,60].

In operation, the desired synchronization signal $sin(k\omega\Delta t + \theta)$ is generated according to three consecutive processes listed as follow:

1. Extraction of fundamental (sinusoidal characteristic) source voltage $v_{Sfund}(k)$ from the measured source voltage $v_S(k)$. In the first stage, the extraction process is conducted in $\alpha\beta$-domain where a Clarke-transformation ($abc - \alpha\beta$ transformation) is applied according to Equation (4). In $\alpha\beta$-domain, source voltage which is subjected to distortion can be expressed as

$$\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} = \begin{bmatrix} v_{\alpha(dc)}(k) + v_{\alpha(ac)}(k) \\ v_{\beta(dc)}(k) + v_{\beta(ac)}(k) \end{bmatrix} \tag{9}$$

where $v_{\alpha(dc)}(k)$ is the fundamental component and $v_{\alpha(ac)}(k)$ is distorted component of source voltage in α domain, respectively. Similar relation valid for source voltage in β domain, $v_{\beta(dc)}(k)$ and $v_{\beta(ac)}(k)$. Here, a STF (as in Equation (6)) is applied to extract $v_{\alpha(dc)}(k)$ and $v_{\beta(dc)}(k)$ which is subsequently converted into a pure sinusoidal signal $v_{Sfund}(k)$ by means of inverse Clarke-transformation ($\alpha\beta - abc$ transformation), as in Equation (10). Note that, the application of STF is only needed when the source voltage is subjected to any distortion. In the case where the source voltage is ideal (balanced-sinusoidal), STF can actually be omitted to reduce structure complexity.

$$\begin{bmatrix} v_{Sfund,\, a}(k) \\ v_{Sfund,\, b}(k) \\ v_{Sfund,\, c}(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{\alpha(dc)}(k) \\ v_{\beta(dc)}(k) \end{bmatrix}. \tag{10}$$

2. Magnitude $V_{Fund\_mag}(k)$ calculation by using the extracted fundamental voltage component ($v_{\alpha(dc)}(k)$ and $v_{\beta(dc)}(k)$). In this stage, the fundamental magnitude of source voltage is computed as follow

$$V_{Fund\_mag}(k) = \sqrt{v_{\alpha(dc)}(k)^2 + v_{\beta(dc)}(k)^2}. \tag{11}$$

3. Direct magnitude $V_{Fund\_mag}(k)$ division from $v_{Sfund}(k)$ to obtain its unity form. In the final stage, the desired synchronization signal $sin(k\omega\Delta t + \theta)$ is obtained as follow

$$sin(k\omega\Delta t + \theta) = \frac{v_{Sfund}(k)}{V_{Fund\_mag}(k)} \tag{12}$$

This technique has only been implemented in three-phase system [59,60]. Hence, further researches to study about its adaptability in single-phase system can be interesting. Despite its strong points,

this technique has one disadvantage where capability of the applied STF is dependent on the selection of its gain parameter, as clearly been mentioned in Section 3.2. To date, there is still no exact procedure to optimally tune the gain value, and it is mostly performed heuristically which can be time-consuming.

3.5. Unit Vector Generation Technique

Another interesting synchronization technique is unit vector generation technique. As its name indicates, its working principle involves generation of unit vectors (consisting of sine and cosine functions) from the measured source voltage. The control structure of unit vector synchronization technique is illustrated in Figure 10. Similar to fundamental component extraction technique (as described in Section 3.4), the main operation of this technique occurred in $\alpha\beta$ domain which requires a domain transformation from three-phase *abc* domain to two-phase $\alpha\beta$ domain by using a Clarke-transformation (as shown in Equation (4)).
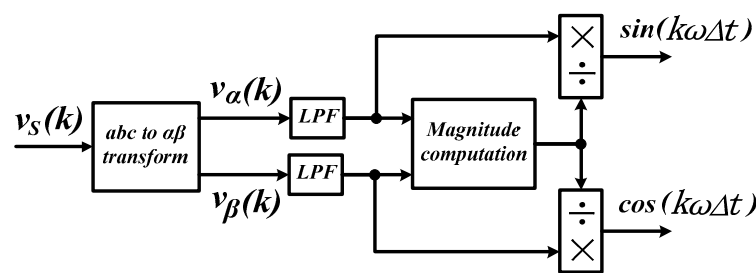

Figure 10. Control structure of unit vector synchronization technique [61–63].

In $\alpha\beta$ domain, the signal in α coordinate $v_\alpha(k)$ represents a sine function and meanwhile the signal in β coordinate $v_\beta(k)$ represents a cosine function. Note that a low-pass filter (LPF) with cutting frequency of 50 Hz (equal to fundamental frequency of the measured source voltage) is applied to filter out higher order harmonics which are normally present in the source voltage [61]. Subsequently, the desired sine and cosine function for synchronization purposes ($sin(k\omega\Delta t)$ and $cos(k\omega\Delta t)$) are generated according to the following approach:

$$sin(k\omega\Delta t) = \frac{v_\alpha(k)}{\sqrt{v_\alpha(k)^2 + v_\beta(k)^2}} \tag{13}$$

and

$$cos(k\omega\Delta t) = \frac{v_\beta(k)}{\sqrt{v_\alpha(k)^2 + v_\beta(k)^2}} \tag{14}$$

where $\sqrt{v_\alpha(k)^2 + v_\beta(k)^2}$ is the computed magnitude of $v_\alpha(k)$ and $v_\beta(k)$.

This technique has only been applied in three-phase system which is supplied by a balanced and sinusoidal source voltage, where it has practically been proven to perform effectively [61,62]. In theory, LPF actually has the ability to filter out higher order harmonics, thus should be able to work appropriately when the source voltage is subjected to harmonic distortion. However, there is a lack of relevant simulation and experimental materials to justify this matter. Hence, further work regarding this matter can provide useful knowledge to the literature. One advantage of this technique is that its control structure is direct and straightforward without involving any complex computational process. Nonetheless, the use of LPF introduces delay and phase lag to the unit vector generation process which renders this technique less popular compared to the others.

4. Comparative Highlights on Phase Synchronization Techniques and Possible Future Works

Generally, the effectiveness of the applied phase synchronization techniques depend on their performance in distorted and unbalanced grid conditions, phase tracking accuracy, dynamic performance, noise immunity, and compatibility with other algorithms in the control system of SAPF. Besides that, control structure complexity and computational burden are also important criteria to be considered in selecting the most suitable phase synchronization techniques. To provide better understanding on the discussed topic and to ease the reading process, important features of each phase synchronization technique presented previously in Section 3 are highlighted in Table 1 including their strengths and weaknesses.

Regardless of evolution and advancement of synchronization techniques, synchronization issue remains a key issue in achieving effective and uninterrupted operation of SAPF in abnormal grid voltage conditions. One existing issue to be addressed is the lack of studies or works that report on the utilization of artificial intelligence (AI) technique for synchronization purposes. Most of the existing synchronization techniques are time-domain based which provides the common benefit of simplicity. Meanwhile, one most recent AI technique which applies the principle of neural network (ADALINE technique as discussed in Section 3.3), has yet been verified to be effective in distorted and unbalanced grid conditions. Moreover, the upcoming smart grid systems will definitely require intelligent technique for effective power flow management. Hence, there is a need for further studies to justify its capability in adverse grid conditions. Other than using AI technique by itself, studies can also be initiated for a hybrid of this technique with the other time-domain based techniques, and the studies should be supported with practical evaluation involving various adverse and dynamic grid conditions.

In most of the existing synchronization techniques discussed in this manuscript, whenever tuning process is involved, the tuning is performed heuristically. Although the synchronization techniques are able to perform satisfactorily by using heuristic tuning approaches, it is actually difficult to know whether their performances are optimal or not. Optimization approaches such as genetic algorithm (GA), particle swarm optimization (PSO), and ant colony optimization (ACO) are well-developed in the literature but none of them have been applied to optimize synchronization processes. Therefore, synchronization scheme with integration of optimization approaches should also be given attention in future studies.

Table 1. Feature comparison of the synchronization techniques discussed in this manuscript.

Synchronization Technique	Single Phase	Three Phase	Non-Ideal Grid	Strengths	Weaknesses
ZCD	Yes	Yes	No	Simplest control structure [9].	Require hardware circuit [51]. Sensitive to noise [9]. Poor dynamic response [69]. Poor performance when grid is subjected to harmonics [67].
SRF-PLL	Yes	Yes	No	Easy to implement [10]. Accurate synchronization under ideal grid conditions [10,54]. Most widely applied techniques [54].	PI controller needs to properly be tuned [35,84]. Unable to cope with distorted and unbalanced grid conditions [10,53,54].
STF-PLL	Yes	Yes	Yes	Suitable for highly distorted and unbalanced grid conditions [55].	PI controller needs to properly be tuned [35,84]. Gain parameter of STF needs to carefully be selected [59,76]. Integration of STF increases control complexity [55].
DDSRF-PLL	No	Yes	Yes	Suitable for highly distorted and unbalanced grid conditions [53].	PI controller needs to properly be tuned [35,84]. Additional SRF loops increases computational burden [53].
ADALINE	Yes	Yes	No	Low computational burden [58]. Can be applied for harmonic extraction purposes [58].	Learning rate needs to be properly tuned [30,58,81]. Unable to cope with distorted and unbalanced grid conditions [58].
Fundamental Component Extraction	No	Yes	Yes	Easy to implement [59,60]. Effective for highly distorted and unbalanced grid conditions [59,60] Can be applied for harmonic extraction purposes [59,60].	Gain parameter of STF needs to carefully be selected [59,76].
Unit Vector Generation	No	Yes	No	Simple control structure [61,62].	LPF needs to properly be tuned [85]. LPF imposes additional delay [61,62]. Unable to cope with distortion and unbalanced grid conditions [61,62].

5. Conclusions

This manuscript has thoroughly reviewed and discussed the state-of-the-art phase synchronization techniques for synchronizing SAPF with the power grid. A conceptual diagram which illustrate general working principle of SAPF and how synchronization algorithm interacts with other algorithms in the control system of SAPF, have been presented in Section 2. The need of a synchronization algorithm is dependent on the characteristics of the applied harmonic extraction algorithm. Generally, an explicit synchronization algorithm can be omitted when operation of the applied harmonic extraction algorithm involves voltage processing stage such as the algorithm developed based on *pq* theory. The features, suitability, and strengths and weaknesses of the synchronization techniques have been analyzed and discussed in Section 3. From the literature, some recently proposed techniques have been revealed to perform better than the traditional SRF-PLL technique. However, SRF-PLL technique is still well-accepted due to its uncomplicated control structure. Hence, further enhancements have been performed to improve capability of SRF-PLL which enables it to cope with distorted and unbalanced grid conditions. Lastly, it is recommended that hybrid, intelligent and optimized techniques for effective and stable synchronization especially in adverse and dynamic grid conditions should be given more attention in the future studies.

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