Article

A Surface-Potential-Based Analytical I - V Model of Full-Depletion Single-Gate SOI MOSFETs

Chuanzhong Xu ^{1,†}, Fei Yu ^{1,*,†} , Gongyi Huang ¹, Wanling Deng ², Xiaoyu Ma ²
and Junkai Huang ²

¹ Department of Electrical and Electronic Teaching, College of Information Science and Engineering, Huaqiao University, Xiamen 361021, China

² Department of Electronic Engineering, Jinan University, Guangzhou 510632, China

* Correspondence: yufei_jnu@126.com; Tel.: +86-0592-6162-385

† These two authors contributed equally to this work.

Received: 10 May 2019; Accepted: 12 June 2019; Published: 14 July 2019

Abstract: A surface-potential-based analytical I - V model of single-gate (SG) silicon-on-insulator (SOI) MOSFETs in full-depletion (FD) mode is proposed and compared with numerical data and Khandelwal's experimental results. An explicit calculation scheme of surface potential, processing high computation accuracy and efficiency, is demonstrated according to the derivation of the coupling relation between surface potential and back-channel potential. The maximum absolute error decreases into 10^{-7} V scale, and computation efficiency is improved substantially compared with numerical iteration. Depending on the surface potential, the drain current is derived in closed-form and validated by Khandelwal's experimental data. High computation accuracy and efficiency suggest that this analytical I - V model displays great promise for SOI device optimizations and circuit simulations.

Keywords: silicon-on-insulator MOSFETs; surface potential; back-channel potential; full-depletion; analytical I - V model

1. Introduction

Silicon integrated circuits (ICs) have become increasingly dense because the feature size of MOSFETs based on silicon-on-insulator (SOI) structure has not been a constraint in the sub-nanometer scale and both performance and cost improve as the feature size decreases. Up to now, there has still been considerable interest in optimizing properties of SOI MOSFETs [1–3] due to the widespread applications of SOI MOSFETs, such as sensors [4], memories [5], millimeter-wave circuits [6], and so on. Therefore, both device property optimization and IC design in the different fields imply that an analytical I - V model for accurately predicting I - V characteristics of SOI MOSFETs is imperative.

Recently, several analytical I - V models for bulk MOSFETs have been reported in the literatures [7–11] based on threshold voltage [7], inversion charge [8], and surface potential [9–11]. These models are demonstrated on the condition that the devices work in the partial-depletion (PD) mode, i.e., back-channel potential can be assumed to equate to zero or channel potential. However, these models cannot be applied into full-depletion (FD) single-gate (SG) SOI MOSFETs without any adjustment, due to the strong back-to-surface (B-S) potential coupling effect introduced by the ultrathin-body and buried oxide (BOX) in the FD SG SOI MOSFETs. Such a coupling effect increases the calculation complexity. In the meantime, some models [12–15] of multiple-gate SOI MOSFETs have been proposed, and some models of FD SG SOI MOSFETs [16–20] incorporating the B-S potential coupling effect are derived. Ravariu et al. [16] and Pandey et al. [17] developed threshold models for long- and short-channel FD SG SOI MOSFETs, respectively, by numerically solving a complicated equation about the position of the minimum back-channel potential. M. Miura-Mattausch et al. [18] also proposed

an analytical I - V model of FD SG SOI MOSFETs based on a completely potential-based description solving the Poisson's equation iteratively together with additional equations. Here, numerical computation reduced the calculation efficiency. W. Wu et al. [19] and Y. S. Yu et al. [20] gave surface-potential-based analytical I - V models in which smoothing functions are employed. In addition, J. Huang et al. [21] described a DC model of FD poly-Si TFTs based on the assumption of B-S potential relation. Because of computation complexity, they gave up deriving B-S potential relation, leading to low computation accuracy.

In this paper, we propose a surface-potential-based analytical I - V model of FD SG SOI MOSFETs. An explicit solution of surface potential in FD SG SOI MOSFETs is solved from the 1-D Poisson's equation and derivation of B-S potential coupling relation. This surface potential calculation scheme has high computation accuracy and efficiency, which is verified by numerical techniques. Subsequently, based on the surface potential, we present the drain current analytically and validate it with Khandelwal's experimental data [22]. Finally, combining with simulation results of this model, we discuss the effects of the different parameters on the electrical properties of FD SG SOI MOSFETs in detail.

2. Surface Potential Explicit Calculation Scheme

For FD SG SOI MOSFETs, a crystalline silicon (c-Si) film is deposited on a BOX film, as shown in Figure 1. The x -axis is perpendicular to the plane of gate, the carrier transport occurs along the y -axis, and the z -axis is set parallel to the structural confinement direction. In addition, t_{ox} and t_{si} are gate oxide and silicon body thicknesses, respectively. Following the gradual channel approximation and neglecting the whole concentration, we can simply write the Poisson's equation as:

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{si}} \left[n_0 \exp\left(\frac{\varphi - V_{ch}}{V_t}\right) + N_a \right]. \quad (1)$$

Here, φ is the electrostatic potential as a function of the variable x , the free charge density is demonstrated as $n_0 \exp[(\varphi - V_{ch})/V_t]$ where V_t is the thermal voltage (kT/q), k is the Boltzmann constant, T is the absolute temperature, q is the magnitude of electronic charge, ε_{si} is the dielectric permittivity of silicon, n_0 is expressed as $n_0 = N_a \exp(-2V_{fp}/V_t)$, V_{ch} is the channel potential, V_{fp} is the quasi-Fermi potential, and the doping concentration is symbolled by N_a . According to Figure 1, there are three boundary conditions for (1), i.e., φ_s is the surface potential with $\varphi_s = \varphi(t_{si})$, φ_b is the back-channel potential with $\varphi_b = \varphi(0)$, and $(d\varphi/dx)_{x=0} = 0$.

Figure 1. x - y cross section of silicon-on-insulator (SOI) MOSFETs.

It is noted that the c-Si film thickness of SOI MOSFETs comes into a sub-nanometer (<100 nm) scale so that the devices work in the FD mode rather than the PD mode of the bulk MOSFETs. From device structure aspect, the sub-nanometer film on BOX results in the strong back-to-surface (B-S) potential coupling effect, implied by the boundary condition $\varphi_b = \varphi(0)$ for (1). Here, φ_b cannot be set as a constant equating to V_{ch} , actually it is a function as φ_s according to $\varphi_s = \varphi(t_{si})$. This function is the B-S potential coupling relation, which is to be derived as follows.

For FD SG SOI MOSFETs, the channel layer is usually in the lightly or moderately doped case, i.e., free charge density is far larger than N_a , yielding:

$$\frac{d^2\varphi}{dx^2} = \frac{q}{\varepsilon_{si}} n_0 \exp\left(\frac{\varphi - V_{ch}}{V_t}\right). \quad (2)$$

We can observe that the mathematical form of (1) is relatively complicated because of the inclusion of an exponent term and a constant term in the right-hand side (RHS) of the equation, so that a solution of φ cannot be solved generally up to now. However, (2) retains the clear physical meaning and becomes the simplification of (1) to help us analytically derive the B-S potential coupling relation. We integrated (2) twice to obtain this relation as:

$$\varphi_s = \varphi_b + 2V_t \ln\left\{\sec\left[\frac{t_{si}}{2L_D} \exp\left(\frac{\varphi_b - V_{ch}}{2V_t}\right)\right]\right\}. \quad (3)$$

Here, L_D is the Debye length with $L_D = (\varepsilon_{si} V_t / 2q n_0)^{1/2}$.

Using the Gauss's law, the relation $\frac{d}{dx}\left(\frac{d\varphi}{dx}\right)^2 = 2\frac{d\varphi}{dx} \frac{d^2\varphi}{dx^2}$, and (1), we can obtain the implicit function of φ_s as:

$$C_{ox}^2 \left(\frac{V_{gs} - V_{fb} - \varphi_s}{V_t}\right)^2 = \frac{2q\varepsilon_{si}}{V_t} \left\{ N_a \left(\frac{\varphi_s - \varphi_b}{V_t}\right) + n_0 \left[\exp\left(\frac{\varphi_s - V_{ch}}{V_t}\right) - \exp\left(\frac{\varphi_b - V_{ch}}{V_t}\right) \right] \right\}. \quad (4)$$

If φ_b is set as a constant with $\varphi_b = V_{ch}$, then (4) degenerates to be only suitable for PD MOSFETs, i.e.,

$$C_{ox}^2 \left(\frac{V_{gs} - V_{fb} - \varphi_s}{V_t}\right)^2 = \frac{2q\varepsilon_{si}}{V_t} \left\{ N_a \left(\frac{\varphi_s - V_{ch}}{V_t}\right) + n_0 \left[\exp\left(\frac{\varphi_s - V_{ch}}{V_t}\right) - 1 \right] \right\}. \quad (5)$$

In the PD mode, we can solve (5) only to get φ_s . However, in the FD mode, we should analytically solve the equation set of (3) and (4) to get the expressions of φ_s and φ_b . Obviously, there is much more computation complexity in the FD mode compared with the PD mode. Substituting (3) into (4), we can solve an explicit solution of φ_b as:

$$\varphi_b = V_{ch} + V_t \ln\left(\frac{4L_D^2 \beta}{t_{si}^2}\right), \quad (6)$$

where β is symbolled as $\beta = \sqrt{\frac{2W_0(2re^{2F})}{W_0(2re^{2F})+4r}}$, F is symbolled as $F = \frac{V_{gs}-V_{fb}-V_{ch}}{2V_t} - \ln\left(\frac{2L_D}{t_{si}}\right)$, r is the nature parameter with $r = \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox} t_{si}}$, and W_0 is the Lambert W function [23], which is the solution of $W_0(x)\exp[W_0(x)] = x$. Furthermore, substituting (6) into (4), we can derive the explicit solution of φ_s as:

$$\varphi_s = V_{gs} - V_{fb} - 2V_t W_0\left[\frac{\lambda}{2} \cdot D \cdot \exp\left(\frac{V_{gs} - V_{fb} - V_{ch}}{2V_t}\right)\right] + \omega. \quad (7)$$

Here, λ is the bulk factor with $\lambda = \sqrt{2q\varepsilon_{si}n_0/V_t C_{ox}^2}$, D can be considered as the impact fact describing the B-S potential coupling effect in FD SG SOI MOSFETs with $D = \sqrt{\sin^2 \beta + N_a \cos^2 \beta \ln(\sec^2 \beta) / 4n_0 L_D^2 \beta^2}$, and ω is the Schroder series [24] used to improve the accuracy of the explicit solution of φ_s with $\omega = -(y/y') / (1 - 0.5yy'' / y' / y')$. Here, $y = C_{ox}^2 (V_{gs} - V_{fb} - \varphi_s)^2 - 2q\varepsilon_{si} [n_0 V_t \exp(\varphi_s / V_t - \varphi_b / V_t) + N_a (\varphi_s - \varphi_b)]$, and y' and y'' are the first and the second derivatives of y versus φ_s , respectively.

We compare φ_s of our scheme with that of the numerical method and show the results in Figures 2 and 3. We observe that good agreements are obtained and computational efficiency of (7) is seven times

that of the numerical method, as shown in Figure 2. Moreover, we analyze the absolute errors of φ_s in the different cases compared with the numerical results of (4) in Figure 3. First of all, the maximum errors of φ_s between (7) and the numerical results are less than 10^{-7} V. Then, the models of PD MOSFETs, i.e., (5), cannot be adopted into FD SOI MOSFETs and errors are up to 0.01V, because φ_b cannot be set as a constant in the FD mode. Lastly, in the process of computing φ_s , N_a should not be ignored even if in the lightly or moderately doped case, or else large errors would be introduced into the models.

Figure 2. Comparisons between the surface potential scheme and numerical results for different V_{ch} .

Figure 3. Absolute errors of φ_s between solution and numerical method vs. V_{gs} .

3. Analytical I-V Model

Considering the single-gate structure of the devices, the charge-sheet model (CSM) [25] derived by Brews can be adopted to derive the drain current including the drift and diffusion components, i.e., I_{ds1} and I_{ds2} , respectively. Based on the CSM and the solution of φ_s , we get the drain current I_{ds} as:

$$I_{ds} = I_{ds1} + I_{ds2} = -\mu \frac{W}{L} \int_{\varphi_{ss}}^{\varphi_{sd}} Q_i(\varphi_s) d\varphi_s + \mu \frac{W}{L} \int_{\varphi_{ss}}^{\varphi_{sd}} dQ_i(\varphi_s). \quad (8)$$

Here, φ_{ss} and φ_{sd} are solutions of φ_s corresponding to $V_{ch} = 0$ and $V_{ch} = V_{ds}$, respectively, and Q_i is the free charge density per unit area, which can be derived by using the Gauss's law at the interface between oxide and channel layers, yielding:

$$Q_i(\varphi_s) = -C_{ox}(V_{gs} - V_{fb} - \varphi_s) + qN_{at_{si}}. \quad (9)$$

In (8), μ is a typical set of universal effective charge mobility [26], including acoustical phonon [27] and surface roughness [28] scattering of the inversion layer carriers influenced from the normal field, i.e.,

$$\mu = \frac{\mu_0}{1 + \theta_1(V_{gs})^{1/3} + \theta_2(V_{gs})^2}, \quad (10)$$

where μ_0 is the maximum extracted value of the mobility at a given doping concentration, and θ_1 and θ_2 are degeneration parameters introduced by phonon scattering and surface-roughness scattering due to V_{gs} .

Substituting (9) and (10) into (8), we can analytically solve the expression of I_{ds} as:

$$I_{ds} = \frac{\mu_0}{1 + \theta_1(V_{gs})^{1/3} + \theta_2(V_{gs})^2 + \theta_3 V_{ds}} \cdot C_{ox} \frac{W}{L} \cdot \left[-\frac{1}{2}(V_{gs} - V_{fb} - \varphi_s)^2 - \left(\frac{qN_{at_{si}}}{C_{ox}} + V_t \right) \varphi_s \right]_{\varphi_{ss}}^{\varphi_{sd}}. \quad (11)$$

Furthermore, we match the results of (11) with Khandelwal's experimental data [22] required from ultrathin-body SOI MOSFETs in the cases of long- and short-channels. In [22], the ultrathin-body SOI MOSFETs were manufactured, with a silicon body thickness of 8 nm and gate oxide thickness of 1.2 nm, respectively. For long-channel devices, the length of channel is 11 μm . For short-channel devices, the length of channel is 30 nm. The parameters used in the simulations are listed in Table 1. As shown in Figures 7–10, we can observe that such a model can give a consistent solution for both transfer and output characteristics. It is noted that, for short-channel devices, channel-length modulation (CLM) is considered by using “effective drain-source voltage” [29] in our I - V model, i.e.,

$$V_{dseff} = \frac{V_{ds}}{\sqrt[a]{1 + (V_{ds}/V_{dsat})^a}}. \quad (12)$$

In (12), the parameter a is a transition factor deciding shift from the drain-to-source voltage V_{ds} to the effective drain-source voltage V_{dseff} , and V_{dsat} is an extracted saturation voltage parameter. In the process of the calculation, we can substitute V_{dseff} for V_{ch} in (6) and (7) to make the model include CLM, which is equivalent with pinch-off behavior or velocity saturation.

In Figures 7 and 8, we compare the model with Khandelwal's experimental data [22] for I_{ds} - V_{gs} and I_{ds} - V_{ds} characteristics in the long-channel device with 11 μm , which does not have a significant presence of channel-length modulation (CLM) in its characteristics. The excellent agreement between the model and the experimental data validates the core drain current model for long-channel devices. In Figures 9 and 10, our model is evaluated for short-channel effects by comparing I_{ds} - V_{gs} and I_{ds} - V_{ds} characteristics against Khandelwal's experimental data [22] for a short-channel device with $L = 30$ nm,

which also demonstrate good model accuracy. The presence of CLM is apparent from Khandelwal's experimental data [22] of output conductance (Figure 10) in this device. The reason why our proposed model can still capture these phenomena quite well is that we introduce “effective drain-source voltage” to describe CLM. According to the transfer characteristics shown in Figures 7 and 9, we can observe that short channel effects lead to subthreshold property degradation and a larger leakage current. According to output characteristics shown in Figures 8 and 10, we can observe that short channel effects result in obvious CLM or velocity saturation.

Table 1. Parameters for simulations in Figures 4–10.

Symbol (Units)	Value in Figures 7 and 8	Value in Figures 9 and 10	Value in Figure 4	Value in Figure 5	Value in Figure 6
N_a (cm ⁻³)	1×10^{12}	1.08×10^{11}	1×10^{13}	1×10^{13}	$1 \times 10^{12}, 1 \times 10^{14}, 1 \times 10^{16}$
t_{ox} (nm)	1.2	1.2	20, 40, 60	20	2
t_{si} (nm)	8	8	50	20, 60, 400	10
V_{fb} (V)	0	0	0	0	0
V_{ch} (V)	-	-	0	0	0
W (μm)	10	10	10	10	10
L (μm)	11	0.03	10	10	10
μ_0 (cm ² V ⁻¹)	250	250	250	250	250
θ_1 (-)	0.001	0.001	-	-	-
θ_2 (-)	0.001	0.001	-	-	-
V_{dsat} (V)	-	0.6	-	-	-
a (-)	-	2	-	-	-

Figure 4. Comparisons between the surface potential calculation scheme and numerical results for different t_{ox} , and the drain current in (11).

Figure 5. Comparisons between the surface potential calculation scheme and numerical results for different t_{si} , and the drain current in (11).

Figure 6. Comparisons between the surface potential calculation scheme and numerical results for different N_a , and the drain current in (11).

Figure 7. Comparisons of transfer characteristics between our drain current model results and long-channel experimental data [22] from Khandelwal et al.

Figure 8. Comparisons of output characteristics between our drain current model results and long-channel experimental data [22] from Khandelwal et al.

Figure 9. Comparisons of transfer characteristics between our drain current model results and short-channel experimental data [22] from Khandelwal et al.

Figure 10. Comparisons of output characteristics between our drain current model results and short-channel experimental data [22] from Khandelwal et al.

4. Discussion

In this section, we give some discussions about surface potential and drain current properties influenced by the structure parameters and the doping concentration of full-depletion single-gate SOI MOSFETs, including t_{ox} , t_{si} , and N_a . The parameters used in the simulations are listed in Table 1. We analyze the effect from the single variable by using our model as follows.

1. The thickness t_{ox} of dielectric between gate and channel rightly determines the ability of inducing charges, particularly for the strong inversion region, as shown in Figure 4. We can observe that φ_s increases as t_{ox} decreases. Thin t_{ox} leads to larger C_{ox} , and then, according to the Gauss's law, many more free charges are introduced in the strong inversion region. It means that larger φ_s and I_{ds} can be obtained in the channel.
2. The thickness t_{si} of the channel film can influence φ_b but not φ_s . According to Figure 5, t_{si} is larger and φ_b becomes larger. It is implied by the simplified Poisson's equation (1) only including the doping concentration. Simultaneously, I_{ds} is affected by t_{si} lightly, because the free charges in the inversion layers are confined to a very thin layer with the order of 10–100 Å [30]. That is also shown in Figure 5, graphed by our model.
3. Finally, we can observe from Figure 6 that φ_s , φ_b , and I_{ds} are in positive correlation with the doping concentration N_a , because N_a directly decides the value of the free charge density.

5. Conclusions

In this paper, we provided a surface-potential-based analytical I - V model for full-depletion single-gate silicon-on-insulator MOSFETs with lightly or moderately doped channels. Based on deriving analytically the back-to-surface potential coupling relation, we solved the explicit solution of the implicit surface potential function by using the Lambert W function, and matched this solution with the numerical iteration method. Considering single-gate structure and ultrathin channel film, the drain current was derived analytically on the basis of the charge sheet model, and good agreements with experimental data were obtained. Finally, we gave the discussions about influences of the structure parameters and the doping concentration on the electrostatic properties of the devices. As a result, accurate simulation results demonstrate that our model can predict electrostatic properties of full-depletion single-gate silicon-on-insulator MOSFETs.

Author Contributions: C.X. and F.Y. conceived and wrote the paper, designed and performed the simulations, and finally analyzed the data; G.H., W.D., X.M. and J.H. contributed to analysis tools.

Funding: This work was funded partially by the Scientific Research Funds of Huaqiao University under grant 16BS706, partially by the Scientific Research Funds for the Young Teachers of Fujian Province under grant JAT170034, and partially by the Fundamental Research Funds for the Central Universities under grant 21617405.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Karatsori, T.A.; Theodorou, C.G.; Josse, E.; Dimitriadis, C.A.; GHibaud, G. All Operation Region Characterization and Modeling of Drain and Gate Current Mismatch in 14-nm Fully Depleted SOI MOSFETs. *IEEE Trans. Electron Dev.* **2017**, *64*, 2080–2085. [\[CrossRef\]](#)
2. Pereira, A.S.N.; Steel, G.D.; Planes, N.; Haond, M.; Giacomini, R.; Flandre, D.; Kilchytska, V. An in-depth analysis of temperature effect on DIBL in UTBB FD SOI MOSFETs based on experimental data, numerical simulations and analytical models. *Solid State Electron.* **2017**, *128*, 67–71. [\[CrossRef\]](#)
3. Bong, J.H.; Kim, S.Y.; Jeong, C.B.; Chang, K.S.; Hwang, W.S.; Cho, B.J. Reliability improvement of a flexible FDSOI MOSFET via heat management. *Appl. Phys. Lett.* **2017**, *110*, 252101. [\[CrossRef\]](#)
4. Amor, S.; Andre, N.; Gerard, P.; Ali, S.Z.; Udrea, F.; Tounsi, F.; Mezghani, B.; Francis, L.A.; Flandre, D. Reliable characteristics and stabilization of on-membrane SOI MOSFET-based components heated up to 335 degrees C. *Semicond. Sci. Technol.* **2017**, *32*, 014001. [\[CrossRef\]](#)

5. Agrawal, N.; Kimura, Y.; Arghavani, R.; Datta, S. Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or III-V Semiconductor) on Variation for Logic and SRAM Applications. *IEEE Trans. Electron Dev.* **2013**, *60*, 3298–3304. [[CrossRef](#)]
6. Balteanu, A.; Sarkas, I.; Dacquay, E.; Tomkins, A.; Rebeiz, G.M.; Asbeck, P.M.; Voinigescu, S.P. A 2-Bit, 24 dBm, Millimeter-Wave SOI CMOS Power-DAC Cell for Watt-Level High-Efficiency, Fully Digital m-ary QAM Transmitters. *IEEE J. Solid State Circ.* **2013**, *48*, 1126–1137. [[CrossRef](#)]
7. BSIM6 Technical Manual. Available online: <http://www-device.eecs.berkeley.edu/bsim/>.
8. Enz, C.C.; Krummenacher, F.; Vittoz, E.A. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *Anal. Integr. Circ. Signal Process* **1995**, *8*, 83–114. [[CrossRef](#)]
9. Scholten, A.; Smit, G.D.J.; Vries, B.D.; Tiemeijer, L.; Croon, J.; Klaassen, D.B.M.; Langevelde, R.V.; Li, X.; Wu, W.; Gildenblat, G. The new CMC standard compact MOS model PSP: Advantages for RF applications. *IEEE J. Solid State Circ.* **2009**, *44*, 1415–1424. [[CrossRef](#)]
10. Miura-Mattausch, M.; Sadachika, N.; Navarro, D.; Suzuki, G.; Takeda, Y.; Miyake, M.; Warabino, T.; Mizukane, Y.; Inagaki, R.; Ezaki, T.; et al. HiSIM2: Advanced MOSFET model valid for RF circuit simulation. *IEEE Trans. Electron Dev.* **2006**, *9*, 1994–2007. [[CrossRef](#)]
11. He, J.; Chan, M.; Zhang, X.; Wang, Y. A Physics-Based Analytic Solution to the MOSFET Surface Potential from Accumulation to Strong-Inversion Region. *IEEE Trans. Electron Dev.* **2006**, *9*, 2008–2016. [[CrossRef](#)]
12. Ortiz-Conde, A.; García-Sánchez, F.J.; Muci, J.; Malobabic, S.; Liou, J.J. A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs. *IEEE Trans. Electron Dev.* **2007**, *54*, 131–140. [[CrossRef](#)]
13. Soon, J.; Yu, B.; Yu, Y.; Taur, Y. A Review on Compact Modeling of Multiple-Gate MOSFETs. *IEEE Trans. Circ. Syst. I Reg. Pap.* **2009**, *56*, 1858–1869.
14. Iniguez, B.; Jimenez, D.; Roig, J.; Hamid, H.A.; Marsal, L.F.; Pallares, J. Explicit continuous model for long-channel undoped surrounding gate MOSFETs. *IEEE Trans. Electron Dev.* **2005**, *52*, 1868–1873. [[CrossRef](#)]
15. Duarte, J.; Choi, S.; Moon, D.; Ahn, J.; Kim, J.; Kim, S.; Choi, Y. A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part II: Drain Current Model. *IEEE Trans. Electron Dev.* **2013**, *60*, 848–855. [[CrossRef](#)]
16. Ravariu, C.; Rusu, A.; Ravariu, F.; Dobrescu, D.; Dobrescu, L. The threshold voltage model of a SOI-MOSFET on films with Gaussian profile. In Proceedings of the 3rd IEEE International Caracas Conference on Devices, Circuits and Systems, Cancun, Mexico, 15–17 March 2000; pp. D64/1–D64/5.
17. Pandey, P.; Pal, B.B.; Jit, S. A new 2-D model for the potential distribution and threshold voltage of fully depleted short-channel Si-SOI MESFETs. *IEEE Trans. Electron Dev.* **2004**, *51*, 246–254. [[CrossRef](#)]
18. Miura-Mattausch, M.; Feldmann, U.; Fukunaga, Y.; Miyake, M.; Kikuchihara, H.; Ueno, F.; Mattausch, H.J.; Nakagawa, T.; Sugii, N. Compact Modeling of SOI MOSFETs With Ultrathin Silicon and BOX Layers. *IEEE Trans. Electron Dev.* **2014**, *61*, 255–265. [[CrossRef](#)]
19. Wu, W.; Yao, W.; Gildenblat, G. Surface-potential-based compact modeling of dynamically depleted SOI MOSFETs. *Solid State Electron.* **2010**, *54*, 595–604. [[CrossRef](#)]
20. Yu, Y.S.; Kim, S.H.; Hwang, S.W.; Ahn, D. All-analytic surface potential model for SOI MOSFETs. *IEE Proc. Circ. Dev. Syst.* **2005**, *152*, 183–188. [[CrossRef](#)]
21. Huang, J.; Deng, W.; Ma, X.; Ning, T. Surface Potential Calculation for Dynamic-Depletion Polysilicon TFTs with Both Gaussian and Exponential DOS Distribution. *IEEE Electron Dev. Lett.* **2013**, *34*, 774–776. [[CrossRef](#)]
22. Khandelwal, S.; Chauhan, Y.S.; Lu, D.D.; Venugopalan, S.; Karim, M.A.U.; Sachid, A.B.; Nguyen, B.Y.; Rozeau, O.; Faynot, O.; Niknejad, A.M.; et al. BSIM-IMG: A Compact Model for Ultrathin-Body SOI MOSFETs With Back-Gate Control. *IEEE Trans. Electron Dev.* **2012**, *59*, 2019–2026. [[CrossRef](#)]
23. Corless, R.M.; Gonnet, G.H.; Hare, D.E.G.; Jeffrey, D.J.; Knuth, D.E. On Lambert’s W function. *Adv. Comput. Math.* **1996**, *5*, 329–359. [[CrossRef](#)]
24. Yu, F.; Deng, W.; Huang, J.; Ma, X.; Chen, S. An Explicit Physics-Based I-V Model for Surrounding-Gate Polysilicon Transistors. *IEEE Trans. Electron Dev.* **2016**, *63*, 1059–1065. [[CrossRef](#)]
25. Brews, J.R. A charge sheet model of the MOSFET. *Solid State Electron.* **1978**, *21*, 345–355. [[CrossRef](#)]
26. Takagi, S.; Iwase, M.; Toriumi, A. On universality of inversion-layer mobility in n- and p-channel MOSFETs. In Proceedings of the Technical Digest, International Electron Devices Meeting, San Francisco, CA, USA, USA, 11–14 December 1988.

27. Huang, C.L.; Gildenblat, G.S. Measurements and modeling of the n-channel MOSFET inversion layer mobility and device characteristics in the temperature range 60–300K. *IEEE Trans. Electron Dev.* **1990**, *37*, 1289–1300. [[CrossRef](#)]
28. Yeric, G.M.; Tasch, A.F. A universal MOSFET mobility degradation model for circuit simulation. *IEEE Trans. Comput. Aided Des.* **1990**, *CAD-9*, 1123–1126.
29. Park, H.J.; Ko, P.K.; Hu, C. A charge sheet capacitance model of short channel MOSFETs for SPICE. *IEEE Trans. Comput. Aided Des. Integr. Circ. Syst.* **1991**, *10*, 376–389. [[CrossRef](#)]
30. Arora, N. *MOSFET Models for VLSI Circuit Simulation: Theory and Practice*, in Shrewsbury, 1st ed.; Springer: New York, NY, USA, 1993.

© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).