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Decoupling Capacitors Placement at Board Level Adopting a Nature-Inspired Algorithm

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Abstract: Decoupling capacitors are fundamental keys for the reduction of transient noise in power delivery networks; their arrangement and values are crucial for reaching this goal. This work deals with the optimization of the decoupling capacitors of a power delivery network by using a nature-inspired algorithm. In particular, the capacitance value and the location of three decoupling capacitors are optimized in order to obtain an input impedance below a specific mask, by using a nature-inspired algorithm, the genetic one, in combination with two electromagnetic solvers used to compute the objective function. An experimental board is designed and manufactured; measurements are performed to validate the numerical results.

Keywords: decoupling capacitors; power delivery network; genetic algorithm (GA); nature-inspired algorithm (NIA); power integrity; signal integrity

1. Introduction

The requests, coming from the market and incorporated by the industry, are more and more steered toward a miniaturization of the devices with the target to improve their performances. All these efforts are not costless: Shrinking the device dimensions implies a non-negligible number of problems such as degradation of the signal quality, increase in heat dissipation problems, and manufacturing complexity. All these aspects result in a collection of power and signal integrity issues [1,2].

Among the several causes that can lead to signal integrity (SI) problems, the power integrity (PI) related to the power/ground supply voltage at board level is one of the central requirements of modern design; having a power distribution network (PDN) defined by a high inductance or spending not enough time and effort on the PDN impedance design can cause severe PI issues [3]. Adopting decoupling capacitances (decaps) [4] is an effective solution in the optic of the reduction of transient noise caused by voltage droop due to the switching currents. A manual placement of decaps can lead to not optimal solution and can be time consuming; for these reasons, CAD tools and new algorithms [5–8] try to propose automatic procedures for the decaps arrangement. However, handling a large amount of decaps can lead to an increase of the power consumption, to reliability issues, and to a decrease of component space available on board [9]. As a result, a trade-off between the number of decaps, as well as their values, and their proper arrangement on board is a must for today's board design to fulfill all the requirements.

At the early stage of a printed circuit board (PCB) design and in particular its PDN, an optimization procedure might help and assist the designers providing a powerful tool from the selection of the electrical and geometrical parameters of the stack-up, to the appropriate placement of each decaps. This convenient and rational design aims to drastically reduce the signal and power integrity issues.

The nature-inspired algorithms (NIAs) [10,11] are a class of optimization algorithms inspired by natural mechanisms. They also include particle swarm optimization (PSO) [12], evolutionary algorithms (EA) [12], and genetic algorithms (GA) [13,14]. PSO is a population-based stochastic optimization technique; compared to EA and GA, the advantages of PSO are that it is easy to implement and there are few parameters to adjust. At the same time, not having evolution operators such as crossover and mutation, its efficiency in exploring the solution domain of the considered problem is limited. On the other hand, for the considered application, EA and GA have shown the highest efficiency from the computational point of view. Between them, GAs have a simpler architecture of the code. Computational efficiency and software architecture simplicity have stirred the choice of GAs as optimization algorithm for this work. The aim of this work is to explore, starting from simple configurations, the use of GAs as suitable algorithms for the optimization of the decoupling capacitance on a PDN at board level. In the following, a GA is adopted for finding the optimum number and values of decaps to be mounted on a simple PDN of a printed circuit board (PCB) with the goal to have an input impedance of the PDN below a specific mask selected by the designer based on the design specifications. The input impedance is evaluated through two different tools: EZpp [15-17] and PI/EMI analysis module within design force (from now on named "DF PI") (by Zuken [18]). The results will be the base for more realistic and complex analysis that will be carried out in the continuation of this research.

The paper is organized as follow: Section 2 describes the test board, in terms of geometry, stack-up, and materials. In the same section, there is a part concerning the main differences between the two solvers EZpp and DF PI. Section 3 is devoted to the GA describing the steps composing the algorithm. Section 4 shows the results of the optimization of decaps value; Section 5 reports the results of the optimization of both decaps value and their position. In Section 6, the proposed approach is validated by comparing the computed results with those measured on a specifically designed PDN board. Finally Section 7 discusses the significant outcomes and introduces the future steps of this research.

2. Overview of the Test Board

The test structure considered in this investigation, as shown in Figure 1, is a two-layer board built by two copper planes (electrical conductivity $\sigma_{cu} = 58$ MS/m, thickness $t_{cu} = 0.03$ mm) representing a PDN with power (PWR) and ground (GND) planes, separated by a FR4 dielectric slab (relative dielectric permittivity $\varepsilon_r = 4.3$, loss tangent $tg\delta = 0.02$, thickness $t_{FR4} = 0.25$ mm).



Figure 1. (a) Test boards and (b) its stack-up. The red circle represents the input port P from which the input impedance Z_{in} in evaluated by EZpp and design force (DF) power integrity (PI), whereas C_1 , C_2 , and C_3 are the three decoupling capacitors whose values have to be optimized by the genetic algorithm (GA).

Figure 1 also shows the port *P*, from which the input impedance Z_{in} of the PDN is evaluated during the optimization process. The target of the optimization is to find suitable values for the capacitances of $N_{pos} = 3$ decaps (C_1 , C_2 , C_3) placed at fixed positions near the input port *P* (blue squares in Figure 1a). In Section 5, the position of the decaps will become an optimization variable. Capacitors' parasitic inductance (ESL) and resistance (ESR) are kept fixed and equal to 50 nH and 30 m Ω , respectively. These stray parameters can be considered a sort of average values among those associated to the 0603 to the 0805 packages of the AVX Y5V series. The coordinates of the input port P and of the three decaps are summarized in Table 1.

Parameter	Description	x (mm)	y (mm)		
Р	Input Port	30	110		
C_1	Decoupling capacitance	10	160		
C_2	Decoupling capacitance	90	160		
$\overline{C_3}$	Decoupling capacitance	90	80		

Table 1. Coordinates of the input port *P* and the three decoupling capacitors (C_1 , C_2 , C_3).

Before proceeding with the optimization task, a comparison between the outputs from EZpp and those from DF PI has been done in order to detect the possible differences between the results. Consequently, the Z_{in} without decoupling capacitances has been computed by the two solvers and compared (Figure 2). Up to almost 50 MHz, the predominant factor is the capacitance of the planes, as justified by the capacitive trend of Z_{in} at low frequency. The equivalent capacitance can be quantified as:

$$C_{theory} = \varepsilon_r \varepsilon_0 \frac{A}{d} \tag{1}$$

where ε_0 is the vacuum permittivity, *A* is the area of the board and $t_{FR4} = 0.25$ mm is the distance between the two planes. EZpp and DF PI provide a capacitance value very close to Equation (1), as reported in Table 2.



Figure 2. Zin computed without decoupling capacitances by EZpp (red line) and from DF PI (blue line).

Table 2. Capacitance value extracted at 1 MHz from Z_{in} (Figure 2).

Solver	Capacitance (nF)			
EZpp	10.86			
DF PI	10.75			
Theory (Equation (1))	10.78			

The largest difference between the results from the two solvers can be appreciated at high frequency, where Z_{in} from DF PI exhibits an excess of inductance with respect to that from EZpp. This inductance can be quantified importing, in the circuit simulator Advanced Design System (ADS) [19], the S-parameters from the simulations without decaps and then adding a tunable series inductance between the termination port and the S-Parameter block of the circuit associated to the EZpp results, as depicted in Figure 3a. Tuning the inductance L1, the matching between the frequency spectra of the input impedance from the two solvers (Figure 3b) is reached using an inductance of L1 = 1.20 nH. According to the IEEE Standard P1597 [20], the feature selective validation technique [20–22] is used to quantify the matching of the two curves in Figure 3b. The matching is classified as "excellent" [20] being the FSV figure of merits GRADE = 1 and SPREAD = 1.



Figure 3. (a) Circuits used in ADS for tuning the inductance L1 in order to match Z_{in} , without decaps, from EZpp with the one from DF PI, getting the profiles shown in (b). The inset shows how a component, in this case a capacitor, is represented by DF PI with traces and vias creating the connection with PWR and GND planes.

The extra inductance L1 is introduced by the DF PI model due to the presence of traces and vias (see inset of Figure 3b), which create the connections of each component with the GND and PWR planes.

This conclusion is corroborated by a procedure in which the trace length l_{trace} (Figure 4a) is changed and the behavior of the input impedance is analyzed. In fact, if l_{trace} is changed from 0 (no traces, but vias) to 10 mm, Z_{in} undergoes variations at high frequencies, as highlighted in Figure 4b.





Figure 4. (a) Trace, whose length is l_{trace} , connecting the port to the vias and (b) Z_{in} computed by DF PI when the l_{trace} is changed from 0 to 10 mm.

3. Implementation of the Optimization Algorithms

The NIA chosen to optimize the capacitance values of the three capacitors is the genetic algorithm (GA) [13,14] inspired by the principles of natural selection. The aim of this section is to briefly describe how this algorithm works and how it is interfaced with the two tools, EZpp and DF PI.

3.1. The Genetic Algorithm

The genetic algorithm is a technique allowing a population, composed by N_p so-called chromosomes (*chrom*), to evolve according to specific laws toward a state able to minimize a cost function. The cost function f_{cost} is a mathematical function whose input is each chromosome of the population and the output is generally a value used for creating a rank among the N_p chromosomes; in this work, the f_{cost} is defined as follows:

$$f_{cost} = N_1 + \frac{N_2}{10^7}$$
(2)

where N_1 is the number of the frequency points (361 in the specific case) of Z_{in} that are larger than a specific mask, Z_{mask} (Figure 5), defined by the user, and N_2 is the area between the mask and Z_{in} . The factor 10^7 is introduced in order to avoid that N_2 becomes predominant with respect N_1 .



Figure 5. Z_{mask} delineating the upper limit for the input impedance Z_{in} of the board.

The target of a GA is to find a vector (*chromosome*) of $N_g = 3$ entries (genes) as,

$$chrom_i = \{C_1, C_2, C_3\}$$
 (2)

representing the capacitance of three decaps placed around P in a fixed position according to Figure 1a.

The objective of the GA is to minimize f_{cost} ; that is to say, to find the best member of the population, *chrom*_{best}, able to provide the smallest f_{cost} as possible.

The first step of the GA is the definition of the initial population, composed by N_p chromosomes, chosen by a random technique [13] from a minimum value, $C_{min} = 10$ nF, and a maximum value, $C_{max} = 1 \mu$ F, resulting in a $N_p \times N_g$ matrix. The next step is the *selection*: For each chromosome, the algorithm evaluates the cost function and ranks the population from the fittest (lowest f_{cost}) to the unfittest (highest f_{cost}) electing the best ones for the next step. The number of chromosomes discarded is selected through the variable X_r : The discarded chromosomes are deleted. In the present study, $X_r = 0.5$, meaning that half population survives, forming the mating pool, and it will be used for the generation of the offspring replacing the discarded chromosomes. Through a "Roulette Wheel" procedure [13], a pair of chromosomes is chosen for generating a pair of offspring; this procedure, called *mating*, takes place until all the $X_r \cdot N_p$ discarded chromosomes are replaced. The crossover point is randomly chosen between the first and the last genes of the parents' chromosomes; in this way, each parent donates part of its genes to the resulting offspring.

The subsequent step is the *mutation*, whose purpose is to introduce diversity in the population randomly altering one or more genes. The number of mutations is regulated by the mutation factor μ which, in the present study, is chosen as $\mu = 20\%$.

Once the mutation is applied, the cost function of the brand-new population is evaluated again. The entire procedure, described so far, is iterated until the maximum number of generations (max_{gen}) is reached or the convergence is reached ($f_{cost} = 0$). The outcome is the optimum values of the three capacitances C_1 , C_2 , C_3 .

3.2. Optimization Flow Using EZpp and DF PI

The genetic algorithm described in the previous subsection is implemented by using EZpp and DF PI as computational engines and is depicted in Figure 6a,b, respectively.



Figure 6. Optimization flow for (a) EZpp and (b) DF PI.

EZpp [17] is a tool, developed at the EMC Laboratory of the University of Missouri Science and Technology, based on a cavity model [15,16] able to find the S- and Z-Parameters of a PDN, once adding decoupling capacitors at any location over the board itself. All the geometrical and electrical parameters of the board, as well as the locations of input port and decaps, are stored in a text file (.ppf file).

On the other hand, DF PI by Zuken is a 3D PCB design suite which allows to draw the board, define material properties, and place components, selected from a vast library. The PI/EMI analysis tool engine implemented inside DF PI is able to provide the profile of the Z_{in} at the input port, as well as its spatial distribution, for specified frequencies.

The two flows in Figure 6a,b have similarities and differences. The main similarity is in their architecture: The logical position of the launching of the computational engine (EZpp or DF PI) for the evaluation of the cost function is the same to ensure a degree of uniformity in the software structure when the computational engine changes. The main difference between the two flows is how the software handles their input. Concerning EZpp, the N_p chromosomes forming the populations are written inside the N_p single.*ppf* files and used as input for EZpp. The resulting N_p input impedances, as .csv files, are compared with the mask for obtaining the cost function. Instead, DF PI introduces more flexibility: The entire population, composed by N_p chromosomes is written in a single *.xml* file which, through a batch procedure, is read by DF PI for the generation of as many input impedances.

4. Optimization of the Decoupling Capacitance Value

Figure 7a shows the result of the optimization using EZpp when the maximum number of generations is $max_{gen} = 10$ and is $max_{gen} = 100$. The resulting input impedances are very similar except at low frequency, around 2 MHz, where the Z_{in} from 10 generations exhibits a peak crossing the mask. As a consequence the case with $max_{gen} = 10$ is characterized by a higher f_{cost} , as confirmed by Table 3. The optimum value for the capacitor C_1 , $C_{1,opt}$, is very similar in both cases, confirming that the closest capacitor to the input port has the highest impact on the input impedance. In the direction of identify the optimal trade-off between computational time and accuracy of the solution, one can adjust the number of the maximum generations max_{gen} : The higher the value of max_{gen} , the lower the value of f_{cost} ; all this process is translated in an increasing of the computational time for the optimization algorithm. In the present case, $max_{gen} = 100$ introduces a slight improvement, in terms of Z_{in} , at low frequencies, where the capacitances have more effect.



Figure 7. (a) Result of the optimization in EZpp after 10 generations (solid red line) and 100 generations (dotted–dashed green line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$.

max _{gen}	<i>C</i> _{1,<i>opt</i>} (nF)	$C_{2,opt}$ (nF)	C _{3,opt} (nF)	N_1	$N_2/10^7$	f _{cost}
10	251.2	79.7	199.0	175	196	371
100	237.3	126.0	170.8	172	196	368

Table 3. Best solution provided by EZpp for the decaps value.

Adopting DF PI as solver for the optimization gives a Z_{in} as illustrated in Figure 8a. Also in this case, there is a slight difference between $max_{gen} = 10$ and $max_{gen} = 100$, at low frequency. The main difference with respect to EZpp is an aftermath of the excess inductance discussed in Section 2. This has a huge impact on the value of f_{cost} , especially for N_2 . A higher inductance implies a higher value of the impedance at high frequency, which means a larger value of the area between the mask and the Z_{in} resulting from the optimization, so explaining the higher value of f_{cost} , reported in Table 4, with respect the values from EZpp in Figure 7. Figure 8b testifies, once again, how an increase of the max_{gen} causes a decreasing of f_{cost} .



Figure 8. (a) Result of the optimization in DF PI after 10 generations (solid red line) and 100 generations (dotted–dashed green line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$.

max _{gen}	<i>C</i> _{1,<i>opt</i>} (nF)	<i>C</i> _{2,<i>opt</i>} (nF)	C _{3,opt} (nF)	N_1	$N_2/10^7$	f _{cost}
10	119.2	138.8	265.5	250	668	918
100	169.7	258.2	101.2	249	667	916

Table 4. Best solution provided by DF PI for the decaps value.

5. Optimization of Decaps Value and Position

The previous section is devoted to the optimization of the value of three decaps, when their position is fixed. The same algorithm used for this task can be adapted for the optimization of the three decaps value as well as their position on the board. Different from the previous scenario, now the decaps values cannot vary from a minimum value ($C_{min} = 10 \text{ nF}$) and a maximum value ($C_{max} = 1 \mu \text{F}$) in a continuous way, but in discrete steps. Defined $C_{elem} = 100 \text{ nF}$ (ESR = $30 \text{ m}\Omega$; ESL = 50 nH) as an elementary capacitance, in each of the $N_{pos} = 3$ positions the algorithm can place from $N_{dec,min} = 1$ to $N_{dec,max} = 5$ elementary capacitances in parallel. The positions on the boards are not arbitrary, but they are uniformly distributed on a grid, as depicted in Figure 9a. Additional relevant difference concerns the solver DF PI: As described in previous sections, because of the presence of 2 mm traces connecting the capacitance component to the vias, Z_{in} coming from DF PI exhibits higher inductance compared with the Z_{in} from EZpp, which does not take into account neither vias and traces. So, in the direction of carrying on a more consistent comparison between the two solvers, the 2 mm traces have been deleted and now the capacitor is directly connected with PWR and GND planes through vias (Figure 9b).

O Possible decap location O Input port							
			(a)			

Figure 9. (a) Possible positions for the decaps over the board and (b) new configuration for the capacitor in DF PI having no traces for the connection with the vias.

The *i*-th chromosome has the following form:

$$chrom_{i} = \{Pos_{1}, Pos_{2}, Pos_{3}, N_{dec,C1}, N_{dec,C2}, N_{dec,C3}\}$$
(3)

where Pos_1 , Pos_2 , Pos_3 represent three of the 52 possible grid positions and $N_{dec,C1}$, $N_{dec,C2}$, and $N_{dec,C3}$ are the number of elementary capacitors in each position.

Figures 10a and 11a show the output of the optimization, for $max_{gen} = 10$ and $max_{gen} = 100$, by using as computational engines EZpp and DF PI, respectively. Both solvers are able to fulfill the condition of an input impedance under the mask, especially at low frequency where the decaps are more effective. Increasing the number of maximum generations from 10 to 100 leads to a slight improvement in terms of cost function: 427 to 429 for DF PI and 326 to 330 for EZpp, as shown by Figures 10b and 11b. The insets in the same figures present the positions and the number of elementary decaps chosen by the GA. The placement resulting from EZpp sees the decaps closer to the input port with respect the position given by the optimization using DF PI. However, both solvers choose a number of decaps very close to the maximum $N_{dec,max} = 5$ and, more relevant, at least one position in the proximity of the input port P.



Figure 10. (a) Result of the optimization in EZpp up to 1 GHz after 10 generations (solid blue line) and 100 generations (dotted–dashed cyan line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$. The insets show the decaps placement after as max_{gen} changes its value and the number of elementary decaps in each position. The red circle represents the input port and the blue squares the position for the decaps.



Figure 11. (a) Result of the optimization in DF PI up to 1 GHz after 10 generations (solid blue line) and 100 generations (dotted–dashed cyan line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$. The insets show the decaps placement after as max_{gen} changes its value and the number of elementary decaps in each position. The red circle represents the input port and the blue squares the position for the decaps.

As mentioned, the benefit of decaps on the input impedance is more evident at low frequency so an optimization limited to $f_{max} = 10$ MHz has been carried out to better exploit the performances of EZpp and FD PI. Figures 12a and 13a show the profile of Z_{in} obtained by the two above-mentioned computational engines.



Figure 12. (a) Result of the optimization in DF PI up to 10 MHz after 10 generations (solid green line) and 100 generations (dotted–dashed light green line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$. The insets show the decaps placement after as max_{gen} changes its value and the number of elementary decaps in each position. The red circle represents the input port and the blue squares the position for the decaps.

When $f_{max} = 1$ GHz, due to the numerous resonances at high frequency, Z_{in} tends to more easily change its profile with the variation of number and position of the decaps and a stable cost function is reached after the 40th generation; when the optimization is limited up to $f_{max} = 10$ MHz, the convergence of the cost function is reached only after 20 generations as shown in Table 5. In addition, now the placement emerging from the optimization is characterized by decaps closer to the input port (Figures 12b and 13b). Finally, a remark on the computational efficiency. The two relevant parameters considered are the convergence (the number of generations needed to have a constant cost function) and the CPU time. In all cases considered, the maximum number of generations needed for convergence is a little less than 100 (Figure 8b) with an average of 49 over all test performed. This indicates that the implemented GA properly covers the search space. The maximum computational time for 100 generations is 109 min, including the plot and storage of the results.



Figure 13. (a) Result of the optimization in EZpp up to 10 MHz after 10 generations (solid green line) and 100 generations (dotted–dashed light green line) compared with the mask and the case without decaps. (b) Cost function f_{cost} as function of the number of generations when $max_{gen} = 10$ and $max_{gen} = 100$. The insets show the decaps placement after as max_{gen} changes its value and the number of elementary decaps in each position. The red circle represents the input port and the blue squares the position for the decaps.

Table 5. Best solution provided by DF PI and EZpp for the optimization of decaps value and position, changing the maximum optimization frequency (f_{max}) and the maximum number of generations (max_{gen}).

Solver	fmax	max _{gen}	N _{dec,C1}	N _{dec,C2}	N _{dec,C3}	N_1	$N_2/10^7$	fcost
	1 CU-	10	5	4	5	137	292	429
DF PI	I GHZ	100	5	5	5	135	292	427
DITT	10 MIL	10	5	4	5	57	11.5	68.5
	10 MHZ	100	5	5	5	56	11.3	67.3
	1 CU	10	5	5	5	142	188	330
EZpp	I GHZ	100	5	5	5	139	187	326
ΥΓ	10 101	10	5	5	5	57	2	59
	10 MHZ	100	5	5	5	56	2	58

6. Measurements

In order to support the results of this work (and also those related to the next steps of the project as indicated in the next section), a test vehicle of a PDN board has been designed and manufactured, whose geometry and electrical characteristics are similar to that described in Sections 2 and 5. Figure 14 shows the top view of the manufactured board in which either the footprint of the SMA connectors (ports) and the grid of pads for the decoupling capacitors are visible (as illustrated in Figure 9a).

As a first check, the input impedance at the left bottom port P of the PDN board without capacitors (bare board) has been measured paying attention to also de-embed the mainly inductive effects of the connector. The comparison between the frequency spectrum of the magnitude of the measured input impedance and the same impedance computed by DF PI (the computational engine of the proposed optimization procedure) is shown in Figure 15.



Figure 14. Manufactured power distribution network (PDN) board with the location of the measurement port P and the grid of possible positions of the decaps.



Figure 15. Comparison between the measured and computed values of the input impedance at the port P of the PDN board in Figure 14 without decaps.

After having run an optimization instance, the proposed algorithm generates the positions of six decoupling capacitors as indicated in Figure 16.



Figure 16. Positions of the decoupling capacitors on the PDN board after optimization (the position and numbers of the ports are circled in red. The input impedance is measured/computed at port numbered "1").

Figure 17 shows the comparison of the measured frequency spectrum of the magnitude of the input impedance of the PDN board with the decoupling capacitors mounted as in Figure 16 and the corresponding computed values.



Figure 17. Comparison between the measured and computed values of the input impedance at the port P of the PDN board with the decaps placed as in Figure 16.

From Figure 17, it appears that the proposed computational procedure is able to catch either the low-frequency (capacitive) behavior of the PDN board or its high-frequency (inductive) one. Between 100 MHz and 1 GHz, the resonant modes of the physical board are well matched with those computed. The number of measured frequency point is less than the number of computed one. This is the reason for the difference of depth between the two notches at around 5 GHz.

7. Conclusions

Decoupling capacitance is used for the reduction of transient noise in power supply network, but at the same time, a redundant number of them can lead to a considerable series of design issues. A systematic procedure for decaps quantification and placing has to be followed at different steps of the design. This work applies a nature-inspired algorithm to the definition of the decoupling capacitors on a PDN. The optimal position, the number of elementary decaps, and some figures of merit of the algorithm (such as the minimum significant number of generations) are evaluated using a GA, in cooperation with two software tools, EZpp and DF PI. Both software tools are suitable calculation engines; they are able to provide an optimal solution in a limited number of iterations with a very limited difference in their results, cross validating each other.

The computed numerical results in terms of the frequency spectrum of the input impedance are validated by means of the comparison with the measured values of the same impedance measured on a specifically designed PDN board.

The next steps of this research project target to apply the proposed procedure to the design of a real and more complex PDN considering some constraints in the cost function (such as minimum number of decaps, reliability issues, weight) and to introduce an artificial neural network (ANN), which will be able, once properly trained, to replace the use of complex software calculations engines as EZpp and DF PI, with a direct impact in the reduction of the simulation and optimization time.

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