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Editorial

Radiation Tolerant Electronics

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1. Introduction

Research on radiation tolerant electronics has increased rapidly over the last few years, resulting in many interesting approaches to model radiation effects and design radiation hardened integrated circuits and embedded systems. This research is strongly driven by the growing need for radiation hardened electronics for space applications, high-energy physics experiments such as those on the large hadron collider at CERN, and many terrestrial nuclear applications including nuclear energy and safety management. With the progressive scaling of integrated circuit technologies and the growing complexity of electronic systems, their ionizing radiation susceptibility has raised many exciting challenges, which are expected to drive research in the coming decade. Even though total ionizing dose effects in bulk CMOS are well known, little is still known on the radiation performance of advanced (FD-)SOI and FinFET technologies. Regarding single-event effects, the continued scaling has drastically increased the number of multiple-transistor or multiple-cell upsets, which requires not only new solutions to reduce the error rate in digital and mixed-signal ASICs, but also for FPGAs. The radiation hardness assurance of complex systems with multiple components in mixed technologies also necessitates new testing paradigms and verification methodologies to limit the time and cost for evaluation.

2. The Present Issue

This Special Issue features fifteen articles highlighting recent breakthroughs in modeling radiation effects for the design of radiation hardened integrated circuits, radiation hardening in embedded systems, and radiation hardening assurance. The contents of these papers are introduced here.

Two papers discuss the effect of radiation on advanced semiconductor devices such as dedicated power MOSFETs and double-polysilicon self-aligned bipolar transistors. In [1], the effects of cell structure adjustment on the performance of a power MOSFET were examined by first analyzing the design parameters. Next, a SEE- and TID-hardened power MOSFET was designed and fabricated. Results of the investigation confirmed the achievement of excellent radiation hardness and decent specific on-resistance for the device. Article [2] discussed the mechanism of degradation on the Irradiated Double-Polysilicon Self-Aligned Bipolar Transistor with a dose rate of 50 rad (Si)/s and 0.05 rad (Si)/s. The comparison of the high and low dose rate showed that the increase of the base current caused by low dose rate irradiation was larger than that caused by high dose rate irradiation, resulting in greater current gain degradation than that caused by the high dose rate, highlighting that the ELDRS effect may occur.

Several papers discuss the total-dose and/or single-event radiation effects on custom designed analog, mixed signal, and RF integrated circuits. A radiation-hardened instrumentation amplifier for sensor readout integrated circuits was presented in [3] to target nuclear fusion applications. The circuit boasts TID effect monitoring and adaptive reference control functions. The radiation tolerance was verified through SPICE simulations with radiation-aware transistor models. In [4], the authors presented the proton induced SEE characterization of a highly integrated RF transceiver in 65 nm CMOS. The exposed proton energies were split into two test campaigns to induce high energy protons

(up to 184 MeV) and low energy protons down to 4 MeV. The results showed a very low sensitivity to proton irradiation, independent of the proton energy. The total ionizing dose radiation assessment of a 15.6 ps single-shot Time-to-Digital Converter was presented in [5]. Two samples were irradiated and were able to reach a dose of 2.2 MGy before failing to meet specification due to an increased non-linearity error, originating from the increased mismatch in the charge-pump of the sampling circuit. A comprehensive evaluation of two subthreshold voltage reference circuits with respect to their resilience to SEE, TID, and TID/DD was performed in [6]. The evaluation was supported by measured results with γ-rays, x-rays, protons, and heavy ions. The high total doses applied in this range of experiments provide a complete evaluation of subthreshold circuits in the whole range of space applications, radiation physics instruments, and medical applications. The authors in [7] discussed a time-variant on Single-Event Transients (SETs) in integrated CMOS ring oscillators. The Impulse Sensitive Function (ISF) of the oscillator was used to analyze the impact of the relative moment when a particle hit the circuit. The analysis was based on simulations and verified experimentally with a Two-Photon Absorption (TPA) laser setup. Article [8] presented a comprehensive study of the effects of SETs and SEUs on a frequency synthesizer for the IEEE 802.15.4 standard. The blocks that work at low frequencies were not affected by ion impacts. However, high frequency circuits such as the VCO were more vulnerable. The VCO's radiation tolerance was improved by using RC-filtering and a capacitive divider was introduced to improve the degraded phase noise.

Two articles focus on the radiation hardening of digital circuits. A new approach to implement fine-grain circuit hardening was developed and validated in [9]. This offers a dedicated VHDL package as a new tool for mitigating soft errors on digital circuits, with minimal code modifications as the designer only has to select which signals or ports should be hardened and then change their datatype accordingly. Article [10] presented a novel method for the physical implementation of Triple Modular Redundant high-speed digital circuits. The method uses a distributed constraining approach for TMR branches to avoid long interconnects between voters. The method was tested with increasingly complex digital modules and showed results that improved as the design size increased.

Three papers of this Special Issue target embedded radiation hardening in FPGA or microcontroller systems. In [11] single-event radiation hardening techniques for SRAM-based FPGAs in 65 nm CMOS technology were discussed. Both layout hardening techniques and configuration hardening techniques including ECC and TMR were employed for this FPGA. The heavy-ion results indicated a satisfactory radiation tolerance, especially for the DICE CRAMs. A novel four module radiation hardening approach for FPGA was presented in [12]. This was implemented on a zynq-7000 development board (Zybo) and it was shown that the proposed method could be used for a radiation tolerant synchronous buck converter design for applications requiring a relatively longer mission time, compared to the TMR and FMR techniques. In [13], a compact model was presented to evaluate the effects of high-level C++ code radiation hardening. The use of appropriate C++ classes facilitated the use of TMR. Additionally, the availability of an easy-to-use performance estimation model could be used for quick and effective radiation tolerance optimization of microcontroller systems.

Finally, two articles presented a link between the research fields of cryptography and image processing, respectively. In [14] the authors presented the total ionizing dose effects on a delay-based physical unclonable function implemented in FPGAs for authentication and key generation in space systems. Article [15] discussed a novel method to protect series and parallel line-buffer-based image processing pipelines against configuration memory errors in SRAM-Based FPGAs. The proposed technique presented lower FPGA resource usage, and fewer false positive detections than the other techniques; moreover, the image processing system did not have to be stopped and rebooted upon errors due to the partial reconfiguration.

3. Future

The wide range of articles in this Special Issue exemplifies the broadness of the field of radiation hardened micro-electronics. The dream to enable high performance computing, signal processing,

and communication in the harshest and most diverse radiation environments presents the community with many research challenges. It inevitably brings researchers together from several disciplines ranging from nuclear and solid-state physics over advanced modeling approaches and creative circuit design techniques to the application of progressive algorithms and deep learning to optimize system performance for the most diverse applications under the harshest of conditions.

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