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A Doping-Less Tunnel Field-Effect Transistor with $Si_{0.6}Ge_{0.4}$ Heterojunction for the Improvement of the On–Off Current Ratio and Analog/RF Performance

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Received: 5 May 2019; Accepted: 21 May 2019; Published: 24 May 2019

Abstract: In this paper, a novel doping-less tunneling field-effect transistor with $Si_{0.6}Ge_{0.4}$ heterojunction (H-DLTFET) is proposed using TCAD simulation. Unlike conventional doping-less tunneling field-effect transistors (DLTFETs), in H-DLTFETs, germanium and $Si_{0.6}Ge_{0.4}$ are used as source and channel materials, respectively, to provide higher carrier mobility and smaller tunneling barrier width. The energy band and charge carrier tunneling efficiency of the tunneling junction become steeper and higher as a result of the $Si_{0.6}Ge_{0.4}$ heterojunction. In addition, the effects of the source work function, gate oxide dielectric thickness, and germanium content on the performance of the H-DLTFET are analyzed systematically, and the below optimal device parameters are obtained. The simulation results show that the performance parameters of the H-DLTFET, such as the on-state current, on/off current ratio, output current, subthreshold swing, total gate capacitance, cutoff frequency, and gain bandwidth (*GBW*) product when $V_d = 1\ V$ and $V_g = 2\ V$, are better than those of conventional silicon-based DLTFETs. Therefore, the H-DLTFET has better potential for use in ultra-low power devices.

Keywords: DLTFET; on/off current ratio; heterojunction; frequency characteristics

1. Introduction

Conventional metal oxide semiconductor field-effect transistors (MOSFETs) with carrier diffusion drift are susceptible to the short-channel effect when device sizes decrease, which can increase the power consumption and off-state leakage current [1–3]. In addition, the subthreshold swing (SS) value of MOSFETs has a minimum limit of 60 mV/Dec at room temperature due to the statistical distribution of thermodynamics, so the switching ratio decreases [4,5]. In order to improve the performance of smaller devices, researchers have studied many new materials and new device structures. Two-dimensional materials have excellent physical, chemical, and optical properties. Meanwhile, materials such as graphene [6], MoS_2 [7], and $PdSe_2$ [8] have adjustable electronic properties and bandgap width. It is these excellent characteristics that give two-dimensional materials great application potential for use in electronic devices. The new device structures that have been researched include multi-gate devices that improve electrostatic characteristics [9], ultrathin silicon-on-insulator (UTSOI) MOSFETs [10], gate-all-around (GAA) MOSFETs [11], and Fin field-effect transistors (Fin-FETs) [12]. Device performance can also be improved by using narrow bandgap semiconductor materials, high-k gate dielectric materials such as III–V-based and $Si_{1-x}Ge_x$-based devices [13,14], and tunneling field-effect transistors (TFETs) [15,16]. TFETs have a lower SS value

and off-state current, so they can obtain a larger voltage gain and noise margin in inverter circuit applications [17]. However, the switching ratio and frequency characteristics are far from ideal in TFETs, and the fabrication processes are complicated, which can limit their application in digital circuits.

To improve the analog/radio frequency (RF) performance and simplify the fabrication processes of TFETs, a doping-less tunnel field-effect transistor (DLTFET) is proposed [18,19]. A DLTFET can form heavily doped source and drain regions using the appropriate metal electrode work functions. Due to the absence of an abrupt junction, the fabrication processes of DLTFETs are simpler, and random doping fluctuations have no effect on device performance [20–22]. Therefore, it is possible to produce DLTFET devices more innovatively with the development of fabrication processes, such as the etching process, epitaxial growth process, and atomic layer deposition (ALD) process. A larger on-state current can also be obtained when device sizes decrease. However, the disadvantages of DLTFETs are their larger off-state current, power consumption, and lower switching ratio, so their use is not competitive [23].

In this paper, a DLTFET with $Si_{0.6}Ge_{0.4}$ heterojunction (H-DLTFET) is proposed using TCAD simulation in order to improve the on/off current ratio and the analog/RF performance. Compared with conventional DLTFETs, H-DLTFETs differ in that their source regions and channel regions use the narrow bandgap semiconductor material germanium and the high carrier mobility material $Si_{0.6}Ge_{0.4}$. The Ge–Si tunneling junction can decrease the effective tunneling length, thereby increasing the on-state current [24]. At the same time, it is possible to reduce the leakage current by the valence band energy difference between germanium and silicon, which is caused by the valence band holes in the off-state. The structure of this paper is organized as follows: First, the device structures and simulation methods of a DLTFET and a H-DLTFET are introduced, and then, the input and output characteristics of the DLTFET and H-DLTFET are discussed. Next, the operating mechanism of the H-DLTFET is studied, and the effect of device size on the performance of the H-DLTFET is analyzed. The C-V and frequency characteristics are then researched. Finally, the conclusions of this paper are presented.

2. Device Structure and Simulation Method

Figure 1a,b shows the structural diagrams of a conventional DLTFET and the proposed H-DLTFET. In Figure 1, the device sizes are both the same, but the source and channel materials are different. The heavily doped source and drain regions are generated by the charge plasma, and the abrupt PN junction is formed between the source and the channel, both of which are consistent with conventional TFETs [25]. The gate and the source with different work functions are located on both sides of the channel, the energy band of the overlapping region between the gate and the source is bending, and the line tunneling is formed from the bottom to the top of the channel so that the electron tunnel efficiency can be improved.

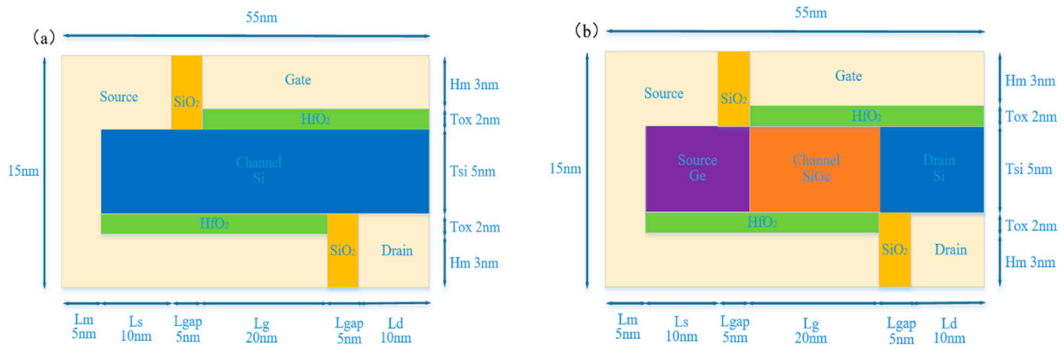

Figure 1. Schematic diagrams of (**a**) a conventional tunneling field-effect transistor (DLTFET) and (**b**) the new proposed doping-less tunneling field-effect transistor with $Si_{0.6}Ge_{0.4}$ heterojunction (H-DLTFET).

Unlike the conventional DLTFET, the semiconductor materials Ge and $Si_{0.6}Ge_{0.4}$ in H-DLTFETs were used as the source and channel materials in order to provide higher carrier mobility. The energy band of the tunneling junction became steeper, and the tunneling efficiency became higher because of

the $Si_{0.6}Ge_{0.4}$ heterojunction between the source and the channel, which greatly improved the on/off current ratio and frequency characteristics. The specific simulation parameters of the DLTFET and H-DLTFET were as follows: the length of the source region L_s, channel L_g, and drain region L_d were 15 nm, 20 nm, and 15 nm, respectively; the doping concentration $N_c = 5 \times 10^{18}$ cm^{-3}; the gate dielectric layer thickness of HfO_2 Tox_1 = 2 nm; the gap-layer thickness of SiO_2 Tox_2 = 5 nm; the channel layer thickness H_c = 5 nm; the source work function φ_{Source} = 5 eV; the gate work function φ_{Gate} = 3.8 eV; and the drain work function φ_{Drain} = 4.2 eV.

In this paper, the simulation was based on SILVACO ATLAS. The non-local band-to-band tunneling (BTBT) model was used to analyze the non-local generation of electrons and holes and was used to accurately simulate the electronic tunneling process. Considering the effect of the channel doping region, the bandgap narrowing model was included. The H-DLTFET simulation models also included the Schokely–Read–Hall recombination, Fermi statistics, and the electric field model [26]. The C-V and frequency characteristics were obtained using an operating frequency of 1 MHz.

3. Results and Discussion

The H-DLTFET had the same device structure, size parameters, and physical models as the conventional DLTFET, except that the source region used the narrow bandgap semiconductor material germanium with larger channel carrier mobility and a smaller bandgap. It also had good compatibility with the silicon process, which decreased the leakage current. The channel region used the high carrier mobility material $Si_{0.6}Ge_{0.4}$, and the forbidden bandwidth and band structure changed with the changes in the germanium content, which resulted in higher carrier mobility and smaller tunneling barrier width. The energy band and effective tunneling length of the tunneling junction both became steeper and shorter because of the Ge–Si heterojunction, which improved the carrier tunneling efficiency, switching speed, and on-state current.

This section consists of two parts. In the first part, the input/output characteristics of the DLTFET and H-DLTFET are compared, and then, the operating mechanism of the H-DLTFET is analyzed. The effects of the source work function, gate oxide dielectric thickness, and Ge content on the performance of the H-DLTFET are then discussed. Finally, the second part compares the C-V characteristics and the analog/RF performance and then analyzes the cutoff frequency and gain bandwidth (*GBW*) product of the DLTFET and H-DLTFET.

3.1. Input and Output Characteristics

Figure 2a shows the transfer characteristics of the DLTFET and H-DLTFET when the drain voltage was 1 V. The maximum on-state current of the DLTFET was 83 μA/μm, whereas the maximum on-state current of the H-DLTFET could reach 169 μA/μm. Meanwhile, compared with the conventional DLTFET, the on/off current ratio of the H-DLTFETs increased by three orders of magnitude due to the lower off-state current. The average SS value could be extracted when the drain current rose from 10^{-6} to 1 μA/μm. The average SS values of the DLTFET and H-DLTFET were 26.7 mV/Dec and 15.2 mV/Dec, respectively. At the same time, the minimum SS values of the DLTFET and H-DLTFET were 6.7 mV/Dec and 3.9 mV/Dec, respectively. The H-DLTFET had a larger line tunneling current due to the $Si_{0.6}Ge_{0.4}$ heterojunction, which could improve the on-state current and SS value. Therefore, the H-DLTFET has great potential in the emerging market of ultra-low bio-equipment.

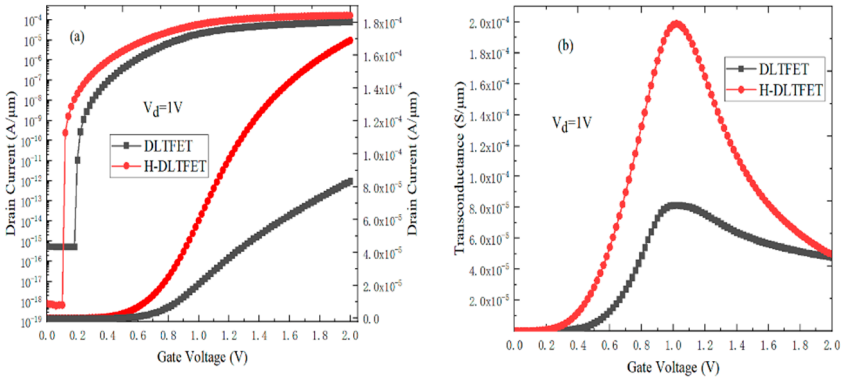

Figure 2. (**a**) Transfer characteristics; (**b**) transconductance of the DLTFET and the H-DLTFET.

As an important parameter, the transconductance (g_m) was used to evaluate the simulation performance of the device, which was defined as the first derivative of the transfer characteristic [27], and the value of g_m is provided by Equation (1):

$$g_m = dI_{ds}/dV_{gs}. \quad (1)$$

As shown in Figure 2b, the maximum g_m value of the DLTFET was 81.5 μS/μm and the maximum g_m value of the H-DLTFET was 198.8 μS/μm, so the g_m value of the H-DLTFET was almost doubled in comparison with the conventional DLTFET.

Figure 3a,b shows the output characteristics of the DLTFET and the H-DLTFET according to the different gate voltages. At first, the drain current increased linearly with the drain voltage, and the output saturation drain currents of the DLTFET and the H-DLTFET were 83.5 μA/μm and 166.9 μA/μm when V_g = 2 V and V_d = 1 V, respectively. Therefore, the output current of the H-DLTFET was much higher than that of the DLTFET.

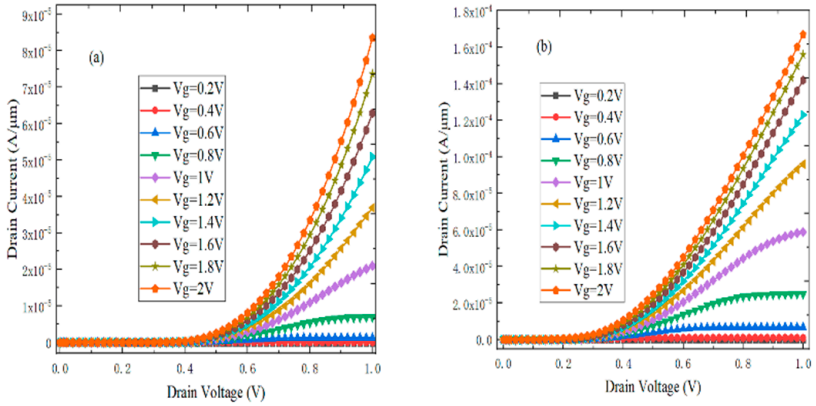

Figure 3. Output characteristics: (**a**) the DLTFET and (**b**) the H-DLTFET at different gate voltages.

3.2. The Operating Mechanism of H-DLTFETs

The operating mechanism of the H-DLTFET is explained in Figures 4 and 5. Figure 4a,b shows the electron and hole BTBT generation rates in the on-state. Line tunneling occurred in the alignment region between the gate and the source, and the carrier tunneling rate was evenly distributed along the tunnel junction. In Figure 4c, the electric field and the BTBT rate of the tunneling junction increased due to the $Si_{0.6}Ge_{0.4}$ heterojunction, so the on-state current increased. In addition, the total current density of the H-DLTFET, according to the on-state, was researched in order to understand the operating mechanism, as shown in Figure 4d. The electrons from the source region and the channel bottom region could be easily absorbed by the drain region to form the tunneling leakage current [28,29].

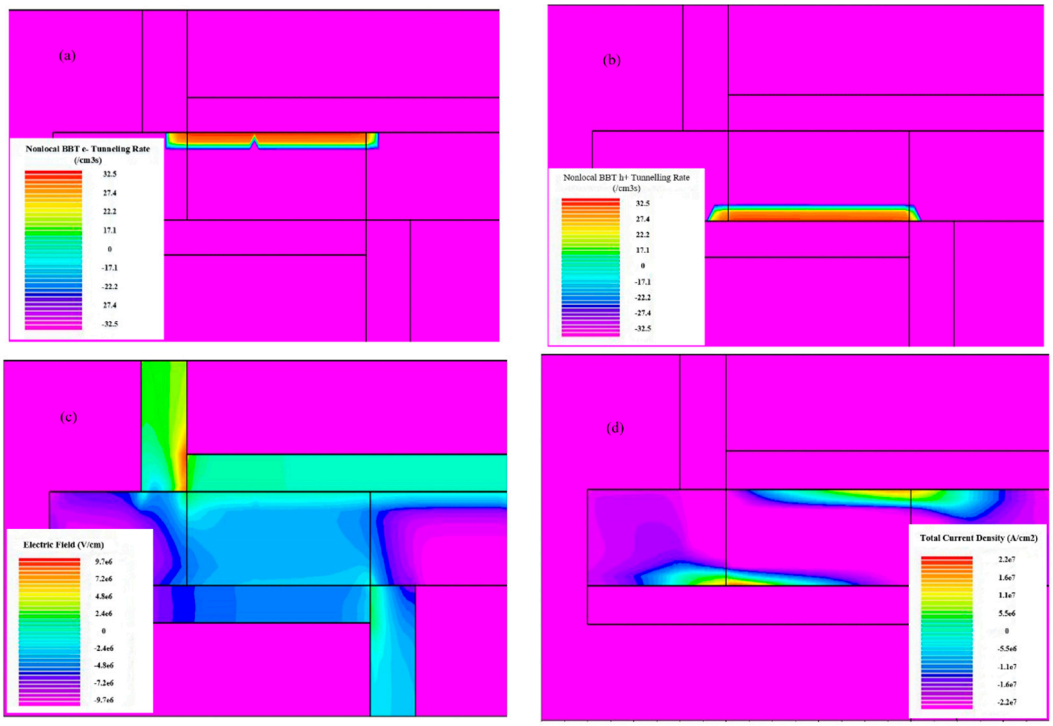

Figure 4. (**a**) Electronic band-to-band tunneling (BTBT) generation rate; (**b**) hole BTBT generation rate; (**c**) electric field distribution; and (**d**) total current density distribution of the H-DLTFET.

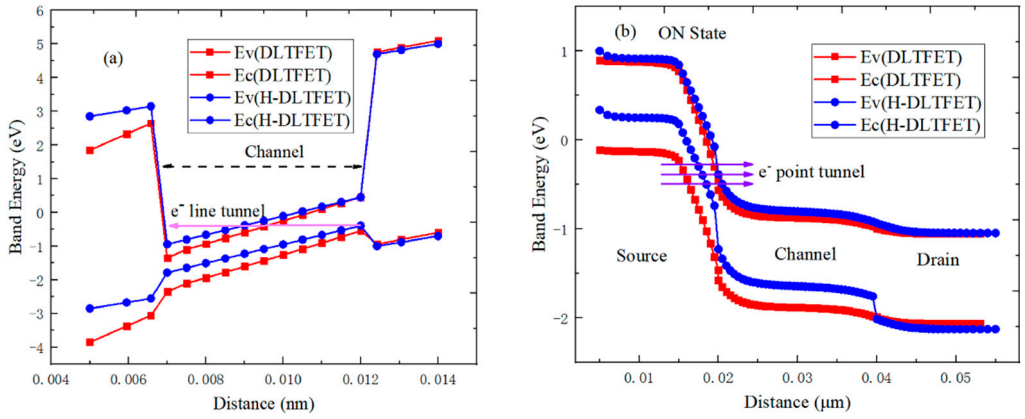

Figure 5. Schematic diagram of the energy band according to the on-state condition (**a**) in the middle of the channel from the top channel to the bottom channel and (**b**) on the channel surface from the source to the drain.

Figure 5 shows the on-state energy band of the DLTFET and the H-DLTFET when they were in different locations. As shown in Figure 5a, the valence band at the bottom of the channel was aligned with the conduction band at the top of the channel, and many electrons tunneled from the bottom of the channel to the top of the channel to form the line tunneling current. The channel of the H-DLTFET used $Si_{0.6}Ge_{0.4}$ material to provide higher carrier mobility. The source with the higher work function could accumulate many holes at the bottom of the channel, and the electrons could be accumulated by the top channel when a lower work function and a higher voltage were applied to the gate. Therefore, the line tunneling current could be generated in the channel region due to the pseudo-mutation PN junction [30]. It can be seen in Figure 5b that the tunneling barrier width of the H-DLTFET between the source and the channel was lower than that of the DLTFET, which could allow more electrons to tunnel from the source to the channel. The narrower the tunneling barrier, the higher the point tunneling current.

3.3. *Effect of Device Sizes on the Performance of H-DLTFETs*

Figure 6 shows the effect of gate oxide dielectric thickness (T_{ox}) on the transfer characteristics and energy band of the H-DLTFET. As shown in Figure 6a, the on-state current and switching ratio of the H-DLTFET increased, and the transfer characteristic curve shifted to the left significantly when the T_{ox} decreased from 5 to 2 nm. The reason for this is that the higher surface potential difference between the gate and the source resulted in a lower tunneling barrier width. The energy band and the electric field of the source/channel tunneling junction then became steeper and higher as the T_{ox} decreased, and the point tunneling current increased, as shown in Figure 6b. Therefore, the H-DLTFET with its thinner gate dielectric was easier to turn on, and the transfer characteristic curve shift to the left was greater.

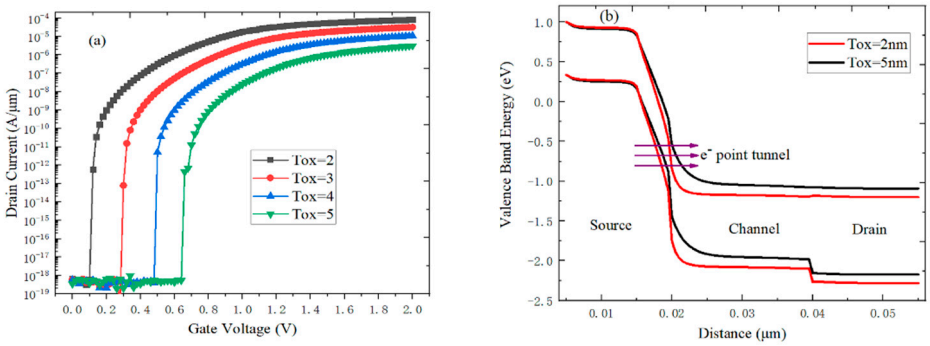

Figure 6. (**a**) Influence of T_{ox} on the transfer characteristic; (**b**) on-state energy band at the surface of channel from the source to the drain.

Figure 7 shows the effect of Ge content on the performance of the H-DLTFET. In Figure 7a, the on-state current of the H-DLTFET increased from 52.7 to 222.3 μA/μm, and the transfer characteristic curve drifted to the left when the Ge content increased from 0.1 to 0.5. The Ge content had an influence on the forbidden bandwidth of $Si_{1-x}Ge_x$ material and on the tunneling barrier width between the source and the channel. It can also be explained by the on-state energy band from the top of the channel to the bottom of the channel according to the different Ge content, as shown in Figure 7b. The energy band became steeper and the electric field and line tunneling area become higher as the Ge content increased, which increased the on-state current. Therefore, the optimum Ge content was 0.4.

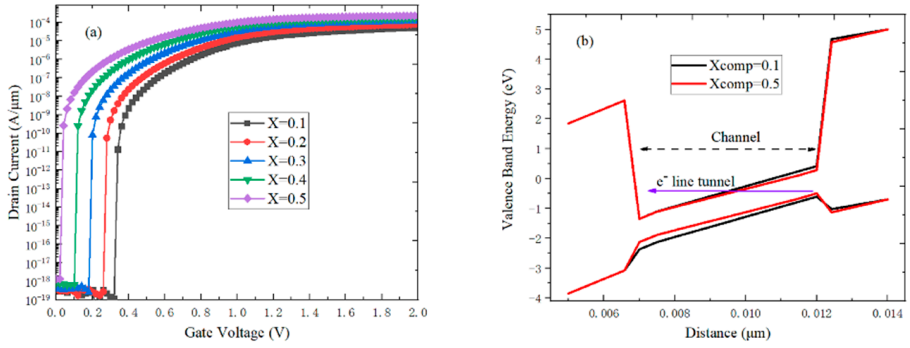

Figure 7. Influence of X_{Ge} on (**a**) the transfer characteristic and (**b**) the on-state energy band from the top channel to the bottom channel.

Finally, the influence of the source work function (Ψ_s) on the performance of H-DLTFETs was also studied. As shown in Figure 8a, the on-state current increased from 19.9 to 110.7 μA/μm when Ψ_s increased from 4.7 to 5.1 eV, so the optimal Ψ_s was 5 eV. At the same time, the off-state current decreased by more than three orders of magnitude. The pseudo-mutation PN junction became steeper, the electric field became higher, and more holes accumulated at the bottom of the channel when the Ψ_s became larger, so the line tunneling current was higher. As shown in Figure 8b, the on-state energy

band and electron thermal excitation barrier at the bottom of the channel became steeper and larger as the Ψ_s increased, and the off-state leakage current could be suppressed effectively.

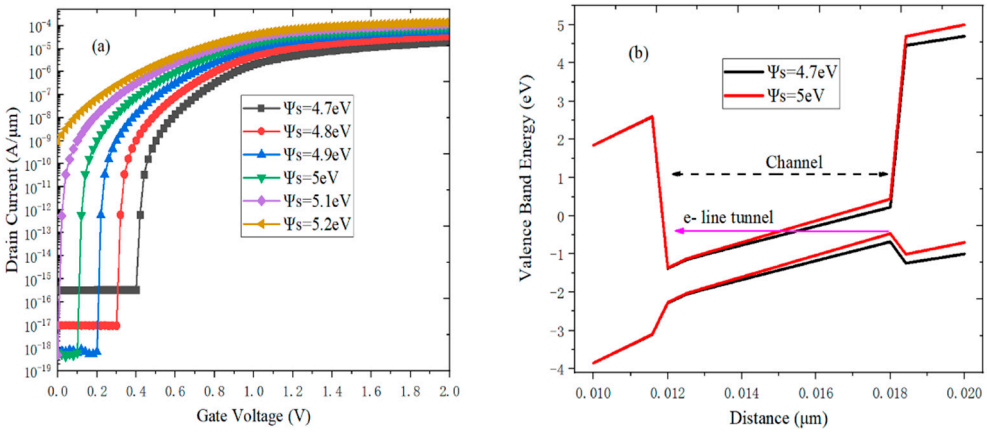

Figure 8. Influence of Ψs on (**a**) the transfer characteristic and (**b**) the on-state energy band from the top channel to the bottom channel.

3.4. Capacitance Characteristics

The gate capacitance (C_{gg}) is one of the basic parameters used to evaluate the frequency characteristic and analog/RF performance of DLTFETs and H-DLTFETs. C_{gg} is mainly composed of gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) [31]. TFETs have a small C_{gs} due to the presence of the source/channel tunneling junction. Figure 9a,b shows the capacitance characteristics of the DLTFET and the H-DLTFET. C_{gg} and C_{gd} both increased as the V_{gs} increased, and C_{gs} maintained a very small value when the drain voltage was 1 V. Therefore, C_{gd} was the major component of C_{gg}. It can be seen in Figure 9a,b that C_{gg} and C_{gd} of the H-DLTFET were slightly lower than that of the DLTFET. The electrons of the source/channel tunneling junction were collected by the drain region. Due to the Ge–Si heterojunction, the electric field at the tunneling junction of the H-DLTFET was higher than that of the DLTFET. Meanwhile, the electron tunneling rate changed as the gate voltage changed, which could also lead to a rapid change in the accumulated electrons.

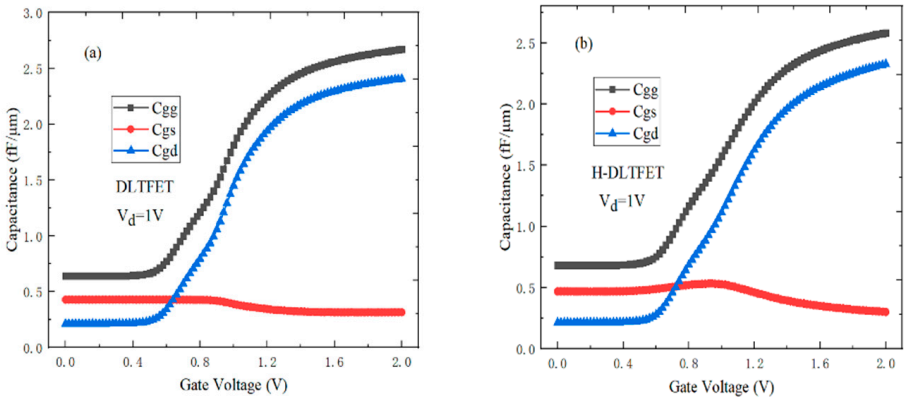

Figure 9. C-V characteristics of (**a**) the DLTFET and (**b**) the H-DLTFET.

3.5. Frequency Characteristic

The cutoff frequency (f_T) and *GBW* product are important indicators for evaluating the frequency characteristics of DLTFETs and H-DLTFETs [32]. In Equation (2), the f_T can be expressed by a ratio of g_m to C_{gg} [33,34].

$$f_T = \frac{g_m}{2\pi c_{gs}\sqrt{1+2c_{gd}/c_{gs}}} \approx \frac{g_m}{2\pi\left(c_{gs}+c_{gd}\right)} = \frac{g_m}{2\pi c_{gg}} \quad (2)$$

The *GBW* can be expressed as a ratio of g_m to C_{gd} for the DC gain value equal to 10 [35], as shown in Equation (3).

$$GBW = g_m/2\pi 10c_{gd} \quad (3)$$

Figure 10a,b shows the f_T and *GBW* of the DLTFET and H-DLTFET when the drain voltage was 1 V. The DLTFET could achieve a maximum f_T of 7.95 GHz and a maximum *GBW* of 1.12 GHz when V_g = 0.9 V and V_{gs} = 0.88 V, respectively. However, the maximum f_T of 20.75 GHz and the maximum *GBW* of 2.71 GHz of the H-DLTFET could be achieved when V_{gs} = 0.94 V and V_{gs} = 0.86 V. Therefore, the H-DLTFET showed better analog/RF performance, so it can be used for the health Internet of Things (IOTs) applications.

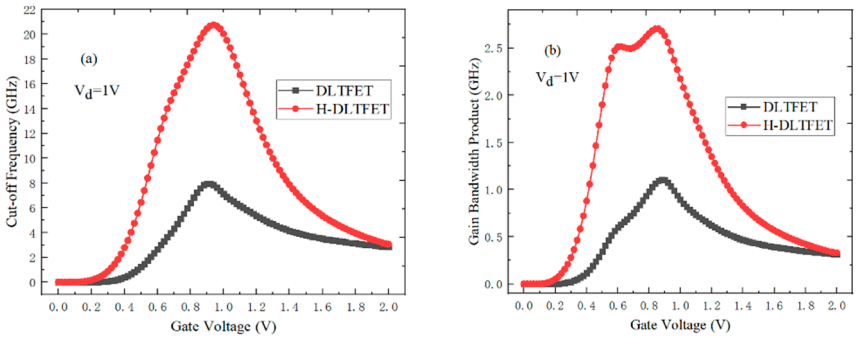

Figure 10. (**a**) Cutoff frequency and (**b**) the gain bandwidth product of the DLTFET and the H-DLTFET.

4. Conclusions

In this paper, a H-DLTFET is proposed and studied using TCAD simulation. Unlike conventional DLTFETs, the source and channel regions of the H-DLTFET used Ge and $Si_{0.6}Ge_{0.4}$ materials to obtain a higher carrier mobility and a lower tunneling barrier width. The energy band and the carrier tunneling efficiency of the tunneling junction became steeper and higher because of the $Si_{0.6}Ge_{0.4}$ heterojunction between the source and the channel, which could greatly improve the on/off current ratio and frequency characteristics. In addition, the effects of the source work function, gate oxide dielectric thickness, and Ge content on the performance of the H-DLTFET were analyzed in detail, and then, the above optimal device parameters were obtained. The simulation results showed that the on-state current and the output saturation drain current of the H-DLTFET increased from 83 and 83.5 to 169 and 166.9 μA/μm, respectively. The maximum g_m also increased from 81.5 to 198.8 μS/μm, and the switching ratio increased by three orders of magnitude compared with the DLTFET when V_d = 1 V and V_g = 2 V. The average SS and minimum SS of the DLTFET were 26.7 mV/Dec and 6.7 mV/Dec, respectively, whereas the average SS and minimum SS of the H-DLTFET were 15.2 mV/Dec and 3.9 mV/Dec, respectively. Meanwhile, the f_T and *GBW* of the H-DLTFET increased from 7.95 and 1.12 to 20.75 and 2.71 GHz, respectively. Therefore, the H-DLTFET had a higher switching ratio and better analog/RF performance, and it has great potential for use in the Internet of Things and neural network computers.

Author Contributions: Conceptualization and writing—original draft preparation, T.H.; methodology, S.W.; validation, S.C.; writing—review and editing, H.L. and W.L.; funding acquisition, H.L.

Funding: This research was funded by the National Natural Science Foundation of China (Grant No. U1866212), the Foundation for Fundamental Research of China (Grant No. JSZL2016110B003), the Major Fundamental Research Program of Shaanxi (Grant No. 2017ZDJC-26), the Innovation Foundation of Radiation Application (Grant No.KFZC2018040206), and the Fundamental Research Funds for the Central Universities (Grant No.

20101196741). It was also supported by the Shanghai Aerospace Science and Technology Innovation Fund, the Fundamental Research Funds for the Central Universities, and the Innovation Fund of Xidian University.

Conflicts of Interest: The authors declare no conflicts of interest.

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