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Integrated Building Cells for a Simple Modular Design of Electronic Circuits with Reduced External Complexity: Performance, Active Element Assembly, and an Application Example

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Abstract: This paper introduces new integrated analog cells fabricated in a C035 I3T25 0.35-μm ON Semiconductor process suitable for a modular design of advanced active elements with multiple terminals and controllable features. We developed and realized five analog cells on a single integrated circuit (IC), namely a voltage differencing differential buffer, a voltage multiplier with current output in full complementary metal–oxide–semiconductor (CMOS) form, a voltage multiplier with current output with a bipolar core, a current-controlled current conveyor of the second generation with four current outputs, and a single-input and single-output adjustable current amplifier. These cells (sub-blocks of the manufactured IC device), designed to operate in a bandwidth of up to tens of MHz, can be used as a construction set for building a variety of advanced active elements, offering up to four independently adjustable internal parameters. The performances of all individual cells were verified by extensive laboratory measurements, and the obtained results were compared to simulations in the Cadence IC6 tool. The definition and assembly of a newly specified advanced active element, namely a current-controlled voltage differencing current conveyor transconductance amplifier (CC-VDCCTA), is shown as an example of modular interconnection of the selected cells. This device was implemented in a newly synthesized topology of an electronically linearly tunable quadrature oscillator. Features of this active element were verified by simulations and experimental measurements.

Keywords: advanced active elements; CMOS; electronic control; circuit synthesis and design; oscillator; modular approach

1. Introduction

Active elements (AEs) are the most important subparts of analog and mixed signal processing systems [1]. They are frequently used in various simple electronic circuits, such as linear filters [2,3] and signal generators [4], and also in complex nonlinear applications [5,6]. Bipolar and unipolar transistors, as active devices [7–9], can be directly applied in the circuit synthesis and design. This approach seems to be beneficial in gaining operation at high-frequency bands [10]. However, in these cases, the dynamics and linearity of the circuits are usually very restricted (tens of mV; see, for example, Reference [9]).

Moreover, these circuits require proper biasing and bias point setting [11], which in general are not easy tasks. The interconnection of transistor-only circuits with other systems requires AC coupling. Some systems [12] use such a high number of transistors that the complexity is similar to standard AEs (e.g., operational amplifiers (OAs)). Furthermore, when electronic controllability is required, then this must be solved separately for each design.

Standard AEs [1–3,13], which have been known for decades, usually utilize a quite high number of transistors. However, they have certain advantages: For instance, no external biasing and bias point settings, stabilized parameters with a minimized influence of temperature changes and fabrication mismatches, many types of easy applications, possible DC coupling of the input/output signals, and a relatively large and linear dynamic range. Standard commercial AEs are fabricated in bipolar junction transistor (BJT) technologies or complementary metal–oxide–semiconductor (CMOS) technologies as standalone devices to use in particular applications, usually in combination with other devices. Another possibility is to integrate the whole system using these AEs and additional components on a chip (system-on-a-chip) [14]. An OA [1,2,13,15] is a basic and widespread AE that belongs to the group of AEs without controllable parameters. It serves as the design for well-known linear and nonlinear building blocks of analog systems. On the other hand, the simplest noncontrollable AE (i.e., a current follower or inverter (CF/I) [13]) also offers a very simple interterminal transfer relation and is very useful for many applications [16]. AEs, known as noncontrollable current conveyors (CCs) [2,13,17–19], combine voltage-mode (VM) and current-mode (CM) signal processing operations. CCs can also be implemented through the specific interconnection of other discrete devices in various VM and CM applications [20]. It is important to note that the previously mentioned AEs do not have the feature of electronic controllability of their parameters.

The simplest electronically adjustable AEs have a single controllable internal parameter. The operational transconductance amplifier (OTA) [21] represents a typical example of the conversion of input voltage difference to an output current through controllable transconductance (g_m) [22]. The electronic control of the voltage gain (A) [23] is also very important in many applications. Variable gain amplifiers (VGAs), referred to as AEs with a controllable A, can be obtained by the particular interconnection between OTAs and CCs [3,13,24] or are accessible as standalone commercial devices [25]. Variants of CCs with controllable internal parameters are also available. They usually allow for adjusting one of the following parameters: The resistance of the current input terminal (R_X) [26], current gain (B) between terminals [27–29], and voltage gain (A) [30] between terminals.

Multiparameter controllability, in the frame of AEs, has been introduced recently. First, CCs and current amplifiers (CAs) with these features target the controllability of parameters R_x and B [31–34]. These multiparametric features are beneficial especially for signal generation and filtering in order to extend the available range of tunability [34,35].

In this work, advanced AEs bring together different simple active subparts, referred to as cells. The combination of an OTA and CC [36,37] represents a typical example of a voltage differencing current conveyor (VDCC). Such a construction of advanced AEs is known as a modular approach (or design). The commercially available integrated circuit (IC) OPA860 [20] can be understood as a modular device because it consists of a CC and voltage buffer (VB) in the same IC package, and both parts can be used independently or are interconnected outside the package. A current feedback operational amplifier (CFOA), in the form of an AD844 chip [38], can be understood similarly (a CC of the second generation and a VB). However, in this case, both subparts are also connected internally. The same idea was also used for the design and construction of integrated universal current and voltage conveyors (UCCs and UVCs) [39,40]. Note that the above-discussed examples (the OPA860, AD844, UCCs, and UVCs) of a "modular design" are not examples of electronically controllable AEs. Typical examples of advanced and also electronically controllable modular AEs, fabricated in an IC form, have been discussed in References [36,37,41,42]. An example of an advanced AE bringing three controllable parameters (g_m, R_x, B) into one device can be found in Reference [43], where a modification of the VDCC (behavioral model) was presented. Many other

concepts were introduced in References [3,4], and especially in Reference [13]. These AEs are described and compared to our design in detail in Section 2.

1.1. Contribution of the Paper

This paper introduces a newly fabricated IC (an ON Semiconductor 0.35-μm I3T25 CMOS process [44]) that allows for a modular design of various advanced AEs with several controllable parameters. Our concept was based on five newly designed different cells included on the chip, namely (a) a voltage differencing differential buffer (VDDB), (b) a voltage multiplier (MLT) with current output in full CMOS form (CMOS MLT), (c) a voltage multiplier with current output with a bipolar core (BJT MLT), (d) a current-controlled current conveyor of the second generation (CCCII) with four current outputs, and (e) a single-input and single-output adjustable current amplifier (CA). The topological novelty of the presented cells is described by the following points:

(1) A new topology of VDDB device with an additional section of differential pairs (to obtain additional voltage input) is proposed. Compared to standard OA topology [45,46], this is a significant change with better dynamics than topology used in Reference [47] and references cited therein;
(2) A new topology of CMOS MLT with a current output terminal is proposed. It contains additional linearizing blocks (not used in the most similar topology [48]) and a "current-boosting" OTA stage in order to increase dynamic range and decrease the linearity error. Note that the multiplier in Reference [48] operated with an input voltage range ±100 mV, but our CMOS MLT design provides ±500 mV. Therefore, the dynamics are significantly improved;
(3) A standard Gilbert core-based [49] BJT MLT was designed in order to obtain a more accurate device than the CMOS MLT (in general, the accuracy of the CMOS design is a problem). It has a larger transconductance constant and better symmetry of output swing currents than the CMOS MLT does. Moreover, our BJT MLT concept, compared to Reference [48], has a current output terminal instead of a voltage output terminal. Thanks to the presence of two multipliers (CMOS and BJT) in our IC package, an extension of the controllability of new advanced AEs is possible;
(4) Compared to Reference [50], a modified CCCII cell topology with full mirroring of currents from differential stage (pair) to four output terminals is presented. The main innovation is in specific biasing current reference generation for output mirrors and driving the value of R_X (which was not the intention of Reference [50]). In contrast to our solution, the concept in Reference [50] is not capable of providing a large dynamic range and output cascoding due to its bias sources (voltage drop in real MOS elements) when very low supply voltage used;
(5) A current amplifier cell with a completely new topology, designed for low-power purposes, is presented. Good linearity in a dynamic range of ±200 μA, linear control of current gain, low input (around 1 Ω) and excellent output resistance, and low power consumption are the main advantages of the proposed concept.

It is important to mention that the design and fabrication of these cells and topologies have not been provided in I3T25 0.35-μm (±1.65-V supply) technology before. The functionality of our design, especially in the case of multipliers and low-voltage technologies, was confirmed. Supply voltage restrictions made the design process more sophisticated, requiring special additional counterparts in the case of MLTs (namely linearization and boosting stages) due to a limited output current swing. Therefore, our cell design is original (newly designed transistor sizes and bias conditions) and optimized (significant modifications and extensions of basic topologies) for selected technology and anticipated applications.

1.2. Organization of the Paper

The rest of this paper is structured as follows. Section 2 contains a comparison of our manufactured IC device with commercially available devices and similar modular approaches.

Section 3 introduces the fabricated device and the features of its partial cells. Selected results that describe the performances of the realized cells of our IC are presented in Section 4. An example of the interconnection of cells assembled in the new advanced controllable AE and its application example (a novel topology of a quadrature oscillator), including a complete analysis (simulation and experimental measurements) and comparisons to state-of-the-art solutions, are presented in Section 5. Finally, Section 6 concludes this paper with an overview of the achieved results.

2. Related Solutions of Modular Concepts

In this section, we compare commercial devices as well as already known modular concepts of IC devices to our proposal.

The general purpose of the implemented cells follows recent requirements for the development of advanced electronically controllable multiterminal active devices. Standard design requirements for novel applications suppose the availability of multiple current output terminals (a CCCII cell) for current-mode operations, voltage differencing/summing operations (a VDDB cell) for voltage-mode processing, multiplication, electronic controllability of the transformation between voltage and current (MLT cells), and gain variability (in our case the current gain of CA). These principles can be used either separately or together depending on the complexity and considered features of the advanced AE. Particularly, features connected with multiplication may lead to nonstandard advanced AEs that are currently unknown and not defined in the state-of-the-art. Such a phenomenon should also be interesting in the synthesis and design of new applications in circuit theory, automatization and control theory, communications, and measurement. Many known advanced AEs, for instance in References [3] and [13], or new types and modifications of AEs can be constructed as the interconnections of several cells in our new IC (see the selected application example in this paper).

Table 1 gives an overview and comparison of typical commercially available examples of modular devices [20,38], as well as relevant customized and fabricated ICs offering interconnections of internal cells ([36,37,39–42]). From this overview we can recognize the following drawbacks:

(a) Low variability (low number of cells [20,36–40]);
(b) Internal cells only, with basic functionality (two cells in the package, and one of them is a voltage buffer [20,38]);
(c) No electronic controllability of the parameters [20,38–40];
(d) Limited electronic controllability (single parameter only [41,42]);
(e) Differential/summing voltage operations are not available (except [39,40]);
(f) Multiplicative operations are not available (except [36,37]).

In contrast to previously fabricated modular cells (or commercial devices AD844 [38] and OPA860 [20]), our new proposal offers many useful features simultaneously:

(a) Five various cells (independent active cells implementing four different types of operations) are available;
(b) A significantly improved variability in interconnection (compared to References [20,36–41], the number of possible combinations is higher);
(c) Four independent electronically controllable parameters of three types (2 g_m, R_X, and B); and
(d) Differential and summing voltage operations as well as multiplicative operations are available.

Our developed IC (including its cells) significantly extends the current state-of-the-art through additional features and controllable parameters (see comparison of typical and similar concepts in Table 1) that were not simultaneously available in the mentioned previous works.

Despite the existence of the "modular approach" presented in this paper, there are also different methods for the assembly/synthesis and classification of AEs [51–53]. The work in Reference [51] focused on a systematic algorithm that employed a nullor-based description of active devices and their counterparts. It gives a comprehensive list of AEs synthesized from voltage and current followers, MOS building blocks (e.g., current mirrors), MOS elements, and complex parts (several types of current conveyors). The difference between our work and Reference [51] is in the depth of abstraction. The compilation of modern active elements used in Reference [51] goes to the origin of

structures (elementary subparts of CMOS topology). Our work, in accordance with the modular approach, supposes the existence of basic building cells (OTAs, amplifiers, etc.). Their interconnection is not always systematic, but heuristic and based on experience determining the best way to interconnect according to the requirements of common applications. A similar classification was also presented in Reference [52], where nullor-based models were used as generalized descriptions of the circuit behavior that can be obtained by different methods of synthesis, interconnection, and understanding of equivalence (reciprocity principles, transformation between voltage- and current-mode and vice versa, etc.). The discussed circuit models of various active subparts (each of them can be constructed through different ways (the interconnection of MOS building parts)) are known in circuit theory as pathological elements. Generally, previous approaches have simply followed the basic idea of synthesis (a single theoretical description of their operations can be obtained in several ways).

The proposed modular design can also be compared to fully integrated (including passive elements) solutions of so-called field-programmable analog arrays (FPAAs) [53]. Very good variability and easy availability of various interconnections of internal components (full integrators, amplifiers, nonlinear operations, etc.) are strong advantages of the FPAA-based designs. However, in comparison to our concept, some of their features are not beneficial:

(a) Continuous electronic control is not available (FPAAs are tunable digitally in discrete steps);
(b) Not favorable frequency features (the expected speed of applications and operation of signal paths up to tens of kHz);
(c) High power consumption (in hundreds of mW);
(d) Not a fully analog solution (additional mixed-mode subsystems and control circuits, including a clock signal, are required in an IC), and therefore the overall complexity is much higher; and
(e) A high cost of available development kits.

Table 1. Comparison of typical examples of commercially available devices to relevant customized modular IC devices.

References	Number of Cells (Internal Subparts)	Types of Cells (Number and Purpose of Terminals)	Independent Cells (No Internal Interconnection)	Variability in Interconnection	Electronically Controllable Parameters	Number of Electronically Controllable Parameters	Types of Electronically Controllable Parameters	Differential/Summing Voltage Operations Available	Multiplicative Operations	Technology (Fabrication Process)
[20]	2	1 current conveyor (1 voltage input, 1 current input, 1 current output); 1 voltage buffer (1 input, 1 output)	Yes	Yes	No	0	-	No	No	BJT commercial
[36,37]	2	1 current-controlled current conveyor (1 voltage input, 1 current input, 2 current outputs); 1 CMOS multiplier (4 voltage inputs, 1 current output)	Yes	Yes	Yes	2	1 g_m, 1 R_X	No	Yes	CMOS 0.7-µm
[38]	2	1 current conveyor (1 voltage input, 1 current input, 1 current output); 1 voltage buffer (1 input, 1 output)	No	No	No	0	-	No	No	BJT commercial
[39,40]	2	1 universal multiterminal current conveyor (3 voltage inputs, 1 current input, 4 current outputs); 1 current conveyor (1 voltage input, 1 current input, 1 current output)	Yes	Yes	No	0	-	Yes	No	CMOS 0.35-µm
[41]	2	1 current conveyor (1 voltage input, 1 current input, 1 current output); 1 OTA stage (2 voltage inputs, 1 current output)	Yes	Yes	Yes	1	g_m	No	No	CMOS 0.7-µm
[42]	5	2 current differentiators (2 current inputs, 1 current output); 2 current conveyors (1 voltage input, 1 current input, 1 current output); 1 OTA stage (2 voltage inputs, 1 current output)	Yes	Yes	Yes	4	g_m	No	No	CMOS 0.7-µm
This work	5	1 VDDB (3 voltage inputs, 1 voltage output); 1 current-controlled current conveyor (1 voltage input, 1 current input, 4 current outputs); 1 CMOS multiplier (4 voltage inputs, 1 current output); 1 BJT multiplier (4 voltage inputs, 1 current output); 1 current amplifier (1 current input, 1 current output)	Yes	Yes	Yes	4	2 g_m, 1 R_X, 1 B	Yes	Yes	CMOS/BJT 0.35-µm

Notes: g_m, transconductance; R_X, resistance of current input terminal; B, current gain. Note that the simplest solutions [20,38] (commercially available devices) were added only for comparison purposes, and they are not typical representatives of complex modular ICs. CMOS: complementary metal–oxide–semiconductor; OTA: operational transconductance amplifier; VDDB: voltage differencing differential buffer.

3. A Developed Integrated Device for the Modular Design of Active Elements

Although there are many up-to-date technologies available, technology with a 0.35-μm minimum size for transistors is very useful in an analog circuit design. In the case of digital or mixed digital and analog circuit design, newer technologies represent a better choice. However, in the pure analog design (our case), such small transistors cause significant problems, for instance due to their non-idealities (e.g., channel length modulation effects). Therefore, we selected ON Semiconductor C035 0.35-μm I3T25 technology [44]. It is available in the frame of the Europractice university consortium, and it is a very good compromise between cost and performance for its intended purposes. The proposed modular concept consists of five completely independent cells (a VDDB, CMOS MLT, BJT MLT, CCCII, and CA) within a single package. For fast and comfortable manipulation, the fabricated device was embedded into a DIL28 ceramic package. The designed cells are described in the following subsections, supplemented by both simulation (Cadence IC6 Spectre simulator with an I3T25 process design kit) and experimental results (see Appendix A). AC transfer responses and impedance plots were obtained by an HP 4395 A (a vector network analyzer) and an Agilent 4294 A (an impedance analyzer). Note that the power supply voltage had a nominal value of ±1.65 V in all simulations and experiments. The overall quiescent power consumption of the whole IC was maximally 45 mW. Figure 1 shows the contents of the IC package and an illustration of the designed top layout, with dimensions of 1526 × 1526 μm.

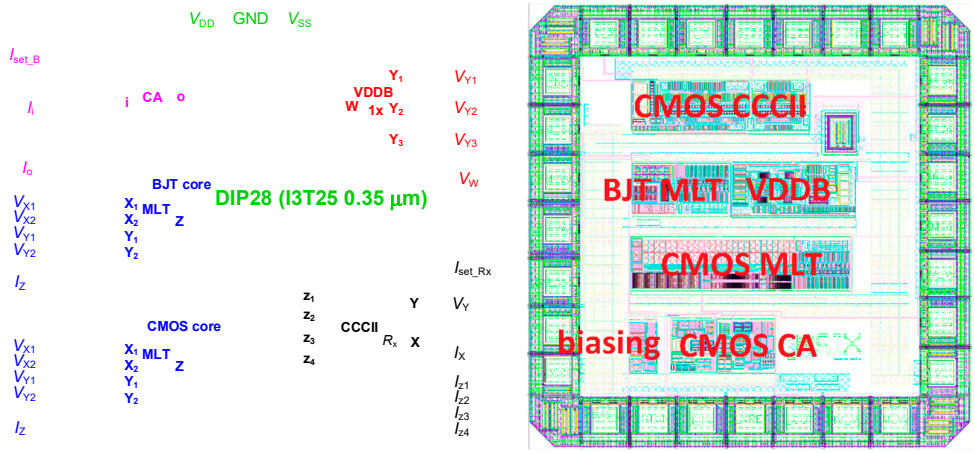

Figure 1. The fabricated IC: (left) contents on a cell level and (right) an illustration of the top layout design.

3.1. Voltage Differencing Differential Buffer (VDDB)

A folded cascode design of an OA [45,46] served as inspiration for the design of the VDDB (see Figure 2). In this active subpart, a full negative feedback was established. Three input voltages at high-impedance inputs, marked as V_{Y1}–V_{Y3}, are processed to the output low-impedance terminal V_W according to the following formula:

$$V_{Y1} - V_{Y2} + V_{Y3} = V_W \,. \tag{1}$$

The proposed CMOS topology, including the designed aspect ratios of transistors (W/L) and bias conditions, is shown in Appendix A (Figure A1).

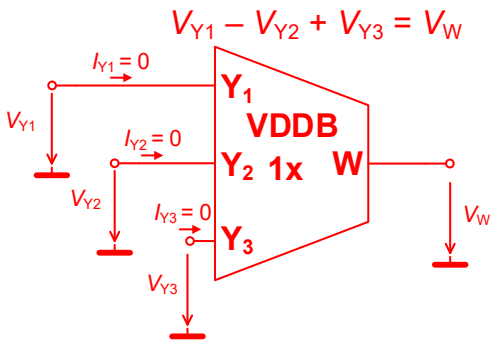

Figure 2. Schematic symbol and interterminal transfer relation of the voltage differencing differential buffer (VDDB).

3.2. Voltage Multipliers with Current Output (CMOS MLT, BJT MLT)

This cell (see Figure 3 (left)) enables the multiplication of two differential input voltages (requiring two pairs of terminals: V_{X1}, V_{X2} and V_{Y1}, V_{Y2}) in the form of output current I_Z. It has beneficial features for circuit synthesis, especially for the construction of lossy and lossless integrator blocks [21] employing grounded capacitors.

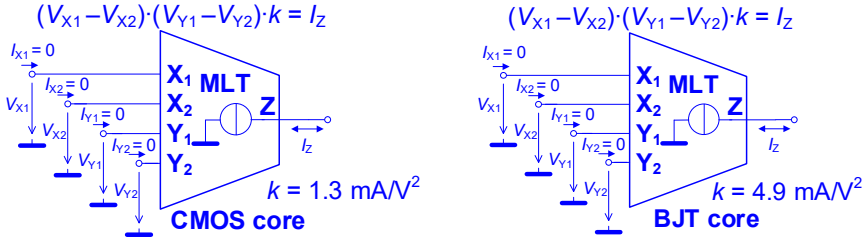

Figure 3. Schematic symbol and description of the ideal interterminal transfer relation of the voltage multiplier to the current output CMOS MLT (left) and BJT MLT (right).

The bidirectional arrow at the output indicates that both polarities of the output current are possible. This topology consists of a linearizing section, a multiplying core and an additional output stage to boost the output current. The most similar solution can be found in Reference [48], but without linearizing sections (see Figure A2 in the Appendix A). The linearizing blocks increase linearity through the input voltage range but also decrease the level of output current. Here, the output current swing is limited to ±low tens of μA. The issue of limited output swing can be solved by the increased gain factor of current mirrors. Such a step significantly degrades the bandwidth of the MLT (increasing area of gate = increasing gate capacity). Therefore, our topology for the CMOS MLT contains two output resistive loads (not used in Reference [48]) and includes additional "current-boosting" OTA stage for amplification and then conversion of voltage difference at these loads to current at the output terminal. The only similarity between our concept and the previous one [48] can be found in the multiplying core. However, it was redesigned for our purposes, with different aspect ratios of transistors designed with different technology. The ideal transfer relation between input voltage pairs and output current has a form,

$$(V_{X1} - V_{X2})(V_{Y1} - V_{Y2})k = I_Z, \quad (2)$$

where k is a constant given by technological parameters, designed aspect ratios of specific transistors, and circuit components of internal topology (see Figure A2 in Appendix A).

The experimental analysis of the CMOS MLT revealed a large impact of fabrication mismatches on its performance. In some applications, different MLT cells having a high value of transconductance constant k could be useful. In order to significantly increase the value of k, a BJT solution as a core part of the MLT seemed to be promising. Therefore, a standard bipolar Gilbert core

[49] (see Figure A3 in Appendix A) of the multiplier (BJT MLT), shown in Figure 3 (right), could be useful because of its beneficial features. The same "boosting" OTA stage serves the same purpose as in the case of the CMOS MLT. Moreover, differences between the simulation and measurement results (including fabrication mismatches) were expected to be not so significant in this case (see the results in sub-section 4.2 and Tables A2 and A3 in Appendix A). Therefore, a BJT MLT was also included in our IC. The ideal transfer relation is identical to Equation (2), but the values of k are different.

3.3. Current-Controlled Current Conveyor of the Second Generation (CCCII)

The CCCII is a very important part of the integrated device (and it also occupies a large part of the chip area). It addresses the requirement for an active cell suitable for current-mode signal processing and therefore for providing multiple current outputs. It offers the mentioned useful features as well as intentional electronic control of the resistance of current input terminal X (Figure 4). We selected the topology of a differential pair with full negative feedback, similarly to References [45,46,50]. The current output terminals of the fabricated cell were based on cascoded current mirrors (Figure A4 in Appendix A) in order to reduce systematic and matching DC offsets and inaccuracies.

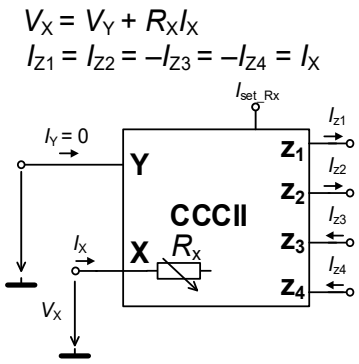

Figure 4. Schematic symbol and description of the ideal interterminal transfer relations of the current-controlled current conveyor of the second generation (CCCII).

3.4. Current Amplifier with Controllable Current Gain (CA)

The adjustable current gain of the CA is a very useful feature in the synthesis of current and mixed mode circuits. Figure 5 shows the single-input single-output concept of this cell available in the designed IC device. Its topology is shown in Figure A5 in Appendix A. Parameter B represents the electronically adjustable current gain as a relation between the input and the output current ($I_o = B \cdot I_i$).

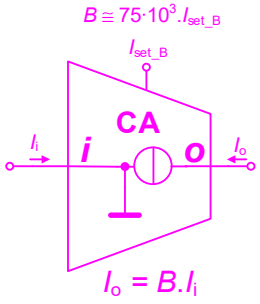

Figure 5. Schematic symbol and description of the ideal interterminal transfer relations of the adjustable current amplifier (CA).

4. Experimentally Tested Features of the Proposed Cells

In this section, performances of the proposed cells of the manufactured IC device are presented. For this purpose, results selected from the simulations and measurements are presented and discussed. The complete analysis is available in Appendix A (see Tables A1–A5).

4.1. The VDDB

Compared to previous implementations [47] and references cited therein, the most important features of this device are as follows: Favorable dynamics (±700 mV), very high resistance of voltage inputs (100 MΩ), total harmonic distortion (THD) lower than 0.5%, and a frequency bandwidth higher than 45 MHz for all possible transfers from input(s) to output (see Figure 6). The output impedance was very low (<1 Ω) at low frequencies. It started to increase above 10 kHz (<10 Ω at 1 MHz), which is common behavior for such a topology. The printed circuit board (PCB) used for the experimental measurements caused increasing terminal and nodal parasitic capacities (about 10–15 pF higher than expected from simulations). It was valid for all experimental results presented in this work. An overview of the simulation and experimental results is summarized in Table A1 (see Appendix A).

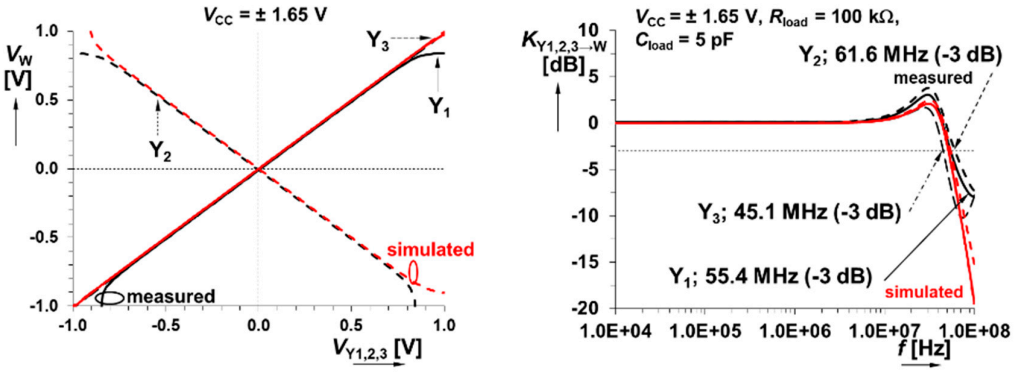

Figure 6. Selected results of the measured and simulated responses of the VDDB: (left) DC transfer responses *Y*1–3 → *W*; (right) magnitude AC transfer responses *Y*1–3 → *W*.

4.2. The CMOS MLT and BJT MLT

The features of the multiplier were tested in the form of emulating behavior of the OTA in two configurations: (1) the X_2, Y_2 terminals are grounded, X_1 (signal input), Z (signal output ($X_1 \rightarrow Z$, indicated in Table A2)), and Y_1 (DC driving voltage); and (2) Y_1 (signal input), Z (signal output ($Y_1 \rightarrow Z$, indicated in Table A3)), X_1 (DC driving voltage), and X_2, Y_2 are grounded. This configuration actually extended the concept of an OTA [21,22] because the operation of multiplication could be used for a simple change in the polarity of the output current. Table A2 indicates the expected differences between the simulated and measured transconductance values (g_{m-s}). These differences were mainly caused by different values of k in the case of simulation ($k \cong -1.8$ mA/V²) and measurement ($k \cong -1.3$ mA/V²). This parameter significantly depended on temperature and fabrication mismatches. The inaccuracy resulted from a variation in the transconductance parameters of partial transistors (thermal voltage) and the non-equal bulk and source voltages (the threshold voltage is influenced) of differential pairs. The design recommendations of the CMOS process supposed that bulks are connected to the highest (P-type/channel MOS) or the lowest (N-type/channel MOS) voltage potentials in the circuit. Therefore, all bulks of NMOS elements are connected to negative supply voltages, and bulks of PMOS types are connected to positive supply voltage. Note that the dispersion of k was predicted from so-called process corner, supply voltage, and temperature variation (PVT) analyses. The experimentally obtained value fell into the expected range of possible deviation (see Figure 7). High input impedances (100 MΩ) represent an important advantage of this cell. In real experiments, the driving of transconductance was possible up to 660 μS. Deviation from the maximum simulated value (about 1000 μS) was given by the uncertainty of k.

This was acceptable when fabrication mismatches were considered. The output impedances (real parts) remained above 100 kΩ for the highest value of driving DC voltage V_X (the worst case). The measured linear dynamic input range was ±500 mV. The THD of the CMOS MLT reached, maximally, 1.5%. This was higher than in the case of the VDDB, but was still very acceptable.

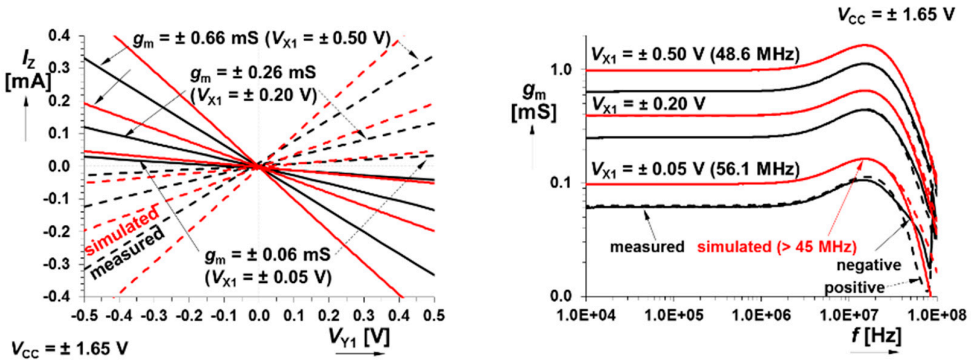

Figure 7. Selected results of the measured and simulated responses of the CMOS MLT: (left) DC transfer responses $Y_1 \rightarrow Z$ for a V_{X1} controlled by DC voltage; (right) magnitude of AC transfer responses $Y_1 \rightarrow Z$ for a V_{X1} controlled by DC voltage.

Compared to the CMOS MLT solution, the BJT core of the MLT substantially improved the performance of the DC accuracy and k. The transconductance constant value reached $k \cong 4.8$ mA/V^2 (simulated) and $k \cong 4.9$ mA/V^2 (measured). The obtained results (simulation and measurement), summarized in Table A3 (see Appendix A), indicated better accuracy and correspondence of simulated and measured transfer responses than in the case of the CMOS MLT. In comparison to the CMOS MLT solution, this represents a very important advantage. Input impedances achieved lower values in the BJT case (due to the bipolar input stage), but they were still sufficiently high for most of the applications. The input dynamic range with linear behavior was slightly higher, ±600 mV and ±700 mV in the simulation and from measurement, respectively. The frequency bandwidth of only 39 MHz could be considered to be some kind of limitation in particular cases, but it was obtained for a very low driving voltage. The range of possible transconductance controls was wider (measuring up to 2400 μS) than in the case of the CMOS MLT (measuring up to 660 μS). The output resistance achieved values >100 kΩ (even for the highest control voltages). The THD values were similar to the previous case. Exemplary DC and AC transfer responses are plotted in Figure 8.

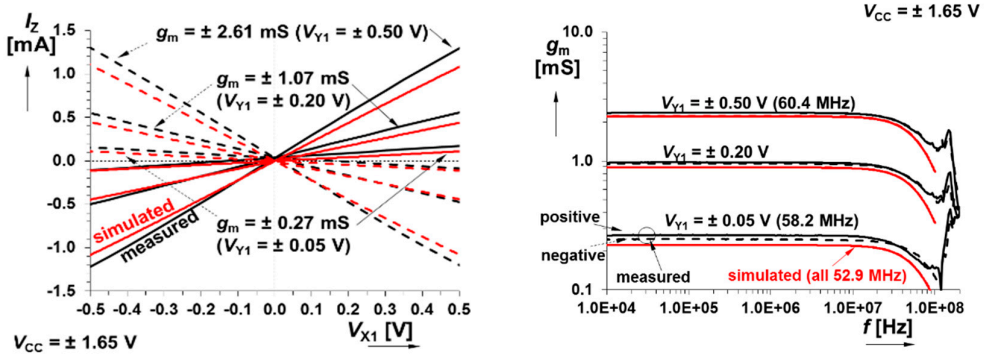

Figure 8. Selected results of the measured and simulated responses of the BJT MLT: (left) DC transfer responses $X_1 \rightarrow Z$ for a V_{Y1} controlled by DC voltage; (right) magnitude of AC transfer responses $X_1 \rightarrow Z$ for a V_{Y1} controlled by DC voltage.

4.3. CCCII

All-important results are summarized in Table A4 (see Appendix A). Dynamic ranges of the current transfers ($X \rightarrow Z_{1–4}$) of the CCCII cell were from ±80 μA up to ±1700 μA, depending on the bias current I_{set_Rx} (driving R_X as $R_X \cong 3.5 \cdot I_B^{-1/2}$). Correspondence between Cadence and the experimental results in most of the DC/AC parameters was relatively high. In the worst case, the lowest usable frequency bandwidth was 37 MHz, but it was possible to reach 50 MHz for the highest I_{set_Rx} at specific transfers.

The input impedance (Y terminal) again reached very high values (100 MΩ), and the output impedances were acceptable (>60 kΩ) even for the maximal I_{set_Rx} setting (the worst case). Note that quite large levels of currents were supposed to be processed. Therefore, quiescent DC bias currents in the branches of the output stages were also quite high (hundreds of μA). The THD levels were maximally up to 0.1%. Selected features of the CCCII are shown in Figure 9.

It is worth noting that the dependence of R_X (simulation: from 2320 Ω → 240 Ω) on I_{set_Rx} (see Table A4) was visible from 5 μA to 350 μA, but there was a significant difference between the simulation and measurement results. This was caused by a natural and expected change in the operation regime of transistors in the structure (the starts of this change in the case of simulations and in the case of a real circuit were different).

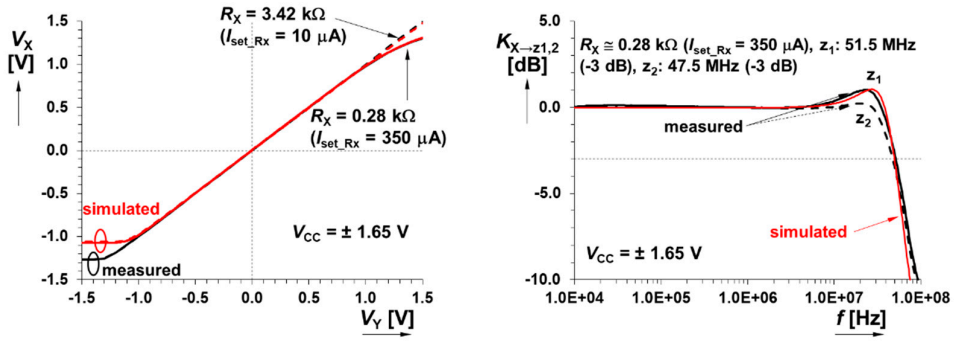

Figure 9. Selected results of the measured and simulated responses of the CCCII: (left) DC response of the $Y \rightarrow X$ transfer; (right) AC responses of $X \rightarrow z_{1–2}$ transfers.

4.4. CA

Table A5 (see Appendix A) describes all-important features of the CA. The current gain (a constant between the output and input current) was defined as $B \cong 75 \cdot 10^3 \cdot I_{set\_B}$ and could be adjusted by the DC driving current I_{set_B}. The linearity of the DC transfer response was excellent (despite dynamics limited to ±200 μA), as well as input and output resistances are/were too. However, this cell targets low-power applications (the main purpose) and not speed. The frequency features of this cell were the worst from all units included in our IC (not overcoming 1.6 MHz, see Figure 10 (left)). A comparison of the real behavior of the CA cell (see Table A5) to Cadence design (nominal) showed the inaccuracy of DC as well as AC performances (Figure 10), especially for higher values of driving current I_{set_B}. Its power consumption was the lowest of all of the designed cells (at least five times). This is the reason why this cell is appropriate for low-power applications. The current gain control was designed for an I_{set_B} current (maximally 15 μA). Differences between the simulation and measurement results for $I_{set\_B} > 15$ μA are given through uncertainty of the setting of the operational regime of particular transistors in the topology (simulations). The evaluated distortion was not higher than 0.6% in the case of this cell.

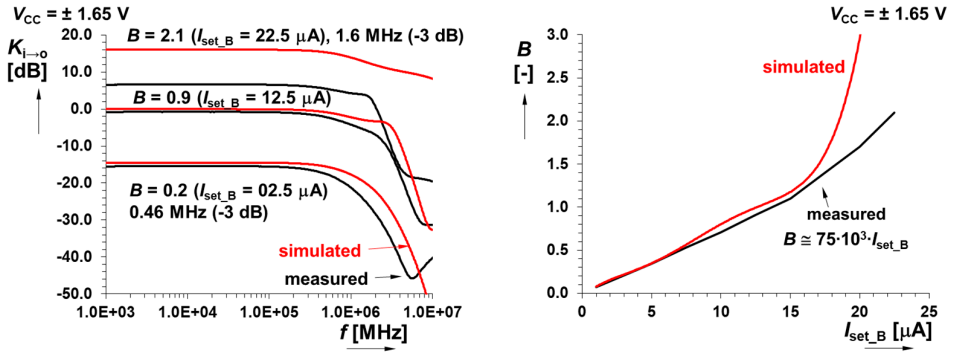

Figure 10. Selected results of the measured and simulated responses of the CA: (left) AC responses of $i \to o$ transfers; (right) dependence of B on I_{set_B}.

5. Example Interconnection of Internal Cells: A Novel Advanced Active Element

Internal cells (the VDDB, CCCII, CMOS MLT, BJT MLT, and CA) of the developed integrated device may be interconnected externally in order to create many types of advanced AEs. The principle of "modular approach" was presented in the overview of standard, modern and newly defined AEs. Their role in new proposals has been discussed in literature. For more details, see References [3,13]. The following text presents one possible novel configuration and interconnection of internal cells in accordance with the principle and methodology introduced in Reference [13].

Figure 11 shows the concept of an advanced AE that has three independently adjustable parameters, namely g_{m1}, R_X, and g_{m2}. Note that the outer terminals of the AE are distinguished from inner (cell) terminals by the symbol " * ". This AE is characterized by the following operation. MLT_1 transforms the differential input voltage from the p^* and n^* terminals to the current (through the controllable transconductance, g_{m1}) flowing out of the auxiliary terminal z_{a^*} ($I_{Za^*} = \pm (V_{p^*} - V_{n^*}) \cdot g_{m1}$). The voltage input Y of the CCCII is connected to this terminal to process the voltage drop at external impedance, which is connected to this terminal. The voltage at z_{a^*} also appears at the terminal X^* (if not grounded). When the current is flowing through terminal X^*, then relation $V_{X^*} = V_{Za^*} + R_X I_{X^*}$ is valid (R_X is also electronically controllable). The CCCII creates a direct copy of I_{X^*} ($I_{Zb^*} = I_{X^*}$) at the second auxiliary terminal, marked as Z_{b^*}. The voltage drop obtained at the external impedance, connected to this terminal, is again transformed to the current. It flows from MLT_2 (where the third controllable parameter g_{m2} is available) at the x^* terminal ($I_{x^*} = \pm V_{Zb^*} \cdot g_{m2}$). Note that the implementation of the MLTs in the AE concept allows for a simple change of polarity for the output currents I_{Za^*}, I_{Zb^*}, and I_{x^*} (i.e., transconductance polarity). We refer to this device as a current-controlled voltage differencing current conveyor transconductance amplifier (CC-VDCCTA).

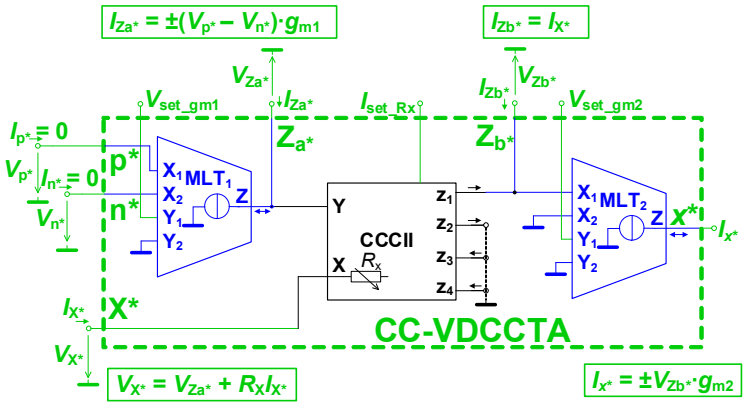

Figure 11. Example of the interconnection of three cells of the fabricated IC, defining an advanced active element (AE) with three adjustable parameters: a so-called current-controlled voltage differencing current conveyor transconductance amplifier (CC-VDCCTA).

5.1. Application Example: CC-VDCCTA-Based Quadrature Oscillator

A simple oscillator enabling the linear tunability of frequency (oscillations) can be realized by utilizing a single CC-VDCCTA (see Figure 11) and four passive components. Its circuit is plotted in Figure 12. The characteristic equation has the following form:

$$s^2 + \frac{(1 - Rg_{m2})}{C_2 R} s + \frac{g_{m1}}{C_1 C_2 (R_X + R_{ext})} = 0, \quad (3)$$

where the condition for oscillation (CO) is fulfilled at $R.g_{m2} \geq 1$. The frequency of oscillation (FO) and the relation between generated signals are given respectively by Equations (4) and (5).

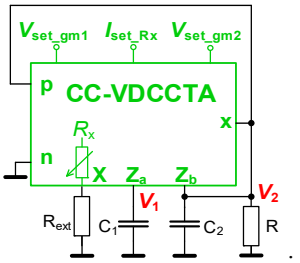

Figure 12. A simple electronically and linearly tunable quadrature oscillator based on CC-VDCCTA.

Equations (4) and (5) have simple expressions:

$$\omega_0 = \sqrt{\frac{g_{m1}}{C_1 C_2 (R_X + R_{ext})}}, \quad (4)$$

$$\frac{V_1}{V_2} = \frac{-g_{m1}}{sC_1}\bigg|_{s=j\omega_0} \Rightarrow \quad \frac{V_1}{V_2} = j\sqrt{(R_X + R_{ext})\, g_{m1}}. \quad (5)$$

Simultaneous adjustment of $R_X + R_{ext}$ and g_{m1} ($g_{m1} = 1/(R_X + R_{ext})$) ensures linear tuning of the FO while keeping output levels constant with the quadrature phase shift during the tuning process. Parameters g_{m2} or R are suitable for automatized CO control (amplitude stabilization). Note that the circuit is able to operate without external R_{ext}. However, direct grounding of the X terminal of the CC-VDCCTA causes operation with lower linearity. Therefore, THD also increases significantly. A small value of R_{ext} increases linearity and the dynamics of signal processing.

The features of the proposed circuit were verified by Cadence Spectre simulations and by laboratory experiments, in which a real fabricated IC device was used. An Agilent 4395A network/spectrum/impedance analyzer and a DS1204B oscilloscope were used for these purposes. Figure 13 depicts the PCB realized for verification purposes. There were several auxiliary circuits on this PCB, including voltage buffers, in order to optimize output (for measurement purposes) with a 50-Ω load (Agilent 4395A).

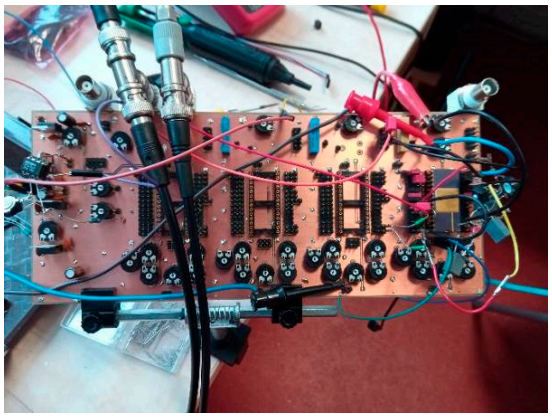

Figure 13. PCB for experimental verification of applications with fabricated chips shown in case of using only one IC package as discussed in the paper (implementation of the designed oscillator.

A practical example of the design of the above-described oscillator starts with the following parameters: f_0 = 159 kHz (oscillation frequency), $C_1 = C_2 = C$ = 1 nF, R_x = 420 Ω (I_{set_Rx} = 100 μA), R_{ext} = 82 Ω, and R = 4.7 kΩ. Next, calculations from Equation (4) lead to g_{m1} = 1 mS (V_{set_gm1} = 0.2 V). We designed and realized an amplitude stabilization circuit (CO control) of this oscillator (see Figure 14) based on the regulation of R. It was supplied from the node of C_2 and was used in all experimental tests. The circuit contained a high-input impedance adjustable amplifier with an OA and a voltage doubler/multiplier controlling the junction field effect transistor (J-FET)-based controllable resistor connected to the node of C_2 (in parallel to R = 4.7 kΩ). The value of g_{m2} was kept to about 540 μS (V_{set_gm2} = 0.3 V). The measured waveforms and their spectral analyses are shown in Figure 15.

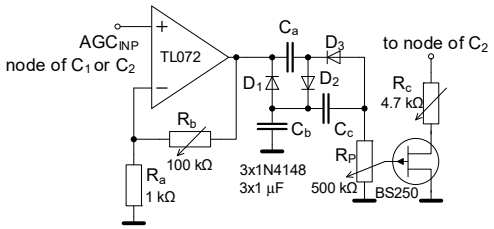

Figure 14. System for amplitude stabilization of the designed oscillator used in the experiments.

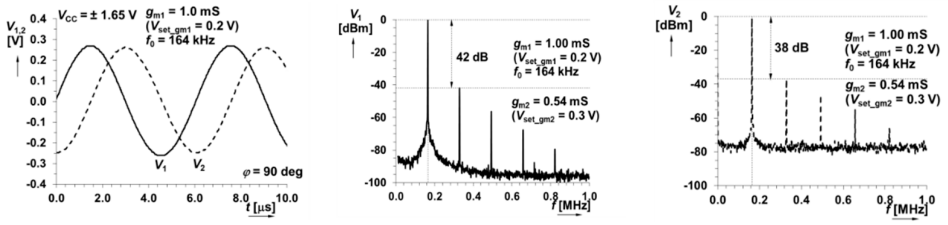

Figure 15. Experimental results for the oscillator: (left) output waveforms; (middle) spectral analysis of V_1; (right) spectral analysis of V_2.

The limited bandwidth and parasitic features of the AEs do not influence the considered low-frequency design significantly. This was confirmed by experimental measurements in the time domain (see Figure 15), where we obtained f_0 = 164 kHz (very close to the expected 159 kHz). A spectral analysis yielded THD values of 0.8% and 1.3% (obtained for V_1 and V_2, respectively).

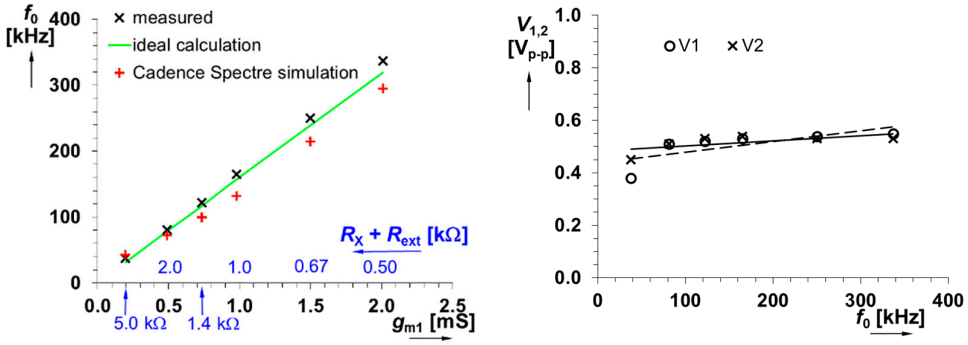

Figure 16. Measured dependences with linear tuning of the frequency of oscillation (FO) of the oscillator: (left) f_0 versus simultaneous control of g_{m1} (V_{set_gm1}) and R_X (I_{set_Rx}); (right) amplitude levels of V_1 and V_2 versus f_0.

Figure 16 (left) shows the character of tunability and behavior of the output responses when f_0 is tuned by g_{m1} (V_{set_gm1}) and R_X ($R_X + R_{ext}$) simultaneously. Note that the low value of R_{ext} = 82 Ω in these tests kept R_X as a dominant source in the adjustment of f_0. The value of $R_X + R_{ext}$ (connected actually in a series) was set from 500 Ω to 5 kΩ (I_{set_Rx} = 100 → 10 μA), and the value of g_{m1} was adjusted in the opposite direction, from 196 μS to 2 mS (V_{set_gm1} = 0.041 → 0.41 V). When this setting was considered, the oscillator offered an ideal tuning range for the FO: f_0 = 32 kHz → 319 kHz (10:1). Cadence simulations yielded tunability from 43 kHz to 295 kHz (7:1), and the laboratory experiments provided the adjustment between 38 kHz and 337 kHz (9:1). The phase shift fluctuated around 90°, with a maximal deviation of ±2° in these bands. The amplitude levels, as well as their ratio, were almost constant during the measured FO tuning (see Figure 16 (right)).

The benefits of the proposed oscillator (available simultaneously) were as follows: (a) all passive elements were grounded, (b) simple electronic controllability, (c) a linear type of tunability, (d) a fully uncoupled FO and CO, (e) two possible ways (driving of g_{m2} or R) for the implementation of the system for automatic amplitude stabilization, and (f) constant output levels and phase shift when oscillation frequency was tuned.

Table 2 compares the features of our design to relevant solutions of similar oscillators (single advanced AE-based circuits). Based on an analysis of the considered concepts, the solution in Reference [56] offered the most similar features. However, the option of tunability was not tested, electronic linear tunability was not even possible, and electronic control of internal R_X in the AE was not supposed. Interesting features were also available in the case of the solution presented in Reference [55]. However, this oscillator did not provide quadrature outputs with constant signal levels (when FO was tuned)

Table 2. A comparison of recently published and the most similar electronically controllable quadrature oscillators based on a single active element and a grounded capacitor.

References	Active Elements	No. of Auxiliary High Impedance Terminals *Z*	No. of Controllable Parameters of Device	No. of Passive Elements	Parameters for f_0 Control	Trend of Electronic Tunability	Fulfillment of CO Given by Parameter	No. of Parameters Suitable for CO Control	FO and CO Fully Uncoupled	Constant Output Amplitude While f_0 Is Tuned	Chip Area/Cell Area (mm^2)	Power Consumption (Full IC/ Cells) (mW)
[36]	VDCC	1	2	4	g_m	nonlinear	*R* value[a]	1	Yes	No	4/0.79	-/45
[55]	ZC-CG-VDCC	1	3	4	g_m, R_X	linear	*B*	1	Yes	No[b]	N/A	-/7
[56]	VDTA	1	2	3	g_m	nonlinear	*R* value[a]	1	Yes	No	N/A	N/A
[57]	DVCCTA	1	1[c]	5	g_m, R_X	N/A	*R* value[a]	2	Yes	N/A	N/A	N/A
[58]	DDTA	1	1	3	g_m	nonlinear	*C* value	0	No	N/A	N/A	N/A
Figure 11	CC-VDCCTA	2	3	4	g_{m1}, R_X	linear	g_{m2}, *R* value[a]	2	Yes	Yes	2.34/0.35	45/34

Notes: CC-VDCCTA: current-controlled voltage differencing CCTA; DDTA: differential difference transconductance amplifier; DVCCTA: differential voltage current conveyor transconductance amplifier; VDCC: voltage differencing current conveyor; VDTA: voltage differencing current conveyor; ZC-CG-VDCC: Z-copy controlled gain VDCC; N/A: not available, not solved, or not tested; g_m: transconductance; R_X: resistance of current input terminal; *B*: adjustable current gain. [a] Value of passive element. [b] Multiphase type of oscillator where quadrature output is also available: However, constant amplitudes (when tuned) are generated only with a 45°phase shift. [c] R_X not implemented in the AE as electronically controllable (R_X = external passive element), and electronic FO tunability available in nonlinear form only (but not tested).

The use of several internal cells in a frame of the single IC package may indicate that the implementation of simple OTA cells (for instance, the well-known solution from References [59,60]) brings simpler topologies of linearly tunable oscillators. Based on the comparison of the structure from Figure 12 (including three adjustable internal cells) and solutions of the oscillators, shown in References [59,60], we can assess that three OTAs (having three g_m parameters) are not sufficient for fully linear tuning of frequency of oscillations even when we accept an unfavorable disturbance of the ratio of output amplitudes during the tuning procedure. The quadrature and linearly tunable solutions, employing OTAs, require at least four active devices (see Reference [59]) and, in addition, also an amplitude stabilization (AGC) as a circuit. From the viewpoint of the number of active devices, our solution brings a reduction in the needed number of active devices (when internal IC cells are counted as discrete parts).

Many applications require several current outputs (implementation of OTAs [3,4,13]). In Reference [54], a perfect example of the synthesis of a multiphase oscillator requiring an active device with several current output terminals was presented. A similar thing can be ensured in our IC modular approach when the CCCII cell is used as a current distributor [16] (Y terminal connected to the ground and current I_{set_Rx} is adjusted to the highest value in order to obtain the lowest R_X value). This current distributor extends the number of output currents of both polarities when it is connected through the X terminal to the current output z of the MLT (forming the OTA part) in the IC package.

6. Conclusions

The presented concept of "modular approach" leads to interesting constructions of advanced AEs, which have multiterminal and multiparameter (single, two, three, or four independently controllable parameters) features. Several of them have already been defined in Reference [13]. However, many of them have not been presented in the literature until now. A fabricated IC device allows various implementations of AEs in different systems of continuous analog and mixed signal processing. Frequency features of cells (units and tens of MHz), given significantly by the used technology I3T25, predetermine the proposed systems for operation to up to hundreds of kHz and units of MHz, with sufficient dynamic ranges of the processed signals. A brief comparison of the most important features of the proposed active cells is presented in Table 3.

Table 3. Brief comparison of the selected important measured features of the proposed cells included in the IC.

Cell	Frequency Features (Bandwidth)[a]	DC Features and Linearity (Dynamics)	Input Impedance	Output Impedance	Quiescent Power Consumption [a]	Accuracy of Simulation Results with Results of Experiments (Design Stage)
VDDB	Good (>45 MHz)	Good (±700 mV)	High (100 MΩ)	Low (good) (0.5 Ω)	Average (9.1 mW)	High
CMOS MLT	Average (>30 MHz)	Good (±500 mV)	High (100 MΩ)	Average (>100 kΩ)	Average (7.8 mW)	Within expected range (process variation)
BJT MLT	Good (>40 MHz)	Good (±700 mV)	Average (170 kΩ)	Average (>100 kΩ)	Average (9.5 mW)	Good
CCCII	Good (>37 MHz)	Good (±500 mV, Y) (to ±1700 μA, X)	High (100 MΩ, Y) Average (0.28 → 3.4 kΩX)	Average (>60 kΩ)	High (16.8 mW)	Good
CA	Low (<1.6 MHz)	Average (but excellent linearity) (±190 μA)	Low [b] (1.4 Ω)	High (good) (>3 MΩ)	Low (1.7 mW)	Average

Notes: All numerical results are measured values; [a] in frame of the IC device; [b] this is a significant advantage in the case of CA.

The proposed and realized AEs can be easily applied in the field of analog signal processing (synthetic immittance functions, filters, oscillators, etc.). The functionality of the modular design of AEs was verified, and one application example (an oscillator) of a newly defined concept (CC-VDCCTA) was presented in this paper in detail. Smooth operating and real measurement results, in comparison to theory and expectations, confirmed the suitability of the modular approach in the development of new circuit applications.

This paper showed and explained the results and performances of all of the designed cells. An application example actually utilized only a part of them. The employment of more cells or different combinations of cells goes beyond the aims of this paper and is a topic of our future research. Nevertheless, the presented example sufficiently explains the purpose of the developed IC (assembly and implementation of advanced AEs) and indicates how the new (or modified) advanced AE can be usefully utilized in an application. This application example was selected because of the usefulness of several adjustable parameters for tunability purposes of the oscillator.

Author Contributions: Conceptualization, R.S. and J.J.; methodology, R.S., R.P., and V. K.; validation, R.S. and R.P.; formal Analysis, R.S. and J.J.; investigation, R.S., R.P., and V.K.; writing—original draft preparation, R.S., J.J., and L.P.; writing—review and editing, R.S., J.J., and L.P.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

This appendix includes the integrated internal topologies of the proposed cells of the manufactured IC device. Furthermore, their performance analyses (simulation versus measurement) are presented in detail.

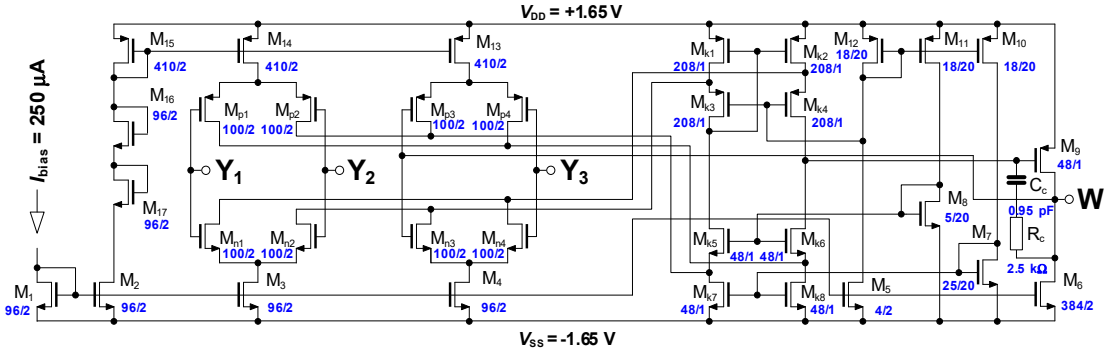

Figure A1. Full CMOS topology of the voltage differencing differential buffer (VDDB).

Table 1. Summary of simulated and measured performances of the VDDB cell. THD: total harmonic distortion.

Parameters/Conditions	Simulation Results (Nominal Run)	Measured Results	Error (Measured vs Simulated)	Design Target
Small-signal AC transfer				
$K_{Y1} \rightarrow_W$ (−3 dB)	1.00 [-] (51.6 MHz)	1.02 [-] (55.4 MHz)	+2% (+7%)	1 (≥30 MHz)
$K_{Y2} \rightarrow_W$ (−3 dB)	1.00 [-] (54.3 MHz)	1.02 [-] (61.6 MHz)	+2% (+13%)	1 (≥30 MHz)
$K_{Y3} \rightarrow_W$ (−3 dB)	1.00 [-] (51.3 MHz)	1.01 [-] (45.1 MHz)	+1% (−12%)	1 (≥30 MHz)
Input dynamic range				
$Y_{1,2,3} \rightarrow W$	≥ ±700 mV	≥ ±700 mV	0%	≥±500 mV
Input DC offset (Monte Carlo)				
	systematic + statistical (mismatch, 3 sigma; 99.7%)	real		
$Y_{1,3} \rightarrow W$	−0.57 ± 20.5 mV	|10| mV	expected statistical range	-
$Y_2 \rightarrow W$	−0.57 ± 20.5 mV	|10| mV	expected statistical range	-
Total harmonic distortion (for input voltage 500 mV_{pk-pk}, 1 kHz)				
$THD_{Y1,2,3 \rightarrow W}$		<0.10%	-	<1%
Terminal impedances				
$R_{Y1,2,3}$, $C_{Y1,2,3}$	≥1 GΩ 2.8 pF	100 MΩ13 pF	-	>50 kΩ
R_W, L_W	0.37 Ω 4.3 µH	0.54 Ω 4.3 µH	-	<10 Ω
measured quiescent power consumption: 9.1 mW				

Basic principle: The topology of the VDDB included an OA-based folded cascoded core. The difference between the standard topology in References [45,46] and our proposal consisted of the following: (a) additional differential NMOS and PMOS pairs ($M_{p3–4}$, $M_{n3–4}$) were used to obtain two additional voltage inputs, where one of them was used for full negative feedback. The low-impedance voltage output was solved as a class A source follower (M_9).

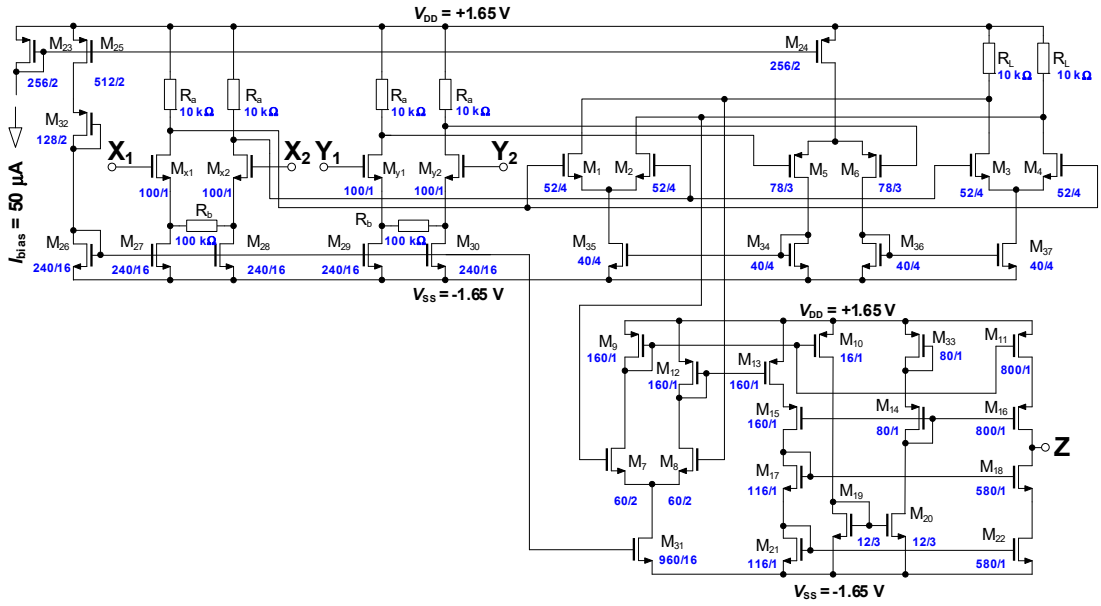

Figure A2. Full CMOS topology of the voltage multiplier with current output (CMOS MLT).

Table A2. Summary of simulated and measured performance of the CMOS MTL cell.

Parameters/Conditions	Simulation Results (Nominal Run)	Measured Results	Error (Measured vs Simulated)	Design Target
Small-signal AC transfer				
$g_{m(X1 \rightarrow Z)}$ (−3 dB) for V_{Y1} = ±0.05 → ±0.50 V	±98 → ± 975 µS (≥53.0 MHz)	±45 → ± 650 µS (≥30.0 MHz)	−54% → −33% (−43%)	≥100 µS → ≥ 1000 µS (≥30 MHz)
$g_{m(Y1 \rightarrow Z)}$ (−3 dB) for V_{X1} = ±0.05 → ±0.50 V	±98 → ± 980 µS (≥44.0 MHz)	±60 → ± 665 µS (≥44.0 MHz)	−39% → −32% (0%)	≥100 µS → ≥ 1000 µS (≥30 MHz)
Input DC dynamic range				
$X_1 \rightarrow Z$ for V_{Y1} = ± 0.05 → ± 0.50 V	≥±500 mV	≥±500 mV	0%	≥±500 mV
$Y_1 \rightarrow Z$ for V_{X1} = ± 0.05 → ± 0.50 V	≥±600 mV	≥±600 mV	0%	≥±500 mV
Input DC offset (Monte Carlo)				
	systematic + statistical (mismatch, 3 sigma; 99.7%)	real maximum		
$X_1 \rightarrow Z$ for V_{Y1} = ± 0.5 V	3.3 ± 63 mV	|6| mV	expected statistical range	-
$Y_1 \rightarrow Z$ for V_{X1} = ±0.5 V	3.2 ± 66 mV	|18| mV	expected statistical range	-
Total harmonic distortion (for input voltage 500 mV_{pk-pk}, 1 kHz)				
$THD_{X1 \rightarrow Z}$ for V_{Y1} = ± 0.1 V		≤0.16%	-	<1%
$THD_{X1 \rightarrow Z}$ for V_{Y1} = ± 0.5 V		≤0.14%	-	<1%
$THD_{Y1 \rightarrow Z}$ for V_{X1} = ± 0.1 V		≤1.45%	-	<1%
$THD_{Y1 \rightarrow Z}$ for V_{X1} = ± 0.5 V		≤0.45%	-	<1%
Terminal impedances				
R_{X1}, C_{X1} for all V_{Y1}	≥1 GΩ 2.5 pF	100 MΩ 10–24 pF	-	>50 kΩ
R_{Y1}, C_{Y1} for all V_{X1}	≥1 GΩ 2.5 pF	100 MΩ 14 pF	-	>50 kΩ
R_Z, C_Z for V_{X1} = ± 0.50 V	1.55 MΩ 5.3 pF	≥100 kΩ 16.2 pF	-	>50 kΩ
measured quiescent power consumption: 7.8 mW				

Basic principle: Two input differential voltages were processed by linearizing segments ($M_{x1\text{-}2}$ and $M_{y1\text{-}2}$) in order to extend the linear range of the DC transfer. Each linearizing segment worked as an operational transconductance amplifier with very low but highly linear (from the viewpoint of signal level) transconductance (practically given by degradation resistor R_b, and therefore high linearity between the input differential voltage and the output current was ensured) with a differential current output that performed differential output voltage at two identical resistive loads. Then, both output voltages were connected to the multiplying core (the basic concept introduced in Reference [48]). A boosting OTA section (differential pair $M_{7–8}$) was used because of the low output level (low gain) of the current (tens of µA instead of hundreds of µA) when the output of the multiplying core, through appropriate current mirrors, was taken directly out.

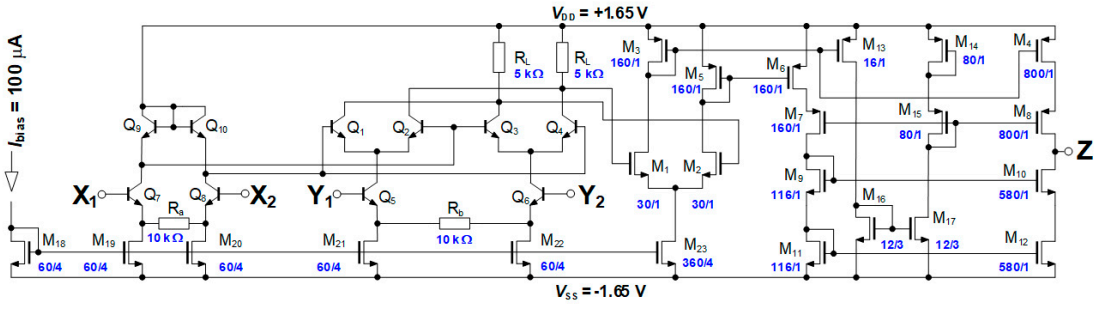

Figure 3. Full CMOS topology of the voltage multiplier with current output (BJT MLT).

Table A3. Summary of simulated and measured performances of the BJT MTL cell.

Parameters/Conditions	Simulation Results (Nominal Run)	Measured Results	Error (Measured vs Simulated)	Design Target
Small-signal AC transfer				
$g_{m\,(X1 \rightarrow Z)}$ (-3 dB) for V_{Y1} = ± 0.05 → ±0.50 V	±222 → ±2220 µS (≥53.0 MHz)	±250 → 2340 µS (≥52.0 MHz)	+13% → +5% (–2%)	±200 → ± 2000 µS (≥30 MHz)
$g_{m\,(Y1 \rightarrow Z)}$ (-3 dB) for V_{X1} = ±0.05 → ±0.50 V	±222 → ±2210 µS (≥53.0 MHz)	±250 → 2350 µ (≥39.0 MHz)	+13% → +6% (–26%)	±200 → ± 2000 µS (≥30 MHz)
Input DC dynamic range				
$X_1 \rightarrow Z$ for V_{Y1} = ±0.05 → ±0.50 V	≥±600 mV	≥±700 mV	+17%	≥±500 mV
$Y_1 \rightarrow Z$ for V_{X1} = ±0.05 → ±0.50 V	≥±600 mV	≥±700 mV	+17%	≥±500 mV
Input DC offset (Monte Carlo)				
	systematic + statistical (mismatch, 3 sigma; 99.7%)	real maximum		
$X_1 \rightarrow Z$ for V_{Y1} = ±0.5 V	−1.4 ± 29 mV	|14| mV	expected statistical range	-
$Y_1 \rightarrow Z$ for V_{X1} = ±0.5 V	−1.3 ± 29 mV	|15| mV	expected statistical range	-
Total harmonic distortion (for input voltage 500 $mV_{pk\text{-}pk}$, 1 kHz)				
THD $_{X1 \rightarrow Z}$ for V_{Y1} = ±0.1 V		≤0.32%	-	<1%
THD $_{X1 \rightarrow Z}$ for V_{Y1} = ±0.5 V		≤0.47%	-	<1%
THD $_{Y1 \rightarrow Z}$ for V_{X1} = ±0.1 V		≤0.17%	-	<1%
THD $_{Y1 \rightarrow Z}$ for V_{X1} = ±0.5 V		≤0.44%	-	<1%
Terminal impedances				
R_{X1}, C_{X1} for all V_{Y1}	129 kΩ, 2.8 pF	176 kΩ 18.3 pF	-	>50 kΩ
R_{Y1}, C_{Y1} for all V_{X1}	127 kΩ 2.8 pF	173 kΩ 15.4 pF	-	>50 kΩ
R_Z, C_Z for V_{X1} = ±0.50 V	803 kΩ 3.9 pF	≥100 kΩ 16.1 pF	-	>50 kΩ
measured quiescent power consumption: 9.5 mW				

Basic principle: This cell was prepared for high-precision applications (inaccuracies in CMOS MLT were expected). In accordance with Reference [49], a linearizing segment was applied to one differential voltage, and the linearizing procedure was different than with the CMOS MLT. It uses exponential/logarithmic dependence of the collector current on base-emitter voltage and linearization of the g_m (differential pair) stage by the degradation resistor (R_a). The attenuation of the signal through the linearizing segment was less significant than with the CMOS MLT. The boosting OTA is also presented in this case due to the same reasons as with the CMOS MLT. In our design, for the highest bandwidth, it was always better to use an additional block than increase the current mirror ratio to a value of 1:100 (a high increase in the C_{gs} parasitic capacity in the node of the current mirror and drop of bandwidth).

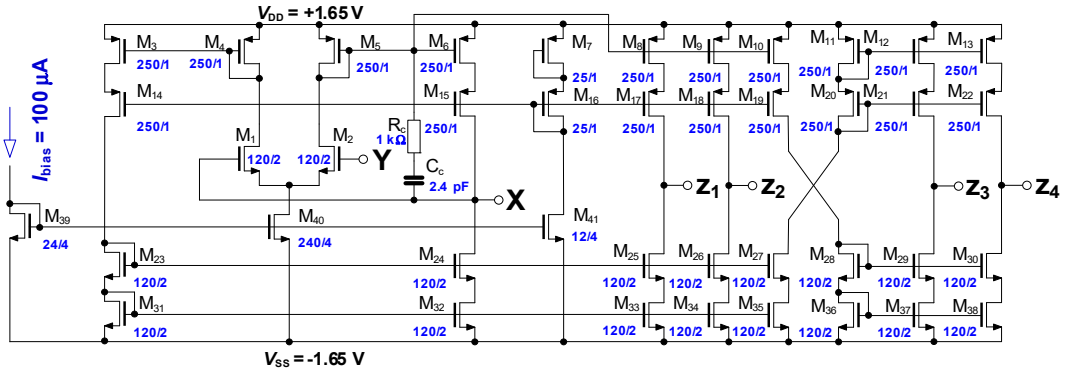

Figure A4. Full CMOS topology of the current-controlled current conveyor of the second generation (CCCII).

Table A4. Summary of the simulated and measured performances of the CCCII cell.

Parameters/Conditions	Simulation Results (Nominal Run with Input/Output Capacity 5 pF)	Measured Results	Error (Measured vs Simulated)	Design Target
Small-signal AC transfer				
$K_X \rightarrow z_1$ (−3 dB) for I_{set_Rx} = 350 μA	1.00 [-] (49.6 MHz)	0.98 [-] (51.5 MHz)	−2% (+9%)	1 (≥30 MHz)
$K_X \rightarrow z_2$ (−3 dB) for I_{set_Rx} = 350 μA	1.00 [-] (49.6 MHz)	0.98 [-] (47.5 MHz)	−2% (−4%)	1 (≥30 MHz)
$K_X \rightarrow z_3$ (−3 dB) for I_{set_Rx} = 350 μA	0.93 [-] (41.1 MHz)	1.00 [-] (37.0 MHz)	+7% (−10%)	1 (≥30 MHz)
$K_X \rightarrow z_4$ (−3 dB) for I_{set_Rx} = 350 μA	0.93 [-] (41.1 MHz)	1.00 [-] (38.7 MHz)	+7% (−5%)	1 (≥30 MHz)
$K_Y \rightarrow x$ (−3 dB) for I_{set_Rx} = 350 μA	1.00 [-] (52.1 MHz)	1.00 [-] (49.7 MHz)	0% (−5%)	1 (≥30 MHz)
$GBW_X \rightarrow z_1$ for I_{set_Rx} = 10→350 μA	12.7 → 49.6 MHz	11 → 51.5 MHz	−13% → +4%	-
$GBW_X \rightarrow z_2$ for I_{set_Rx} = 10→350 μA	12.7 → 49.6 MHz	9.8 → 47.5 MHz	−23% → −4%	-
$GBW_X \rightarrow z_3$ for I_{set_Rx} = 10→350 μA	10.8 → 41.1 MHz	7.8 → 37 MHz	−28% → −10%	-
$GBW_X \rightarrow z_4$ for I_{set_Rx} = 10→350 μA	10.8 → 41.1 MHz	8 → 38.7 MHz	−26% → −6%	-
$GBW_Y \rightarrow x$ for I_{set_Rx} = 10→350 μA	11.9 → 52.1 MHz	6.1 → 49.7 MHz	−49% → −5%	-
Input DC dynamic range				
$X \rightarrow Z_{1\text{-}4}$ for I_{set_Rx} = 10 → 350 μA	±80 → ± 1700 μA	±99 → ± 1700 μA	+24% → +0%	±100 → ±1000 μA
$Y \rightarrow X$ for I_{set_Rx} = 10,350 μA	≥±500 mV	≥±1000 mV	+100%	≥±500 mV
Input DC offset (Monte Carlo)				
	systematic + statistical (mismatch, 3 sigma; 99.7%)	real		
$X \rightarrow Z_1$ for I_{set_Rx} = 100 μA	0.047 ± 8.2 μA	-5.4 μA	expected stat. range	-
$X \rightarrow Z_2$ for I_{set_Rx} = 100 μA	0.047 ± 8.2 μA	-0.05 μA	expected stat. range	-
$X \rightarrow Z_3$ for I_{set_Rx} = 100 μA	−0.043 ± 12.0 μA	0.65 μA	expected stat. range	-
$X \rightarrow Z_4$ for I_{set_Rx} = 100 μA	−0.043 ± 12.0 μA	-0.64 μA	expected stat. range	-
$Y \rightarrow X$ for I_{set_Rx} = 100 μA	0.336 ± 3.771 mV	2.5 mV	expected stat. range	-
Total harmonic distortion				
THD $x \rightarrow z_{1,2}$ for I_{set_Rx} = 50, 350 μA (for input current 100 $\mu A_{pk\text{-}pk}$, 1 kHz)		0.04, 0.07%	-	<1%
THD $x \rightarrow z_{3,4}$ for I_{set_Rx} = 50, 350 μA (for input current 100 $\mu A_{pk\text{-}pk}$, 1 kHz)		0.003, 0.11%	-	<1%
THD $y \rightarrow x$ for I_{set_Rx} = 50 and 200 μA (for input voltage 500 m$V_{pk\text{-}pk}$, 1 kHz)		0.08, 0.07%	-	<1%
Terminal impedances				
R_X, C_X for I_{set_Rx} = 5 → 350 μA	2320 → 240 Ω, 10 pF	6670 → 280 Ω, 20 pF	+188% → +17%	2500 → 250 Ω
R_Y, C_Y for all I_{set_Rx}	≥1 GΩ 2.7 pF	100 MΩ,14.5 pF	-	>50 kΩ
$R_{z1,2}$, $C_{z1,2}$ for I_{set_Rx} = 5 μA	52 MΩ, 4.8 pF	100 MΩ, 15.9 pF	-	>50 kΩ
$R_{z1,2}$, $C_{z1,2}$ for I_{set_Rx} = 350 μA	44 kΩ, 4.8 pF	66 kΩ 15.9 pF	-	>50 kΩ
$R_{z3,4}$, $C_{z3,4}$ for I_{set_Rx} = 5 μA	106 MΩ, 2.5 pF	100 MΩ 15.9 pF	-	>50 kΩ
$R_{z3,4}$, $C_{z3,4}$ for I_{set_Rx} = 350 μA	49 kΩ 2.5 pF	82 kΩ 15.9 pF	-	>50 kΩ
measured quiescent power consumption: 16.8 mW				

Basic principle: The topology of the CCCII was based on a differential pair ($M_{1\text{-}2}$) with full negative feedback that allowed for a simple control of terminal resistance X as an inversely

proportional function of g_m by bias current. Then, the current difference of the differential pair was taken out by cascoded current mirrors. The ideal scheme of this idea is shown in Reference [50], but our solution had some significant modifications. One of them consists in the full mirroring of currents from the differential pair. Then, symmetrical dynamics of the current and voltage responses (no DC drop on bias sources) was available. The next modification included cascoded and multiple current outputs.

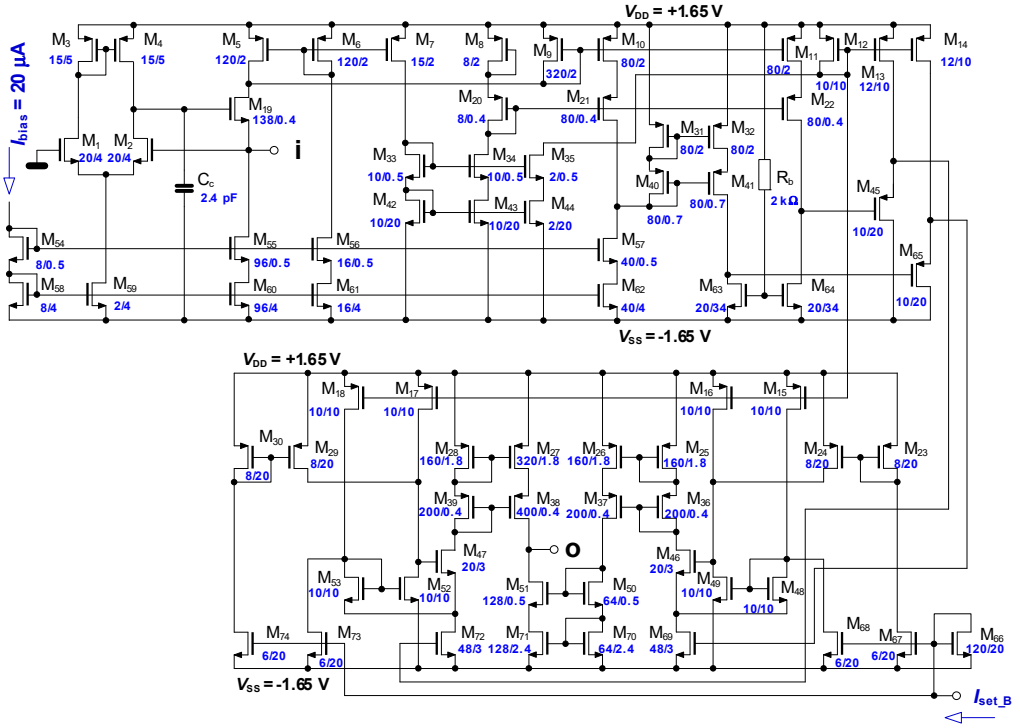

Figure A5. Full CMOS topology of the adjustable current amplifier (CA).

Table A5. Summary of simulated and measured performances of the CA cell.

Parameters/Conditions	Simulation Results (Nominal Run)	Measured Results	Error (Measured vs Simulated)	Design Target
Small-signal AC transfer				
$K_{(i\rightarrow o)}$ [-] for I_{set_B} = 1→22.5 µA	0.08 → 6.35	0.07 → 2.14	–12% → –8%	0.1 → 1.0
$K_{(i\rightarrow o)}$ [dB] (−3 dB) for I_{set_B} = 1 µA	–22.3 → 16 dB (0.69 → 2.89 MHz)	–23.4 → 6.6 dB (0.46 → 1.56 MHz)	–12% → –66%	
B [-] for I_{set_B} = 1 → 22.5 µA	0.076 → 6.346	0.067 → 2.138	+5% → –59%	
GBW $_{i\rightarrow o}$ for I_{set_B} = 1 → 22.5 µA	0.69 → 2.89 MHz	0.46 → 1.56 MHz	–33% → –46%	≥100 kHz
Input dynamic range				
I → o for I_{set_B} = 1 → 22.5 µA	≥±200 µA	≥±180 µA	–10%	≥±150 µA
Input DC offset (systematic)				
I → o for I_{set_B} = 1 → 22.5 µA	0.04 → 0.06 µA	6 → –9 µA	expected stat. range	-
Total harmonic distortion (for input current 100 ⊚$A_{pk\text{-}pk}$, 1 kHz)				
THD $_I$ → o for I_{set_B} = 12.5 µA		0.14%	-	<1%
Terminal (input/output) impedances				
R_i, L_i for all I_{set_B}	0.91 Ω 31 µH	1.4 Ω 42 µH	-	<10 Ω
R_o, C_o for I_{set_B} = 1 → 22.5 µA	80 MΩ → 59 kΩ, 3.9 pF	30 MΩ → 3 MΩ 14.1 pF	-	>1 MΩ
measured quiescent power consumption: 1.7 mW				

Basic principle: A part of this cell used a very similar but not identical to principle of CCCII. The input stage (see top part of Figure A5) consisted of an OTA section with a full negative feedback. After processing and DC-shifting the signal in both polarities, the current gain-controlling part was connected (see bottom part of Figure A5). Both branches were tied together in the output stage, including current mirrors.

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