electronics

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Four-Step Current Commutation Strategy for a Matrix Converter Based on Enhanced-PWM MCU Peripherals

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Received: 9 April 2019; Accepted: 9 May 2019; Published: 15 May 2019

Abstract: In this paper, an efficient implementation of the four-step current commutation technique for controlling bidirectional power switches in a Matrix Converter (MC) is proposed. This strategy is based on the enhanced pulse width modulation peripheral included in the *C*2000 Delfino 32-bit microcontroller of Texas Instruments. By tuning the algorithmic parameters contained in this module, the four-step commutation process is carried out on the Microcontroller Unit (MCU) without overloading the full complex processor and avoiding the use of additional special hardware such as Field-Programmable Gate Arrays (FPGA) or Complex Programmable Logic Devices (CPLD) when controlling the MC. The algorithm is implemented on the TMS320F28379D MCU and operationally validated on an MC prototype, where the functionality of the proposal is demonstrated.

Keywords: four-step commutation control; matrix converter; bidirectional power switches

1. Introduction

The direct matrix converter is a power electronics topology that efficiently carries out the AC-AC energy conversion without intermediate stages. This converter utilizes solid-state power devices and a minimum of energy storage elements, only for filtering purposes; besides, it incorporates beneficial characteristics, viz., bidirectional power flow, compact structure, high-quality low-frequency signals, and a unitary power factor operation, among others [1–3]. Direct MC is composed of an array of nine Bi-Directional power Switches (BDS), which are its main power components, as can be seen in Figure 1.

The BDS is an idealized element with the ability to block voltage and conduct current in both directions. A near-ideal behavior can be achieved by the junction of silicon devices like diodes and power transistors. Figure 2 shows the common topologies used to implement a BDS through Insulated Gate Bipolar Transistors (IGBT).

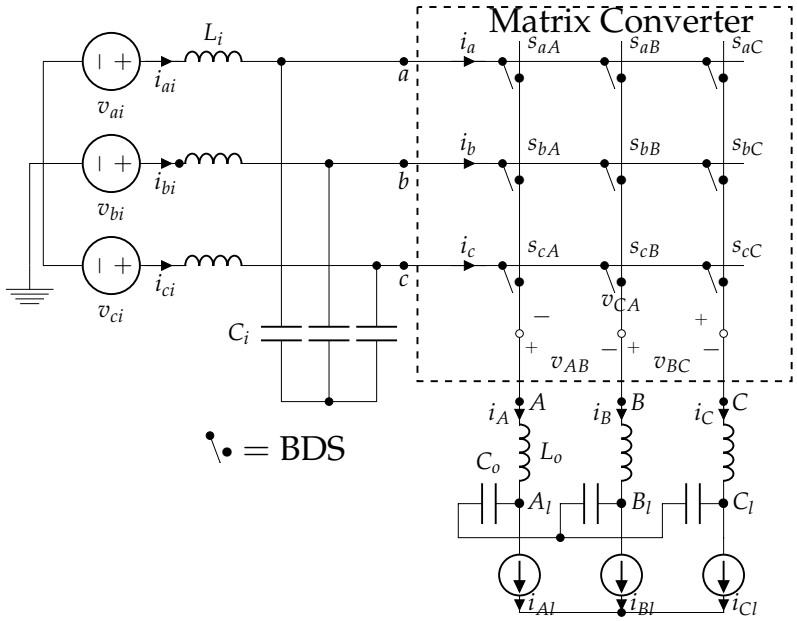

Figure 1. Matrix converter circuit and peripherals. BDS, Bi-Directional power Switches.

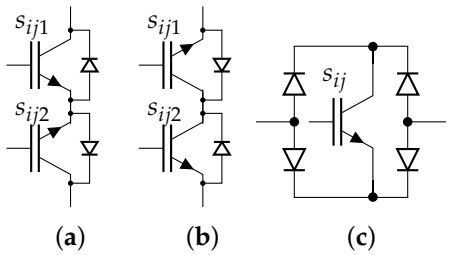

Figure 2. BDS topologies: (**a**) common-emitter, (**b**) common-collector, and (**c**) diode bridge.

In the BDS configurations presented in Figure 2a,b, two power transistors and two diodes were utilized. Operationally, the direction of the current through the BDS can be controlled, and in an instant of time, this current flows across two devices (one diode and one transistor). On the other hand, in the configuration shown in Figure 2c, one power transistor and four diodes are included in the circuit. In this case, the current flows through three components (a transistor and two diodes), and the direction of the current cannot be controlled [4]. As a result of the above, this last topology exhibits higher losses than the other two. In relation to the BDS conformed by two IGBTs, the common-emitter configuration is preferred instead of the common-collector because of implementation issues, as established in [1]. Another BDS configurations based on new power transistor technologies like Gallium Nitride (GaN), Silicon carbide Metal-Oxide-Semiconductor Field-Effect Transistors (Sic-MOSFETs), Silicon carbide Junction Field-Effect Transistors (Sic-JFETs), etc., have been recently proposed, but it is still necessary to utilize a two-transistor configuration [5–8]. The BDS control in the MC represents a fundamental task due to the lack of a natural freewheeling path for the electrical current; therefore, the commutation must be actively controlled all the time to overcome undesirable and destructive conditions, as those that will be described below. If two BDS of the same column are closed at the same time, as shown in Figure 3a, a line-to-line short-circuit appears, resulting in undesirable over-currents. Likewise, if no switch on the same column is closed, as is shown in Figure 3b, there is no path to inductive load currents, causing the appearance of over-voltages.

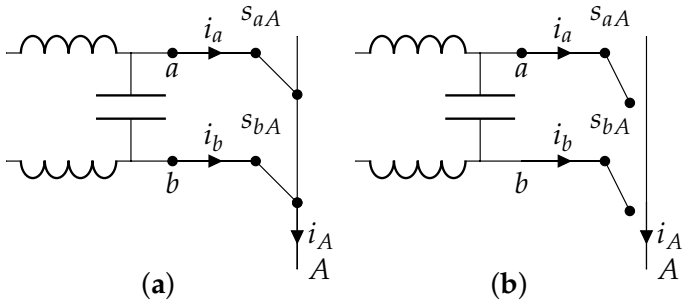

Figure 3. BDS issues in the Matrix Converter (MC): (**a**) short-circuit and (**b**) open-circuit.

In order to overcome these drawbacks, several commutation strategies based on the application of sequential steps using current measurements [9–11], voltage measurements [12–16], or measurements of both signals [17–19] have been proposed. One of the most relevant strategies is the four-step current commutation [9,20], which performs the switching from one BDS to another depending on the instant value of the current, as shown in Figure 4.

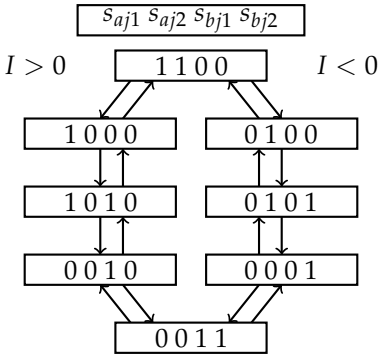

Figure 4. Four-step current commutation sequence.

This commutation strategy is independently applied in each column of the MC, so it requires the implementation of algorithms that run in parallel within a fast processing device. Generally, this issue is solved using a Complex Programmable Logic Devices (CPLD), FPGA, or multiple microprocessors, added to the main processing device, which is in charge of performing the estimation of the switching times. Likewise, this last task is efficiently executed by a Digital Signal Processor (DSP) [21–23]. Another proposal is to implement the complete algorithms in an FPGA [24,25].

In this sense, this paper presents the implementation of a fast and reliable four-step current commutation strategy, where the overall scheme utilizes the enhanced Pulse Width Modulation (ePWM) peripheral included in the C2000 Delfino MCU family of Texas Instruments. By utilizing the proposed implementation, the commutation strategy allows running all its processes in parallel without overloading the microprocessor; therefore, the use of additional dedicated hardware as FPGA or CPLD can be avoided, and the MCU carries out exclusively the full control of the MC.

The rest of the document is organized as follows: Section 2 describes the fundamentals of the MC. Section 3 explains the usage and configuration of the ePWM modules to run the four-step commutation technique. In Section 4, the results obtained through the experimental implementation are presented. This section includes the switching signals generated for the BDS with the implemented four-step current commutation strategy, in addition to the signals generated by the MC when using the SVD modulation technique, which serve to validate the effectiveness of the proposal. Section 5 presents a brief discussion

in which the results obtained in this proposal are compared with the results presented in other recent investigations. Finally, in Section 6, the general conclusions of the work are established.

2. Matrix Converter

The MC operates from the proper manipulation of the commutation logic of nine BDS (s_{ij}), which make up the 3×3 matrix (**S**). In the MC, each BDS links any of the three input voltages $(v_a, v_b, v_c)^\intercal$ to each one of the three output voltages $(V_A, V_B, V_C)^\intercal$ (see Figure 1). At any time, in each column of the MC, only one switch must be closed to ensure a safe operation. This is represented by Equation (1).

$$\begin{aligned} V_{ABC} &= \mathbf{S} V_{abc}, \\ I_{abc} &= \mathbf{S}^\intercal I_{ABC}, \\ \mathbf{S} &= \begin{pmatrix} s_{aA} & s_{aB} & s_{aC} \\ s_{bA} & s_{bB} & s_{bC} \\ s_{cA} & s_{cB} & s_{cC} \end{pmatrix}^\intercal \end{aligned} \tag{1}$$

where $0 \leq s_{ij} \leq 1$ and $s_{aj} + s_{bj} + s_{cj} = 1$, for $i \in \{a, b, c\}$ and $j \in \{A, B, C\}$. Additionally, the vectors included in Equation (1) are the following: input currents, $I_{abc}=\begin{pmatrix} i_a & i_b & i_c \end{pmatrix}^\intercal$, output currents, $I_{ABC}=\begin{pmatrix} i_A & i_B & i_C \end{pmatrix}^\intercal$, input voltages, $V_{abc}=\begin{pmatrix} v_a & v_b & v_c \end{pmatrix}^\intercal$, and output voltages, $V_{ABC}=\begin{pmatrix} v_A & v_B & v_C \end{pmatrix}^\intercal$. Through an adequate modulation strategy, a desired output voltage is generated, where the MC reaches a maximum voltage ratio of $v_{out}/v_{in}=\frac{\sqrt{3}}{2}$, for a floating output voltage [26,27]. Among the modulation techniques, duty-cycle modulations present many interesting features. In these schemes, matrix **S** of Equation (1) is represented by the averaged values of the s_{ij} elements, taken over a constant switching period. In this sense, Equation (1) can be rewritten as in Equation (2), on which are applied the same considerations indicated above for elements s_{ij}. The objective of the modulation technique is to determine the matrix **M** by solving the problem described by Equation (2); considering that the input voltages, V_{abc}, and output currents, I_{ABC}, are known, and that the output voltages, V_{ABC}, and input currents, I_{abc}, are the established reference signals.

$$\begin{aligned} V_{ABC} &= \mathbf{M} V_{abc}, \\ I_{abc} &= \mathbf{M}^T I_{ABC}, \\ \mathbf{M} &= \begin{pmatrix} m_{aA} & m_{aB} & m_{aC} \\ m_{bA} & m_{bB} & m_{bC} \\ m_{cA} & m_{cB} & m_{cC} \end{pmatrix}^\intercal \end{aligned} \tag{2}$$

where the inner matrix parameters fulfill the following two properties: $0 \leq m_{ij} \leq 1$ and $m_{iA} + m_{iB} + m_{iC} = 1$ for $i \in \{a, b, c\}$ and $j \in \{A, B, C\}$. In this paper, the Singular Value Decomposition (SVD) modulation proposed by Hojabri et al., [28] is utilized. Hence, the elements of matrix **M** are estimated considering the vector decomposition of three-phase voltage and current signal sets. Once the matrix **M** has been calculated, the obtained duty-cycles are applied to the converter.

Figure 5 presents a single-side switching pattern, where it can be observed that over a certain commutation period T_{sw}, each BDS s_{ij} is active ("on") during a predefined time given by $m_{ij} * T_{sw}$. Each transition between a pair of BDS is carried out through the four-step current commutation process, as depicted in Figures 6 and 7. The signals involved in the commutation process between each pair of BDS of the MC first column are presented in these figures. Considering the first case presented in Figure 6, where s_{aA} is the off-going and s_{bA} is the on-coming BDS, the four-step commutation process can

be explained as follows: (i) in the first step, the non-conducting switch of the off-going BDS is turned off; (ii) then, the on-coming conducting switch is turned on (second step); (iii) in the third step, the off-going conducting switch is turned off; and (iv) in the final step, the on-coming non-conducting switch is turned on. As stated before, the commutation logic depends on the electrical current direction, as can be seen in Figures 6 and 7 previously discussed.

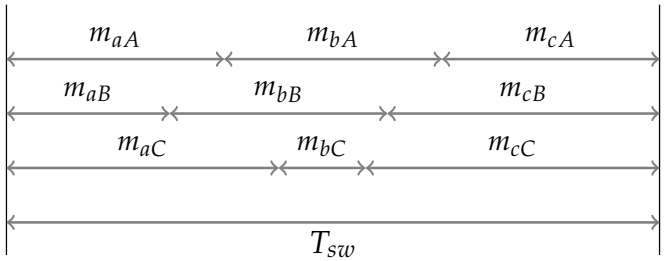

Figure 5. Single-side switching pattern for the duty-cycle modulation.

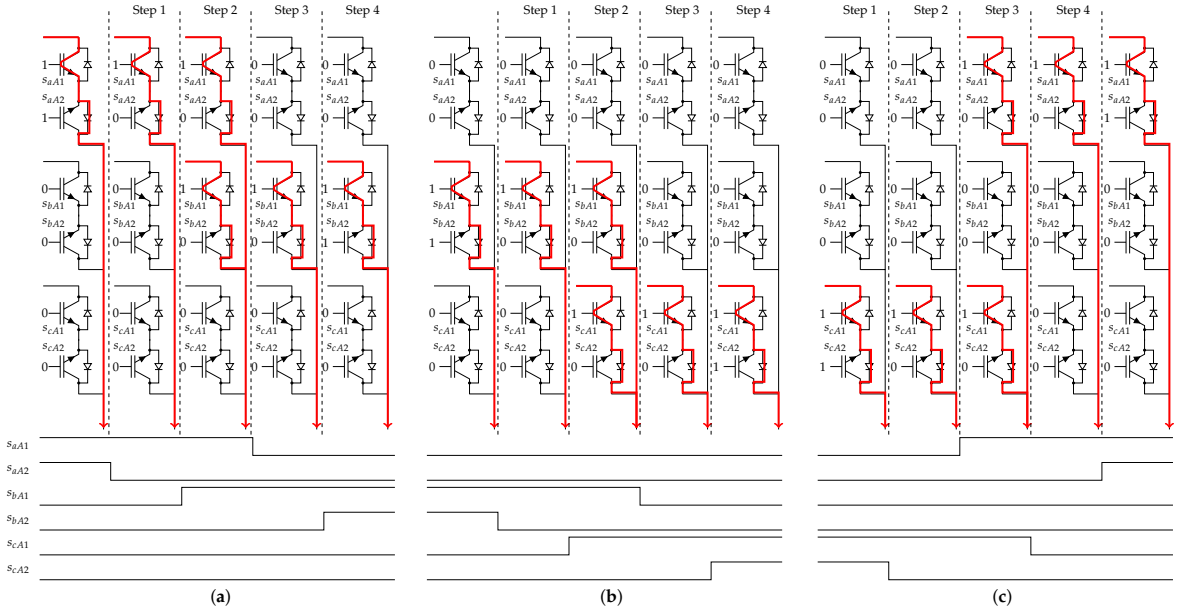

Figure 6. Four-step commutation logical signals, outgoing current case, for the transitions (**a**) s_{aA} to s_{bA}, (**b**) s_{bA} to s_{cA}, and (**c**) s_{cA} to s_{aA}.

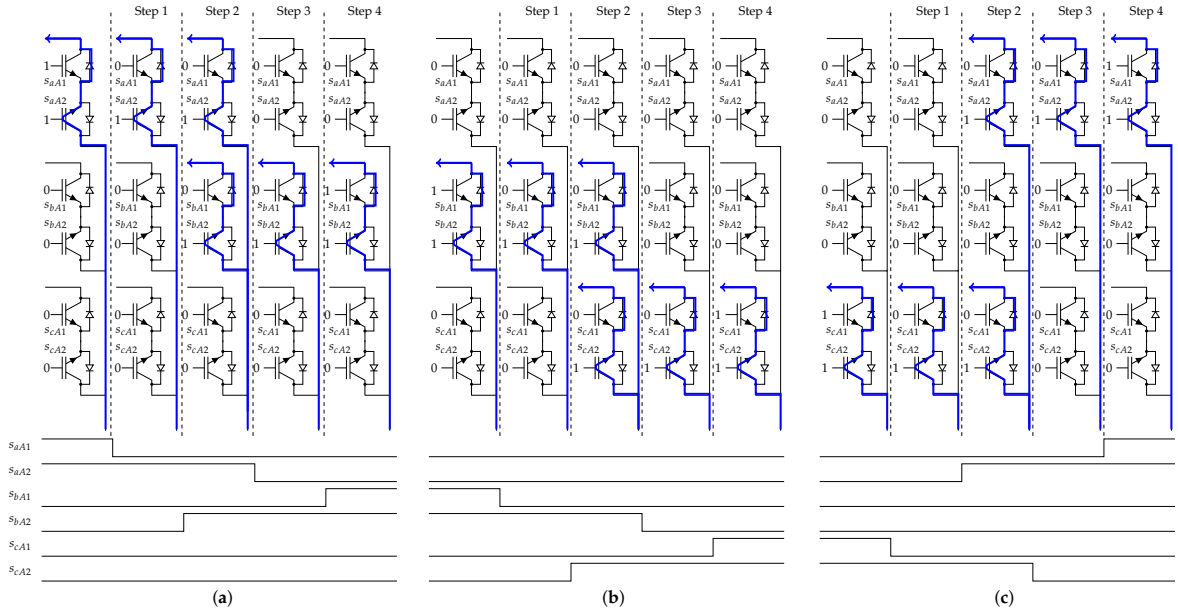

Figure 7. Four-step commutation logical signals, incoming current case, for the transitions (**a**) s_{aA} to s_{bA}, (**b**) s_{bA} to s_{cA}, and (**c**) s_{cA} to s_{aA}.

3. ePWM Module

The ePWM module of the C2000 TI family incorporates the functions needed to implement PWM algorithms with improved functionalities [29]. The configuration of the peripherals is achieved by modifying the corresponding registers, which requires minimal processing. It is worth mentioning that the duty-cycles are updated during each commutation period. In this paper, the ePWM Type 4 of the device TMS320F2837xD is used for implementing the four-step current commutation technique. The configuration required to generate the gate signals for the BDS in an MC column is described below. For the other two columns, only the same structure in the remaining ePWM modules of the MCU needs to be replicated.

3.1. ePWM Configuration

Each ePWM module is utilized to control one BDS, s_{ij}; thus, three ePWM modules are required for operating a single column in the MC. In this sense, a total of nine modules is required to control the complete MC. For the first column, three ePWM modules were used, identified as 1, 2, and 3. The clock in these modules was configured to execute the count-up from zero until reaching the value established in the PRD register, generating a saw-tooth signal. Comparing these signals with the values set in the registers CMPA, CMPB, PRD, or the ZERO value, the desired output signals can be obtained once the counters have reached one of these values. Output signals can be set at a high-level (set) or low-level (clear). Each ePWM module provides two output signals, ePWMxa and ePWMxb, which are directly assigned to each transistor of the BDS. These last signals can be configured to maintain the time delay required in the four-step algorithm, through the dead-band submodule shown in Figure 8. In this device, the dead-band time is configured by the registers FED and RED, and once the ePWM has been properly configured, the respective outputs ePWMxa and ePWMxb can be exchanged through the register DBCTL[OUTSWAP] (DBO) [30]. The latter is an essential feature for the implementation of the four-step algorithm. Additionally, the ePWM module has two registers, CMPC and CMPD, which can be used as sources of flags and interruptions.

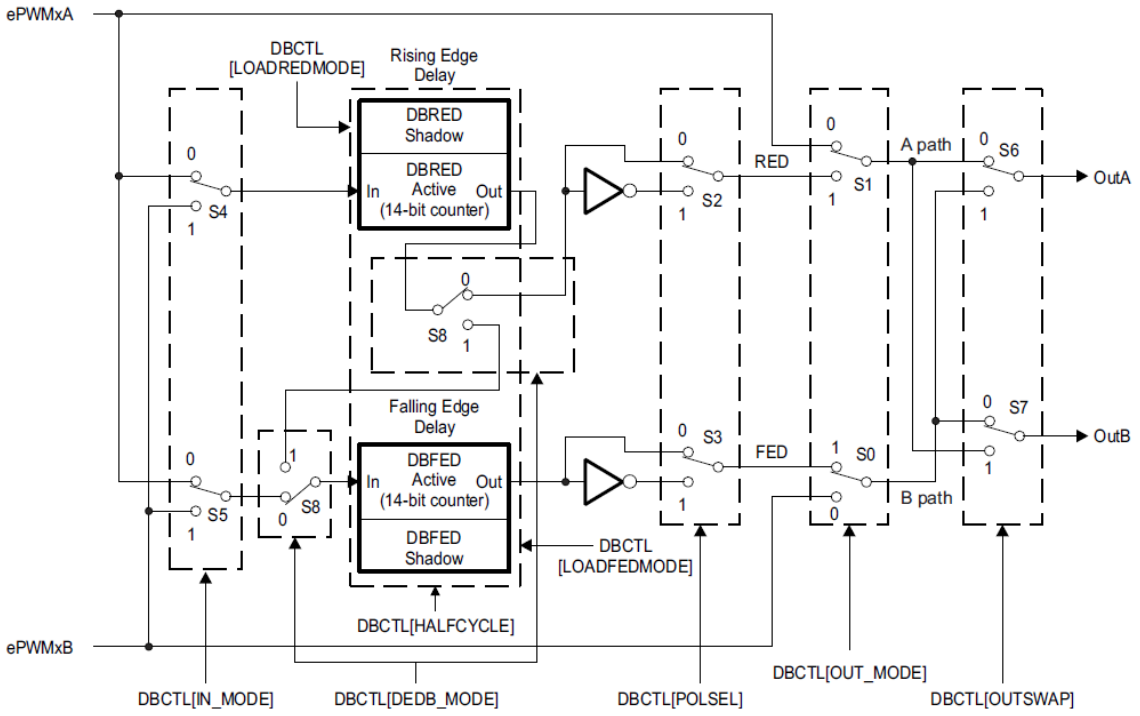

Figure 8. Enhanced Pulse Width Modulation (ePWM) dead band submodule [30].

3.1.1. BDS s_{aj}

The ePWM1 is assigned to the control of the BDS s_{aj}; hence, this peripheral is configured to activate its outputs an instant after the counter is superior to zero and until the value of (m_{aj})*PRD is reached. This is achieved by defining the set and clear signals when the counter reaches the values FED/2 (CAU_1) and (m_{aj})*PRD (CBU_1), which were loaded in registers CMPA and CMPB, respectively.

3.1.2. BDS s_{bj}

ePWM2 generates the commutation signals for the BDS s_{bj}; for this, it must be active as long as the value of the counter is higher than (m_{aj})*PRD + FED/2 and lower than (m_{aj} + m_{bj})*PRD. This is achieved by placing these last two values in the registers CMPA (CAU_2) and CMPB (CBU_2), besides configuring them as *set* and *clear* signals, respectively.

3.1.3. BDS s_{cj}

Finally, ePWM3 is configured to control the BDS s_{cj}; in this case, the module is activated while the value of the counter is higher than (m_{aj} + m_{bj})*PRD + FED/2, and it remains in that state until the PRD value is reached. The above is achieved by configuring the CMPA register with the value (m_{aj} + m_{bj})*PRD + FED/2 (CAU_3), and similarly to the *set* signal, the *clear* signal is reached when the counter is equal to the value in the register PRD (PRD_3). The process of generating the switching signals for the ePWM1, ePWM2, and ePWM3 modules, under the four-step commutation strategy, is graphically represented in Figure 9.

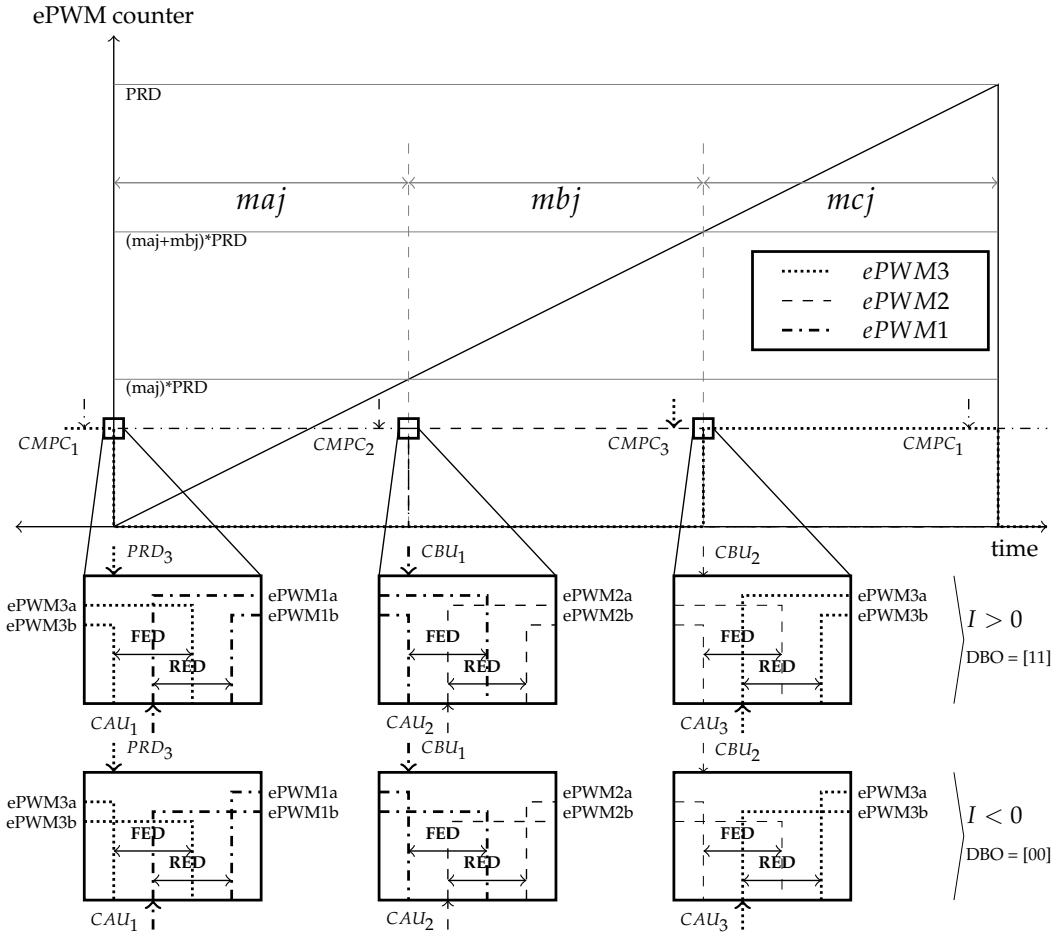

Figure 9. Four-step ePWM configuration and logical signals. DBO, DBCTL[OUTSWAP].

3.2. Current Sign Detection

The direction of the current is determined using an external circuit, which provides a digital signal indicating the current sign. This signal is read an instant before starting the commutation to assign the appropriate value in the DBO register. This procedure is carried out within a software interruption that is triggered when the counter reaches the value loaded in the CMPC register, once the commutation times have been estimated. For a particular value assigned to the DSG variable, which corresponds to the time between the reading of the current sign and the beginning of the commutation, the ePWM1 CMPC register is loaded with a value equal to PRD-DSG ($CMPC_1$), the ePWM2 CMPC register with a value equal to (m_{aj})*PRD-DSG ($CMPC_2$), and the ePWM3 CMPC register with a value equal to (m_{aj} + m_{bj})*PRD-DSG ($CMPC_3$).

4. Experimental Results

In order to verify the effectiveness of the proposed algorithm, a prototype of the three-phase direct matrix converter (Figure 1), was implemented. The MC experimental setup was built using the HGT1S1260A4DS IGBTs, and for the input and output filter, the following elements were utilized, $L_i = 1$ (mH), $C_i = 5$ (μF), $L_o = 2.2$ (mH), and $C_o = 4$ (μF). Finally, a resistor of 170 (Ω) was connected to each of the MC output terminals as electrical load. The corresponding gates of the IGBTs were triggered by a pulse of ±15 (V) through the HCPL-3120 gate-driver. Figure 10 illustrates the complete experimental test

system. The four-step commutation strategy along with the SVD modulation technique were implemented in the TMS320F28379D device. The 32-bit floating-point CPU of the MCU has a Trigonometric Math Unit (TMU) accelerator, which allows evaluating the matrix **M** of Equation (2) in a time inferior to 5 [µs].

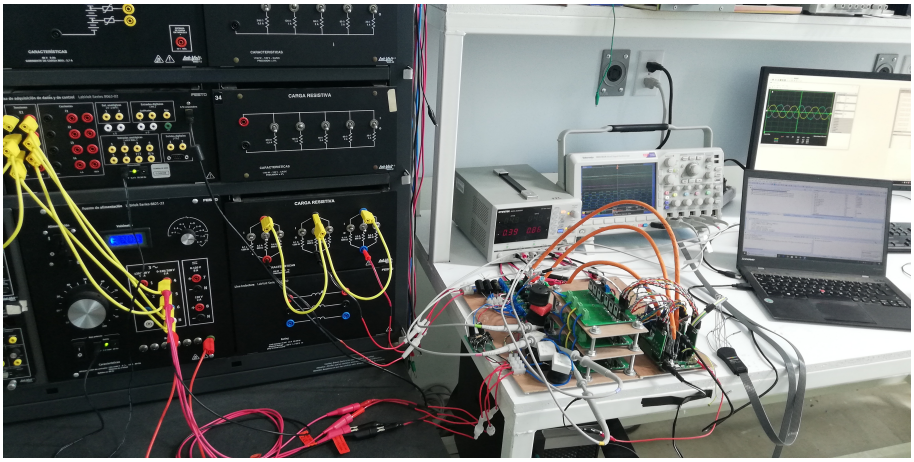

Figure 10. System implementation for testing purposes.

Figure 11a–c presents the signals involved in the commutation of the MC third column, namely, the input voltages (v_a, v_b, v_c), the output voltage v_C, and the gate signals obtained from the implemented four-step commutation strategy. In this case, input voltages v_a, v_b, and v_c were sequentially applied to output voltage v_C, during periods of time established by $m_{aC} * T_{sw}$, $m_{bC} * T_{sw}$, and $m_{cC} * T_{sw}$, respectively. Figure 11a illustrates the case when a transition between BDS s_{aC} and s_{bC} occurs, which means that the output voltage at MC phase C (v_C) passes from being equal to the input voltage (v_a) to be synthesized by the phase b input voltage (v_b). This figure also illustrates the control signals generated for the six switches that make up the three BDS of the MC third column, allowing one to appreciate the four steps required to achieve the commutation.

Likewise, Figure 11b,c presents the transition between BDS s_{bC} and s_{cC} and the transition between BDS s_{cC} and s_{cA}. The first transition implies disconnecting the MC output terminal of phase C from the input terminal of phase b and connecting it to the input terminal of phase c. The last transition presented in Figure 11c corresponds to the case when the connection of the MC output terminal of phase C is changed from input terminal of phase c to the input terminal of phase a. In each figure, the three signals of the input voltages (v_a, v_b, and v_c) and the phase C output voltage (v_C) are shown, and from these signals, the MC operation principle is verified, which can be summarized by synthesizing the output voltages from the input voltages. On the other hand, in each case, the control signals (s_{aC1}, s_{aC2}, s_{bC1}, s_{bC2}, s_{cC1}, and s_{cC2}) serve to verify the correct operation of the implemented four-step commutation strategy.

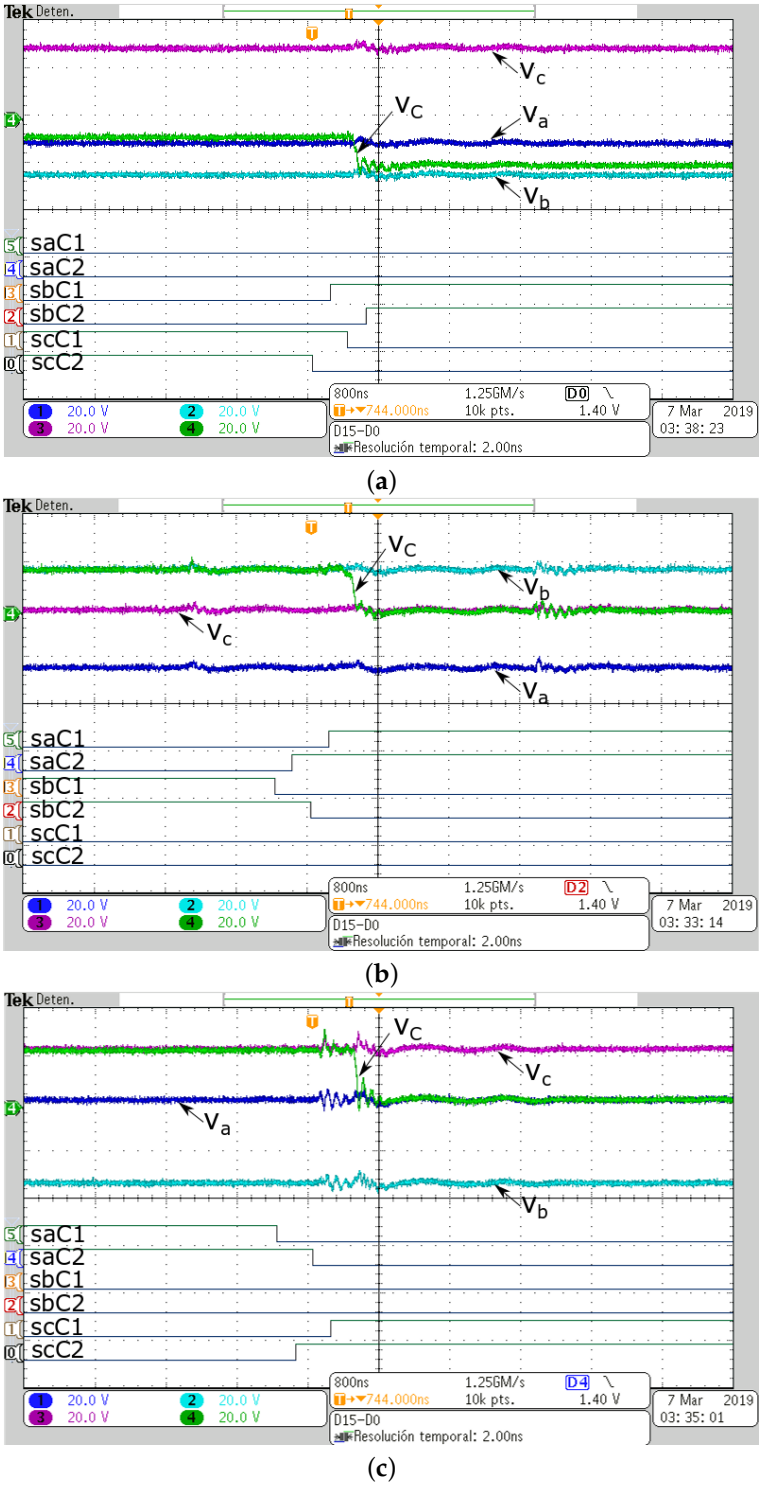

Figure 11. Output voltage transitions (**a**) v_{aC} to v_{bC}, (**b**) v_{bC} to v_{cC}, and (**c**) v_{bC} to v_{cC}.

Finally, the developed MC architecture was tested to validate the proper operation of the MC when both the four-step commutation strategy and the SVD modulation technique were implemented in the same processing board. Figure 12 exhibits the 60-Hz phase *a* input voltage (v_{ai}) and the 50-Hz filtered line-to-line output voltage (v_{ABl}) signals, demonstrating that the prototype is able to generate the characteristic MC

output voltage signals (v_{Al} and v_{Bl}) effectively with no significant low order harmonics, as can be seen from voltage signal (v_{ABl}).

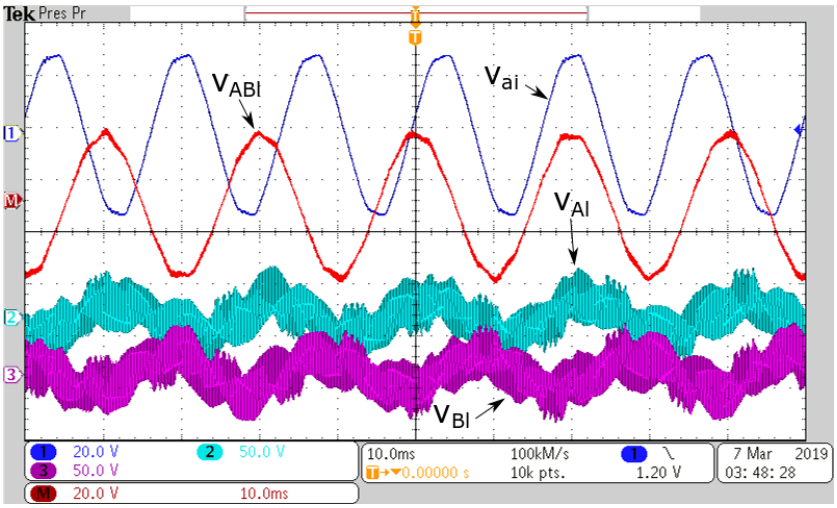

Figure 12. MC input-output voltages.

5. Discussion

In order to control the operation of the MC in a safe way, the modulation strategy that establishes the switching sequence and the commutation technique must be properly implemented by means of programming control routines that can be executed in parallel on processing boards. For this purpose, the common practice is to use either the combination of several processing devices or one single complex device. This common practice, however, increases the complexity and cost of the implemented applications. Accordingly, the proposal in this work aims to reduce that complexity and cost related to the implementation of the switching sequence and the commutation technique, which is highlighted based on the following discussion where the proposed implementation is compared with those that follow the common practice.

For instance, in [21,22,31,32], the control algorithms were implemented in a DSP in conjunction with an FPGA, where the DSP-board is responsible for performing the calculations required for the modulation strategy and generating the switching signals through its PWM peripherals, while the FPGA executes the commutation strategy required to activate the transistors. These papers show how both processing devices interact with each other in order to perform all the control tasks required. The experimental implementation presented in [23,33] utilized the dSPACE DS1104 control board to generate the PWM signals, and then, these signals were supplied to a CPLD, which executed the four-step commutation technique. Likewise, in proposals such as those presented in [24,34,35], an FPGA platform performed all the routines that control the experimental MC.

From the MC experimental implementations reviewed, it is clear that the implementation of any modulation strategy, scalar or vector, in addition to the commutation technique represent a complex programming task and a considerable processing load. In this sense, a simple solution consists of dividing the total of the functions necessary to control the MC into two processing devices, at the expense of raising the cost of full implementation. On the other hand, all proposals that include complex devices like FPGAs or CPLDs have the disadvantage of increasing the difficulty of programming since they require the use of Hardware Description Language (HDL) instead of sequential programming in C language, as in the current proposal. Furthermore, the aforementioned complex devices require additional hardware to operate properly in this specific application. The implementation proposed in this paper

incorporates a low-cost, compact MCU board as a single processing device, which by programming hierarchical interruptions, allows it to perform the four-step commutation strategy without interfering with the execution of the modulation scheme. For this reason, this approach can be considered an advance in the implementation of control algorithms for the MC, since it improves the size, costs, and ease of programming, in the prototyping stage of MC.

6. Conclusions

This paper proposed a strategy to implement the four-step current commutation technique using the ePWM peripheral of the TMS320F28379D MCU of TI. By straightforwardly programming hierarchical interruptions, through the setup of the MCU registers, a four-step commutation strategy without interfering with the execution of the modulation scheme has been performed. In this way, the MCU is fully capable of processing both algorithms in parallel, the commutation strategy, and the SVD modulation scheme, avoiding the use of additional specialized hardware such as FPGA or CPLD. The original proposal was validated through an experimental MC prototype, where the obtained output voltages corroborated that the modulation, and commutation strategies were efficiently implemented in the MCU. Based on this strategy, the double-side switching pattern can be also implemented, with the respective additions and modifications. This feature might be useful to improve the quality of the signals generated by the MC, and this important aspect is under research with results that will be published in a forthcoming publication. The TI C2000 devices are widely used in the power electronics field, and in the context of this work, a single TMS320F28379D MCU-board has allowed an improvement of the MC prototyping, where a reduction of costs and implementation complexity have been achieved, aspects that contribute to the maturation of this type of technology.

Author Contributions: Conceptualization, methodology, data curation, visualization, and supervision, L.R.M.-V., J.M.L.-G., and A.P.-M.; software and validation, D.A.d.J.G.-T., L.R.M.-V., and A.P.-M.; writing, original draft preparation, L.R.M.-V.; formal analysis, investigation, and writing, review and editing, L.R.M.-V., J.M.L.-G., J.G.A.-C., and A.P.-M.; resources and project administration, J.M.L.-G.; funding acquisition, J.M.L.-G. and J.G.A.-C.

Funding: This project was fully supported by the Mexican Council of Science and Technology CONACyT, Grant Number 587661/433405.

Acknowledgments: The authors would like to thank the Department of Electronic Engineering and Department of Electrical Engineering of the University of Guanajuato for its financial support.

Conflicts of Interest: The authors declare no conflict of interest.

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