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Design and Investigation of the Junction-Less TFET with Ge/$Si_{0.3}Ge_{0.7}$/Si Heterojunction and Heterogeneous Gate Dielectric

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Abstract: To improve the on-state current and reduce the miller capacitance of the conventional junction-less tunneling field effect transistor (JLTFET), the junction-less TFET with Ge/$Si_{0.3}Ge_{0.7}$/Si heterojunction and heterogeneous gate dielectric (H-JLTFET) is investigated by the Technology Computer Aided Design (TCAD) simulation in this paper. The source region uses the narrow bandgap semiconductor material germanium to obtain the higher on-state current; the gate dielectric adjacent to the drain region adopts the low-k dielectric material SiO_2, which is considered to reduce the gate-to-drain capacitance effectively. Moreover, the gap region uses the $Si_{0.3}Ge_{0.7}$ material to decrease the tunneling distance. In addition, the effects of the device sizes, doping concentration and work function on the performance of the H-JLTFET are analyzed systematically. The optimal on-state current and switching ratio of the H-JLTFET can reach 6 μA/μm and 2.6×10^{12}, which are one order of magnitude and four orders of magnitude larger than the conventional JLTFET, respectively. Meanwhile, the gate-to-drain capacitance, off-state current and power consumption of the H-JLTFET can be effectively suppressed, so it will have a great potential in future ultra-low power integrated circuit applications.

Keywords: JLTFET; Charge plasma; On-state current; gate-to-drain capacitance

1. Introduction

The mechanism of traditional metal oxide semiconductor field effect transistors (MOSFETs) is thermal electron emission, so the subthreshold swing (SS) is limited to 60 mV/Dec at room temperature [1–3]. The SS value of MOSFETs is severely degraded by the short channel effect. The channel is more likely to generate the leakage current when the size of the transistor decreases, which will result in a higher power consumption [4,5]. To solve the above problems, researchers have conducted extensive research on tunneling field effect transistors (TFETs) with steep SS characteristics. The physical mechanism of TFETs is band to band tunneling (BTBT), which refers to the quantum tunneling of electrons from a valence band to a conduction band [6–9]. The TFETs is compatible with the Complementary Metal Oxide Semiconductor (CMOS) technology, which is not likely to be influenced by the short channel effect. Moreover, it can break the SS limit of 60 mV/Dec, and the leakage current is small under the off-state condition [10]. Besides, TFETs can also decrease the operating

voltage. Therefore, TFETs would be one of the most promising alternatives to MOSFET in low-power integrated circuit applications [11,12].

However, there are also inherent disadvantages in TFETs, such as the small on-state current and large miller capacitance [13]. To improve the on-state current of TFET, new device structures are proposed, such as the L-channel tunneling field effect transistor (LTFET) [14,15], U-channel tunneling field effect transistor (UTFET) [16], heterojunction tunneling field effect transistor (HTFET) [17], and T-shaped gate tunneling field effect transistor (HTG-TFET) [18,19]. To achieve the tunneling effectively, it is necessary to form the highly doped abrupt junction in these novel device structures. At the same time, this requires complex fabrication processes and a high thermal budget [20]. To overcome the above issues, the junction-less tunneling field effect transistor (JLTFET) is constructed. The high doped n^+-n^+-n^+ substrate is converted into the p^+-i-n^+ structure by the polar-gate and control-gate with different work functions, which can enhance the gate-to-channel control [21,22]. The doping concentration and type of channel region are consistent with the source region and drain region. Meanwhile, the effects of the complex fabrication processes, random doping fluctuations and thermal costs can also be effectively avoided through the charge plasma concept [23].

The junction-less TFET with the Ge/$Si_{0.3}Ge_{0.7}$/Si heterojunction and heterogeneous gate dielectric (H-JLTFET) is proposed to improve the on-state current and reduce the miller capacitance. The paper framework is as follows: Section 2 describes the parameters and models of the H-JLTFET. Section 3 demonstrates the simulated results and discussion. Section 4 shows the conclusions.

2. Methods

Figure 1a shows the device structure schematic of the conventional JLTFET. The polar-gate and control-gate with different work functions are used in the conventional JLTFET with the heavily n-type-doped channel, which can improve the gate-to-channel control. Compared to the conventional JLTFET, the differences of the H-JLTFET are that the on-state current can be improved by the Ge/$Si_{0.3}Ge_{0.7}$/Si heterojunction, and the gate-to-drain capacitance can be reduced by the low-k dielectric material SiO_2 near the drain region, as shown in Figure 1b. The H-JLTFET has the higher on-state current and the lower gate-to-drain capacitance, so it has great potential in ultra-low power integrated circuit applications.

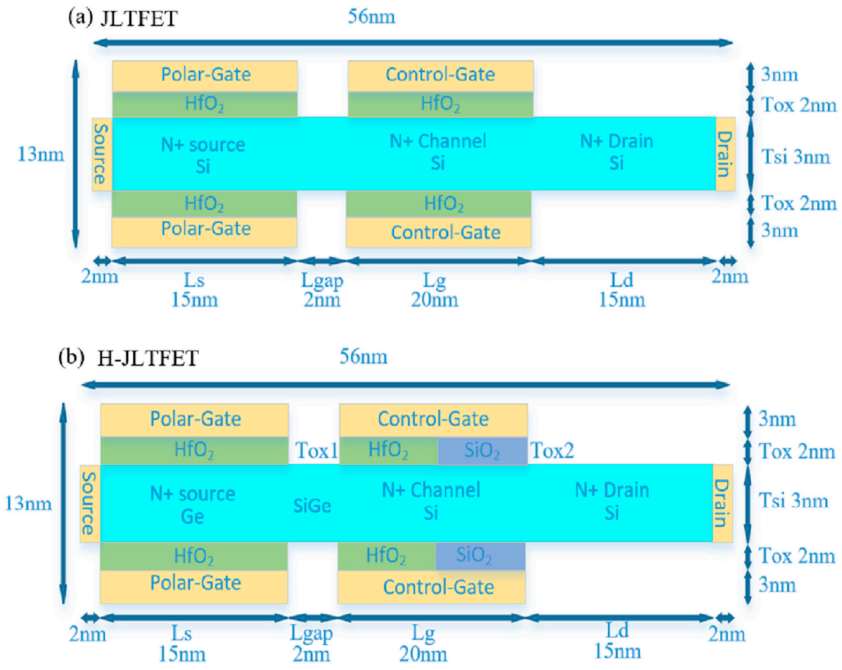

Figure 1. Device structure schematic of (**a**) JLTFET; and (**b**) H-JLTFET.

The detailed parameters of JLTFET and H-JLTFET in the simulation are as follows: the length of the source region (L_s), channel region (L_g) and drain region (L_d) are respectively 15 nm, 20 nm and 15 nm; the gap length (L_{gap}) between the polar-gate and control-gate is 5 nm; the thickness of HfO_2 T_{ox1} = 2 nm, the thickness of SiO_2 T_{ox2} = 2 nm, the thickness of the silicon body T_{si} = 3 nm; What is more, the doping concentration and doping type of the source region (N_s), pocket region (N_p), channel region (N_g), and drain region (N_d) are $1 \times 10^{19}/cm^3$ and the N type, respectively. Furthermore, the double-gate process is adopted in the simulation to improve the gate-to-channel control.

All the simulation results of H-JLTFET are based on the SILVACO ATLAS, from version 3.8.52.R (Santa Clara University, Santa Clara, CA, USA). The non-local BTBT model is used to consider the spatial variation of the energy band and the non-local generation of electrons and holes [24]. Due to the highly doped channel, we also adopt the Fermi-Dirac statistics and the band gap narrowing model to reduce the carrier concentration. Moreover, considering the effects of interface traps or defects at the Si/HfO_2 interface, the conventional JLTFET simulation should also include the Shockley-Read-Hall recombination and trap-assisted tunneling models, which can explain the cause of the electron tunneling band gap by traps or defects. The high-k dielectric material HfO_2 of the H-JLTFET is smaller than that of the JLTFET, so the interface trap effects could be ignored in the H-JLTFET simulation [25]. Furthermore, it is necessary to take the quantum confinement effect into account under the heavily doped channel and thin oxide dielectric. The tunneling process will be more accurate by using the above physical models. The simulation result will be discussed in detail.

3. Results and Discussion

3.1. The Input Characteristics

It is not difficult to find, by observing Figure 2a, that the H-JLTFET can obtain the on-state current of 6 μA/μm and switching ratio of 2.6×10^{12} when the drain voltage is 1 V, whereas the on-state current and switching ratio of JLTFET are respectively 0.15 μA/μm and 1.75×10^8. Therefore, the on-state current and switching ratio of H-JLTFET are increased by one and four orders of magnitude, respectively. The reason for this is that the $Ge/Si_{0.3}Ge_{0.7}/Si$ heterojunction is formed in the channel of H-JLTFET, the energy bands can be bent more severely, and the BTBT efficiency increases. Meanwhile, it can also decrease the tunneling distance.

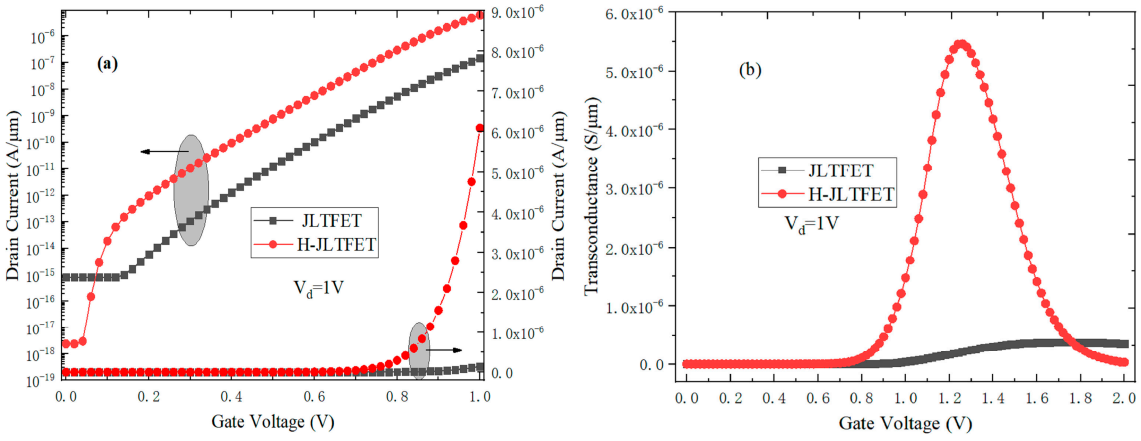

Figure 2. (**a**) Transfer characteristics; and (**b**) transconductance of JLTFET and H-JLTFET.

The transconductance is an important indicator to evaluate the analog performance. It can be obtained by the first derivative of the transfer characteristics [26]. Equation (1) is the calculation formula of the transconductance:

$$g_m = dI_{ds}/dV_{gs} \quad (1)$$

In Figure 2b, the transconductances of JLTFET and H-JLTFET markedly increase when the gate voltage increases from 0 V to 1.2 V. The maximum transconductance value of the JLTFET is 3.8×10^{-7} S/μm, whereas the maximum transconductance value in the H-JLTFET can reach up to 5.5×10^{-6} S/μm when the gate voltage is 1.2 V; consequently, the transconductance value can be increased by an order of magnitude. According to the transconductance definition, the higher the on-state current is, the higher the transconductance value is. As a result, the H-JLTFET can obtain a better analog performance.

3.2. The Output Characteristics

As shown in Figure 3a, the output current of the JLTFET and H-JLTFET increases when the drain voltage increases, and the output current of the H-JLTFET become saturated when the drain voltage reaches 0.8 V. The H-JLTFET can obtain a higher saturation drain current and lower pinch-off voltage compared with the conventional JLTFET, so it has an obvious advantage in the output characteristics. This is explained by the fact that the H-JLTFET has the stronger tunneling efficiency and the higher electron concentration.

Figure 3b shows the output conductance characteristics of the JLTFET and H-JLTFET when the gate voltage is 1 V. The output conductance can be calculated by the ratio of the drain current to the output voltage, which can be expressed by Equation (2):

$$g_{\mathrm{ds}} = dI_{ds}/dV_{ds} \tag{2}$$

Due to the higher on-state current, the H-JLTFET has the larger output conductance. When the gate voltage is 1 V, the H-JLTFET has the maximum output conductance, at 11.3 μs/μm, when the drain voltage is 0.66 V. However, the JLTFET can obtain the maximum output conductance, at 0.615 μs/μm, when the drain voltage increases to 0.8 V.

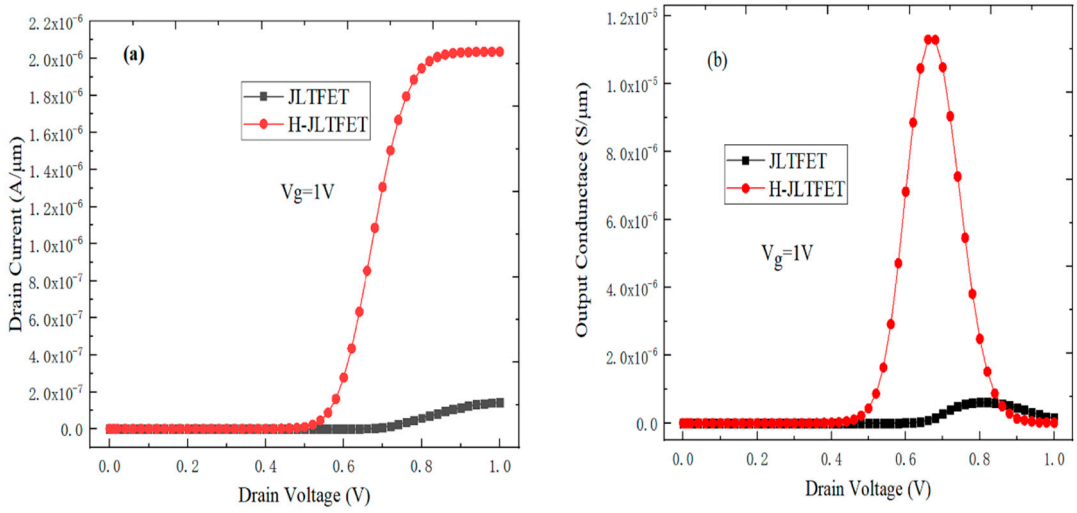

Figure 3. (**a**) Output characteristics; and (**b**) output conductance of JLTFET and H-JLTFET.

The non-local BTBT model is used to consider the spatial variation of the energy band and the non-local generation of electrons and holes. Figure 4a shows the energy band of JLTFET and H-JLTFET under the off-state condition. It can be seen clearly that energy band structure is similar to the P^+-I-N^+ transistor configuration, and the tunneling barrier width is relatively wide under the off-state condition. Therefore, the probability that electrons from the valence band would tunnel to the conduction band is negligible, which indicates that the BTBT phenomenon is unlikely to happen. The energy band of the JLTFET and H-JLTFET under the on-state condition is shown in Figure 4b. For the JLTFET and H-JLTFET, the tunneling barrier width between the source and channel is narrowed, and the tunneling

range is widened when the positive gate voltage is applied to the control-gate, so the BTBT phenomenon is more likely to occur, and the tunneling current increases exponentially. The H-JLTFET has a higher electric field and smaller tunneling distance at the source/channel tunnel junction compared with the JLTFET, which can help to obtain a higher electron concentration and on-state current, as shown in Figure 2a.

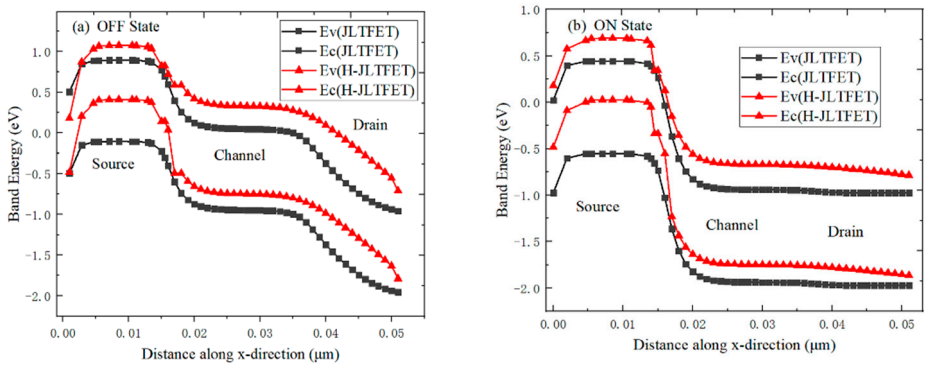

Figure 4. (**a**) Energy band diagram under the off-state; and (**b**) energy band diagram under the on-state.

3.3. Effect of Device Sizes on the Transfer Characteristics

Figure 5a shows the effect of the channel doping concentration on the transfer characteristics. When the channel doping concentration increases, the off-state current gradually increases, and the on-state current decreases to some extent, which leads to the decrease of the switching ratio. The Fermi-Dirac statistics and band gap narrowing models are used to reduce the carrier concentration of the heavily doped channel. The reason for this is that the source/channel tunnel junction under the off-state condition would be turned on slightly when the channel doping concentration is higher than 1×10^{17} cm^{-3}. At the same time, the energy band of the tunnel junction becomes steeper when the doping concentration decreases, so the effective tunneling length decreases, and the tunneling efficiency and on-state current increase. In Figure 5b, the on-state current decreases with the channel height increasing, and the off-state current increases to some extent, so the switching ratio drops. This is because the electron impedance and channel electron thermal excitation barrier increase when the channel height increases. Figure 5c shows that the transfer characteristic curve drifts to the left when the Ge component in the $Si_{1-x}Ge_x$ material increases, and the optimal Ge component is x = 0.7. The reason for this is that the band gap of $Si_{1-x}Ge_x$ decreases with the Ge component increasing. Meanwhile, the on-state current increases first and then remains, and the off-state current remains basically the same, so the switching ratio change trend is consistent with the on-state current. This is because the electric field of the tunnel junction becomes higher, the energy band become steeper, and the electrons from the source region are more likely to tunnel into the channel when the Ge composition increases. Therefore, the on-state current can be improved.

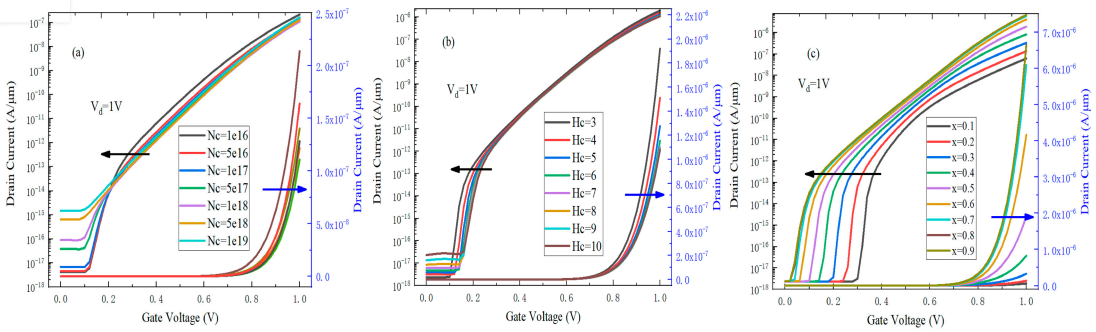

Figure 5. The effects of (**a**) the channel doping concentration; (**b**) the channel height; and (**c**) the Ge content in $Si_{1-x}Ge_x$ material on the transfer characteristics of the H-JLTFET.

It can be found through the observation of Figure 6a that the transfer characteristic curve shifts to the left when the thickness of the gate oxide dielectric layer decreases from 5 nm to 1 nm. It is necessary to consider the quantum confinement effect when the H-JLTFET is under the thin oxide dielectric. The on-state current decreases when the thickness of the gate oxide dielectric increases, and meanwhile the off-state current decreases first and then remains; consequently, the switching ratio of the H-JLTFET rises first and then falls. This is because the energy band becomes more curved when the gate oxide dielectric thickness decreases. As shown in Figure 6b, the optimal thickness of the gate oxide dielectric is 2 nm.

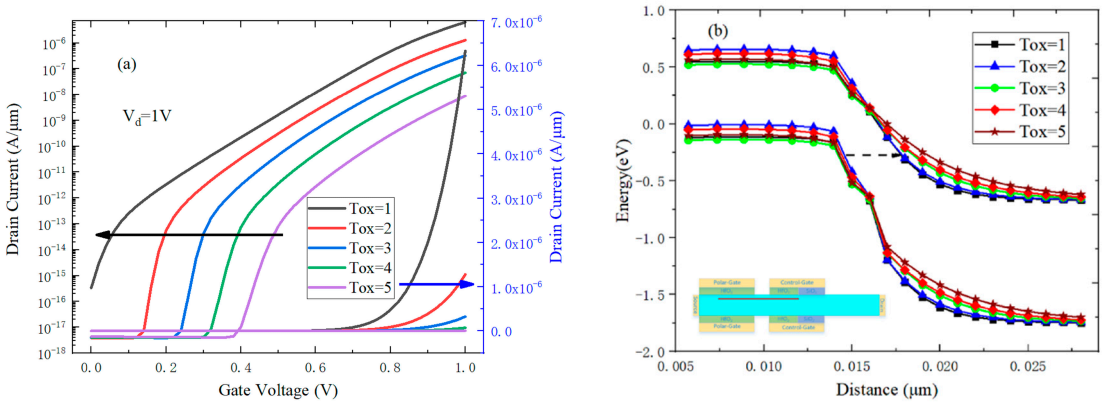

Figure 6. Effect of the gate oxide dielectric thickness on the device performance. (**a**) Transfer characteristics; and (**b**) energy band of the tunnel junction under the on state.

It can be seen from Figure 7a that the smaller the gap length is, the larger the on-state current is. At the same time, the off-state current substantially remains constant, so the switching ratio increases when the gap length decreases. In Figure 7b, the electric field of the source/channel tunnel junction becomes stronger, and electrons from the source region are more likely to tunnel into the channel when the gap length decreases, which would result in the increase of the on-state current and the switching ratio.

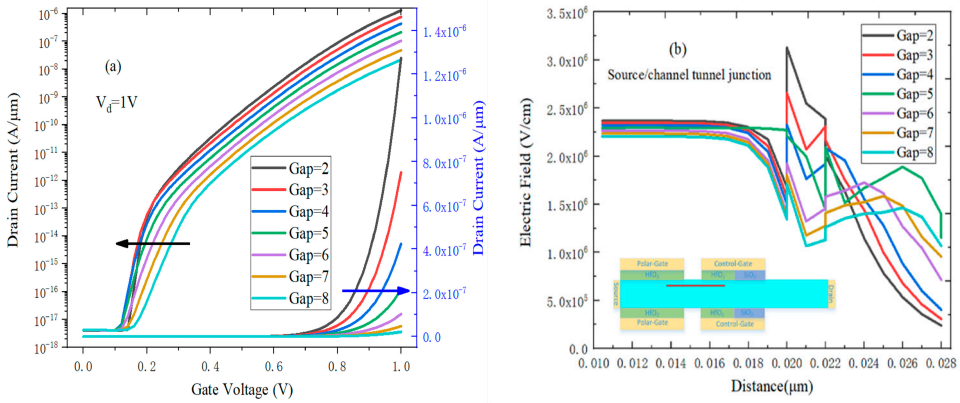

Figure 7. The effect of the gap length between the polar-gate and control-gate on the device performance. (**a**) Transfer characteristics; and (**b**) electric field of the tunnel junction under the on state.

For the JLTFETs, the gate work function has the larger impact on the modulation of the device performance. In Figure 8a, the on-state current increases slightly when the work function of the polar-gate increases. Meanwhile, the transfer characteristic curve shifts to the left and the threshold voltage decreases. The reason for this is that energy band at the source/channel tunnel junction bends steeply. Figure 8b shows the transfer characteristics under the different control-gate work functions. It can be seen that the transfer characteristic shifts to the left, and the on-state current increases with the

control-gate work function decreasing. Furthermore, the off-state current increases rapidly when the control-gate work function drops below 4.3 eV. The control-gate work function has the greater influence on the transfer characteristics, when comparing Figure 8a,b. When the control-gate work function decreases, the electric field of the tunnel junction increases, the surface potential of the control-gate near the drain side region decreases, and the energy band bends severely. As a result, the BTBT phenomenon happens easier, and the on-state current becomes higher. The optimal device design parameters can be obtained by analyzing the effects of the device sizes on the device performance, which can help to reduce the process complexity and further improve the device overall performance.

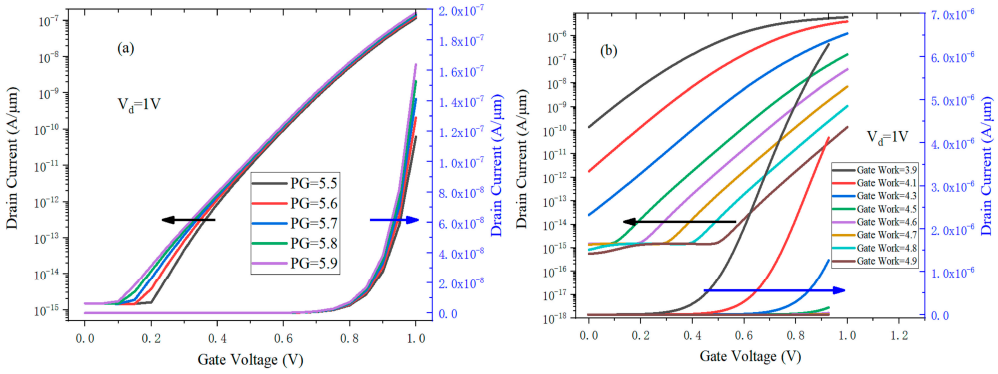

Figure 8. The effect of the gate work function on the transfer characteristics (**a**) the polar-gate work function; and (**b**) the control-gate work function.

3.4. Capacitance Characteristics

It is known that the frequency characteristics and amplification capability of an integrated circuit are closely related to the total gate capacitance, and the total gate capacitance is mainly composed of the gate-to-drain capacitance and gate-to-source capacitance. The capacitance characteristics of the JLTFET and H-JLTFET is simulated at the small signal frequency of 1 MHz. Owing to the formation of a heterogeneous gate dielectric under the control-gate, the total gate capacitance and gate-to-drain capacitance of the H-JLTFET are lower than that of the JLTFET, as shown in Figure 9. The total gate capacitance of the JLTFET and H-JLTFET is mainly determined by the gate-to-drain capacitance when the gate voltage is higher than 0.5 V. The miller capacitance is mainly determined by the gate-to-drain capacitance, so the miller capacitance of the H-JLTFET is smaller than that of the JLTFET. The reason for this is that the source/channel tunnel junction turns on as the gate voltage increases, and a large amount of electrons can pass through the tunnel junction to flow into the drain region, which can lead to an increase of the electron concentration and the gate-to-drain capacitance near the drain region. Meanwhile, the gate-to-source capacitance is kept at a small value due to the higher tunnel barrier at the drain/channel tunnel junction.

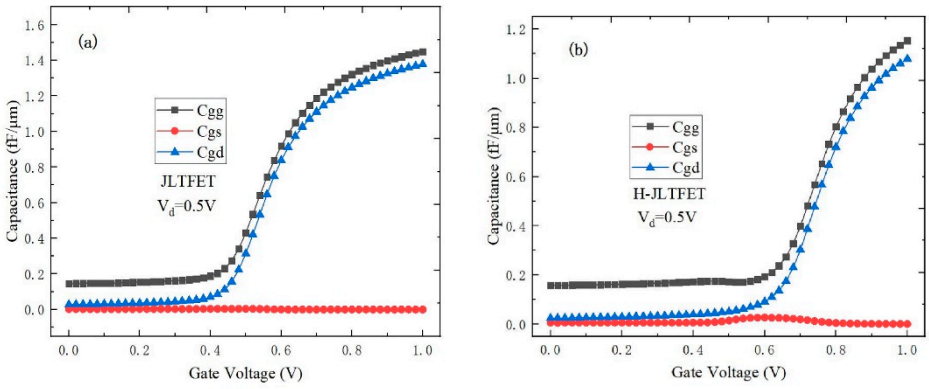

Figure 9. Capacitance characteristics of (**a**) JLTFET; and (**b**) H-JLTFET.

3.5. Frequency Characteristic

The frequency characteristics could be evaluated by the cutoff frequency and the gain bandwidth product [27]. Here, the cutoff frequency can be calculated by the ratio of the transconductance to the total gate capacitance, and the relevant equation (3) is as follows:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+2C_{gd}/C_{gs}}} \approx \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} = \frac{g_m}{2\pi C_{gg}} \tag{3}$$

For the fixed static gain of 10, the gain bandwidth product can be calculated through Equation (4):

$$GWB = g_m/2\pi 10C_{gd} \tag{4}$$

To improve the frequency characteristics, it is very effective to increase the transconductance, and to reduce the total gate capacitance and gate-to-drain capacitance by observing Equations (3) and (4).

Figure 10a, b respectively shows the cutoff frequency and gain bandwidth product of the JLTFET and H-JLTFET. The H-JLTFET can obtain a maximum cutoff frequency of 0.68 GHz and gain bandwidth product of 0.072 GHz when the gate voltage is 1.24 V. However, the conventional JLTFET has a maximum cutoff frequency of 0.039 GHz and a maximum gain bandwidth product of 0.004 GHz when the gate voltage is 1.68 V. The cutoff frequency and gain bandwidth product of the H-JLTFET are 17 times higher than that of the conventional JLTFET, so the H-JLTFET can get better frequency characteristics. This is because the H-JLTFET has a higher transconductance, and lower total gate and gate-to-drain capacitances. Therefore, the H-JLTFET is more suitable for low-power analog circuits.

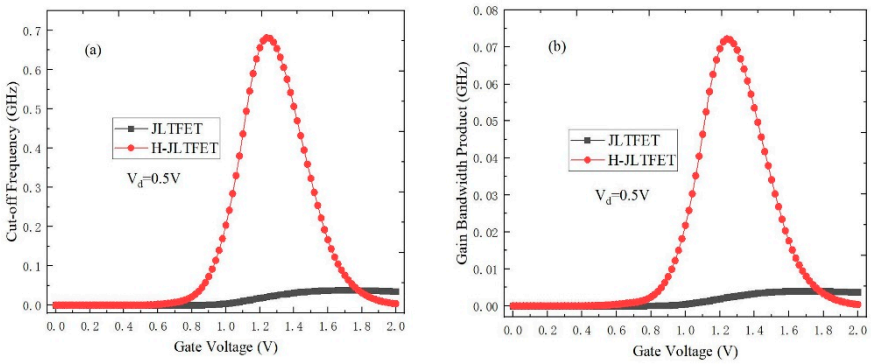

Figure 10. (**a**) Cutoff frequency; and (**b**) gain bandwidth product of the JLTFET and H-JLTFET.

4. Conclusions

To improve the on-state current and reduce the miller capacitance of the conventional JLTFET, the H-JLTFET is constructed and researched in this paper through the SILVACO-ATLAS. Compared to the conventional JLTFET, the differences of the H-JLTFET are that the source region uses germanium material to improve the on-state current; and the gap region between the polar-gate and control-gate uses $Si_{0.3}Ge_{0.7}$ material to reduce the tunnel distance. Moreover, the gate dielectric adjacent to the drain region uses low-k dielectric material SiO_2, which is considered to reduce the gate-to-drain capacitance effectively. The simulation results show that the H-JLTFET can achieve an on-state current of 6 μA/μm and switching ratio of 2.6×10^{12} when the gate voltage is 1 V, which means that the on-state current and switching ratio increase by one and four orders of magnitude, respectively. In addition, the effects of the device sizes, doping concentration and work function on the performance of the H-JLTFET are researched systematically to optimize the overall device performance. Compared to the JLTFET, the gate-to-drain capacitance, off-state current and power consumption of the H-JLTFET can be suppressed, and the H-JLTFET has a higher on-state current and frequency characteristics, so it has great potential in low power integrated circuit applications.

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