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A 3GS/s 12-bit Current-Steering Digital-to-Analog Converter (DAC) in 55 nm CMOS Technology

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Abstract: A 3GS/s 12-bit current-steering digital-to-analog converter (DAC) fabricated in 55 nm complementary metal–oxide–semiconductor (CMOS) technology has been presented. A partial randomization dynamic element matching (PRDEM) method based on switching sequence optimization is proposed to mitigate the mismatch effect and suppress the harmonic distortion with low hardware complexity. In the switching current cell, the cascode structure together with "always-ON" small current sources are used to keep the output impedance high and uniform. A compact layout of the switching current array is carefully designed, featuring short wires routing and small parasitic capacitance. According to the measured results at 3GS/s, this DAC demonstrates a spurious-free dynamic range (SFDR) of 74.64 dBc at low frequency and 50 dBc at 1.5 GHz output. The chip occupies an active area of 0.2×0.48 mm^2 and consumes a total power of 495 mW.

Keywords: digital-to-analog converter (DAC); spurious-free dynamic range (SFDR); current-steering; partial randomization dynamic element matching (PRDEM); switching sequence optimization; "always-ON" current source

1. Introduction

High-speed, high-precision digital-to-analog converters (DACs) are widely used in communication systems, direct digital synthesizers and instrumentation [1–5]. A critical challenge for DAC is to realize a high spurious-free dynamic range (SFDR) for wideband applications. The basic types of DACs generally include resistive, capacitive, and current-steering structure. Resistive and capacitive DAC usually need an output buffer to provide sufficient driving capacity, and the speed and linearity of the output buffer will limit the performance of high-speed DAC. In contrast, the current-steering DAC can directly drive the load without the need for additional buffer, and the output current is converted to voltage by using simple resistor. Therefore, compared with the capacitive or resistive structure, the current-steering structure is the preferred choice for DAC implementation nowadays. The dynamic performance of current-steering DAC is generally degraded by many factors, mainly including: (1) load variation effect, especially parasitic capacitance-induced finite output impedance; (2) current sources mismatch; and (3) signal-dependent switching transients. To overcome these problems, the cascode structure together with "always-ON" small current sources are used to keep the impedance high and uniform. The dynamic element matching (DEM) technique, featuring the random selection of current sources, can be employed to mitigate the mismatch effect and relax the matching requirement for current sources, enabling the use of small transistors, thus allowing a more compact design of the

current cells. This results in shorter wires and smaller parasitic capacitance, which are beneficial to reduce the errors caused by the switching operation of the internal current sources [6–9].

In this paper, a 3GS/s 12-bit current-steering DAC prototype fabricated in 55 nm CMOS technology is presented. A method combining DEM and current sources switching scheme optimization is adopted to suppress both the random and systematic errors with less circuit complexity. The switching current cell with "always-ON" characteristic is designed, and the relevant array layout is deliberately implemented. The measurement results reveal that the SFDR of the DAC is 74.64 dBc at low frequency and greater than 50 dBc over the entire Nyquist zone.

2. Proposed DAC Architecture

Considering the trade-off between complexity, area, speed, power, and linearity, a segmented architecture of DAC was chosen. The four most significant bits (MSBs) are thermometer-coded, which have advantages of guaranteed monotonicity and reduced glitch energy. The 8 least significant bits (LSBs) are binary with respect to compactness and simplicity, which can reduce the chip area and wiring complexity [10–13]. The DAC mainly consists of low-voltage differential signaling (LVDS) receiver, multiplexer (MUX), encoder and DEM, delay equalizer, switching current source array, and clock distribution network, as shown in Figure 1.

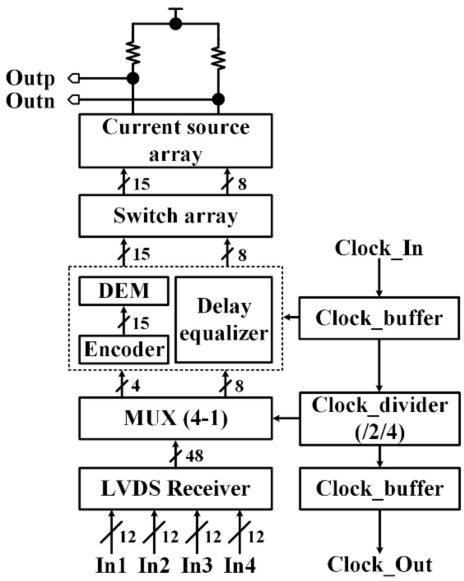


Figure 1. Digital-to-analog converter (DAC) architecture.

MUX is integrated on-chip to reduce the digital interface data rate. Four parallel digital input signals (a total of 48 pairs of differential signals) with bit stream of 0.75 Gbps per channel are provided off-chip via the LVDS receiver, then synthesized by 4-1 MUX into 1-way 3 Gbps bit stream for the DAC core processing. The 4 MSBs are transformed to 15-bit thermometer codes by encoder, and then fed into the DEM module. The delay equalizer aligns the lower 8 LSBs with the higher bits, cancelling out the delay between signal paths. After that, all the data is passed to the switching current sources array to control the output current. The DAC output is terminated with a pair of load resistors used to convert current into voltage. The transmission direction of the clock signal is opposite to the data path, and the divided clock signal is sent out of the chip, reserved for data synchronization purposes.

3. Circuits Implementation Details

3.1. Partial Randomization Dynamic Element Matching Based on Switching Sequence Optimization

In the high-speed current-steering DAC, errors affecting performance can be divided into two categories: random errors and systematic errors [11]. Usually, the simplest way to reduce random errors is to increase the device size so as to improve the matching. However, this will result in a larger layout dimensions, and consequently, the systematic errors such as gradient error will increase. In addition, a large area can cause a timing skew problem due to the presence of more parasitic component mismatches and increased routing complexity [14].

Some switching schemes for current sources have been used to minimize the deterministic gradient error. According to the characteristics of error distribution, if the turn-on sequence of the current sources is optimized, the accumulated residual error can be reduced, thus counteracting the influence of systematic errors [15–17]. In reference [17], an optimized switching sequence is proposed to compensate for the linear gradient error in the current sources array, exhibiting the lowest integral nonlinearity (INL) with the minimum variance. In this design, by using the method in reference [15,17], four groups of optimal switching sequence for 15 unary current sources are obtained, which are superior to the sequential sequence and symmetrical sequence in term of INL and variance, as shown in Table 1. When calculating the INL and variance of different switching sequences, it is assumed that the error sequence corresponding to the sequential sequence [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] is [−7, −6, −5, −4, −3, −2, −1, 0, 1, 2, 3, 4, 5, 6, 7].

Table 1. Performance comparison of different switching sequences for one-dimensional 1 × 15 array.

	Switching Sequence	INL *	Variance
Sequential sequence	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	28	421.86
Symmetrical sequence	13, 11, 9, 7, 5, 3, 1, 15, 2, 4, 6, 8, 10, 12, 14	7	9.33
Optimized sequence (4 groups)	8, 6, 10, 4, 12, 2, 14, 15, 1, 13, 3, 11, 5, 9, 7 7, 9, 5, 11, 3, 13, 1, 15, 14, 2, 12, 4, 10, 6, 8 8, 10, 6, 12, 4, 14, 2, 1, 15, 3, 13, 5, 11, 7, 9 9, 7, 11, 5, 13, 3, 15, 1, 2, 14, 4, 12, 6, 10, 8	4	4.8

* INL, integral nonlinearity.

Although the switching sequence optimization can reduce the gradient error, the random error still exists, and DEM technique is a feasible solution for such situation. The core operation of DEM is carried out by the scrambler, which executes the process of randomly mapping the inputs to the outputs. The mapping of the scrambler can be considered as a combinations problem [18]. Compared with the full randomization DEM, which suffers from excessive hardware overhead, the partial randomization DEM (PRDEM) technique only utilizes a subset of all combinations and allows for a limited degree of scrambling, providing a trade-off between harmonic distortion suppression and hardware complexity [19,20]. By randomly selecting one of several possible usage patterns of unary current sources array, the PRDEM converts the error resulting from the mismatches to white pseudorandom noise which is uncorrelated with the input sequence, such that the harmonic distortion is scrambled into white noise, thereby obtaining an improved SFDR with a slight increase in the DAC noise floor [21–27].

In this design, a PRDEM technique together with optimization strategy for current source switching sequence is presented, and the implementation is shown in Figure 2.

The scrambler of PRDEM realizes the random permutation using two stages of MUXs, controlled by pseudo-random sequence P<0:1> from the pseudo-random binary sequence (PRBS) generator. The MUX selectively passes one of the two inputs to the output under the control bits P<0:1>, which has an equal probability of being 1 or 0 and are independent of the input sequence. When P<0:1> changes randomly between “00”, “01”, “10”, and “11”, the input is randomly mapped to the output based

on the four configurations of optimized switching sequence. Taking P<0:1> = "00" as an example, the mapping relationship between the input Ti (i = 1–15) and the output TTi (i = 1~15) of PRDEM is as follows:

$$\begin{array}{ccccccccccccccc} T1 & T2 & T3 & T4 & T5 & T6 & T7 & T8 & T9 & T10 & T11 & T12 & T13 & T14 & T15 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ TT9 & TT6 & TT11 & TT4 & TT13 & TT2 & TT15 & TT1 & TT14 & TT3 & TT12 & TT5 & TT10 & TT7 & TT8 \end{array} \quad (1)$$

The switching sequence corresponding to the above mapping relationship is [8, 6, 10, 4, 12, 2, 14, 15, 1, 13, 3, 11, 5, 9, 7], which is one of the four optimized configurations.

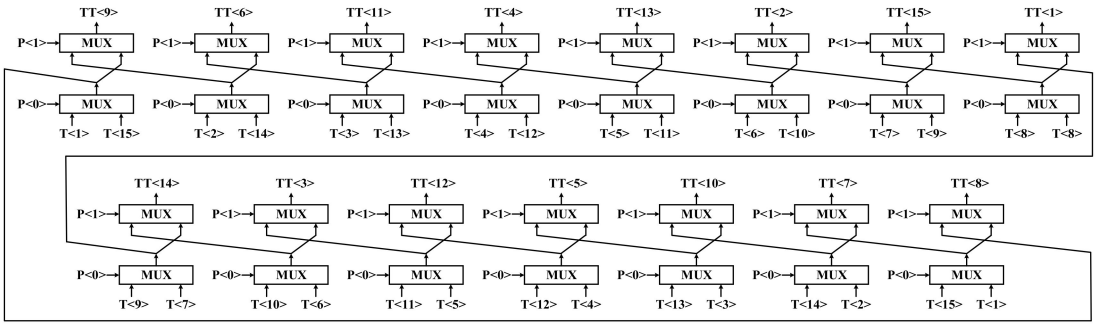


Figure 2. The implementation of the partial randomization dynamic element matching (PRDEM) based on switching sequence optimization.

In general, PRDEM based on switching sequence optimization achieves simultaneous suppression of systematic and random errors with less design complexity, and the matching requirements for the current sources is relieved. Therefore, the usage of small size transistors is possible, the resultant smaller areas and shorter routing wires help reduce the parasitic effects, and the SFDR at high frequency can be improved.

3.2. Switching Current Cell Design

The performance of DAC is largely determined by the design of switching current cell, which is composed of current source and switching differential pair, as shown in Figure 3.

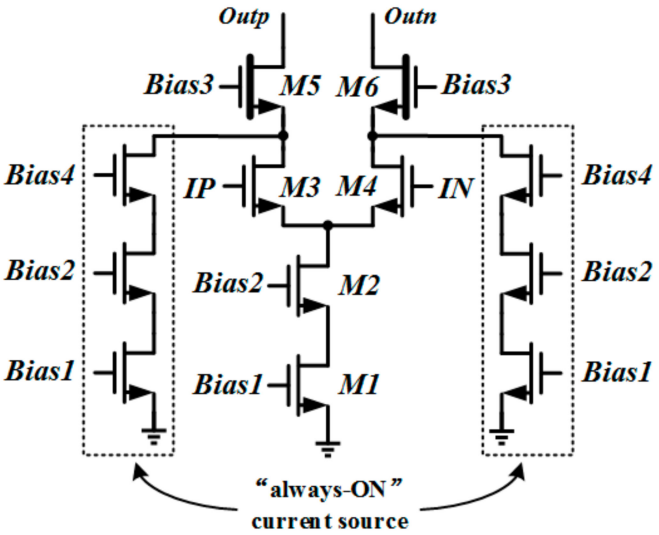


Figure 3. Switching current cell with "always-ON" current sources.

M1 is essentially a current source transistor with a large size to support the required matching. M2 is a cascode transistor that isolates the switching pair M3/M4 from the current source M1, and its size is as small as possible to reduce the parasitic capacitance at the sources of M3/M4. The switching pair M3/M4 should be designed with minimum size for tolerant mismatch to speed up the switching operation. The cascode transistors M5/M6, which are thick gate oxide type to accommodate the large swing of output signal, are used to increase the output impedance [28]. Unfortunately, this conventional method of impedance enhancement works only at low frequencies, but not as well at high frequencies. Due to the parasitic effect, the output impedance of the switching current cell is finite and decreases with the increase of frequency. The linearity is affected since there will be a current division between the load impedance and the DAC output impedance. Besides, when the current switch is in "on" or "off" state, the output impedance is different to some extent, meaning that the output impedance is signal-dependent, which will cause harmonic distortion.

In order to solve this problem, small "always-ON" current sources are added to the sources of M5/M6 [10]. This not only balances the output impedance before and after switching, but also prevents M5/M6 from being turned off completely even if M3/M4 are turned off, keeping them active and in a weak conduction. As a result, the switching speed of M3/M4 is much faster than that without "always-ON" current sources, which can make the switching action of the whole switching current sources array more consistent and help to reduce the signal-dependent switching delay, thus alleviating the impact of timing error at high frequency. Simulation results show that the effect can be significant when the "always-ON" current is set to 5–10% of the main current.

3.3. Switching Current Array Layout

For high-precision DAC, the current weights vary greatly. For the segment ratio of 4–8, the weight of the unary current sources (M1–M15) controlled by thermometer code is 256 times that of the minimum binary current source (L1) in LSBs. If the size of L1 is taken as the benchmark, the size of M1–M15 is 256 times that of L1, and this will bring great challenges to the layout design. The current sources array design is oriented by reasonable layout, focusing on the overall floorplan and placement. The size difference between the horizontal and vertical dimensions should not be too large, avoiding too long and narrow ship, otherwise it is not conductive to wires routing. First of all, the current sources array can be optimized from the circuit level, the appropriate transistor size is selected, and the number of transistors contained in each current source is determined. In this design, L3 is selected as the benchmark, which is composed of a unit transistor M_{CS}. Current sources with weights higher than or lower than L3 are made up of a certain number of transistors in parallel or in series [8], respectively, as shown in Figure 4.

High frequency performance benefits from simplicity and low parasitic capacitances. Accordingly, a well-designed compact floorplan in Figure 5 is adopted without using special intricate layout patterns, featuring short wire routings for current sources connections.

The MSBs section includes 15 current sources, each occupying two columns for a total of 30 columns. The LSBs section occupies eight columns. In summary, the current sources array contains 32 rows and 38 columns of transistors. In the middle of the layout, LSBs and MSBs current sources are arranged in an interleaving way, and LSBs current sources are symmetrical, while the remaining MSBs current sources are located on both sides. The LSBs have a small current weight, requiring only a small number of transistors to supply the operating current, and the extra transistors in every LSBs column are used as dummy transistors, which are set to have the same current as the normal current unit for the purpose of thermal distribution equalization. Moreover, the outermost columns and rows of the whole current source area are surrounded by dummy rings, providing identical environment to the inner ones and reducing the edge effect. Also, they can offer filtering for bias voltages.

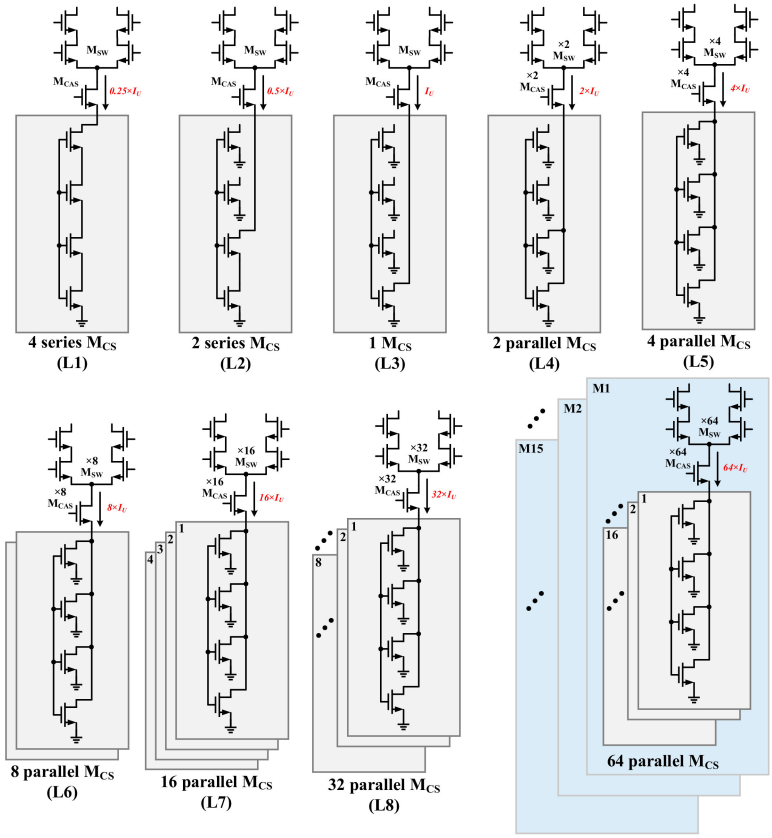


Figure 4. Switching current sources array design.

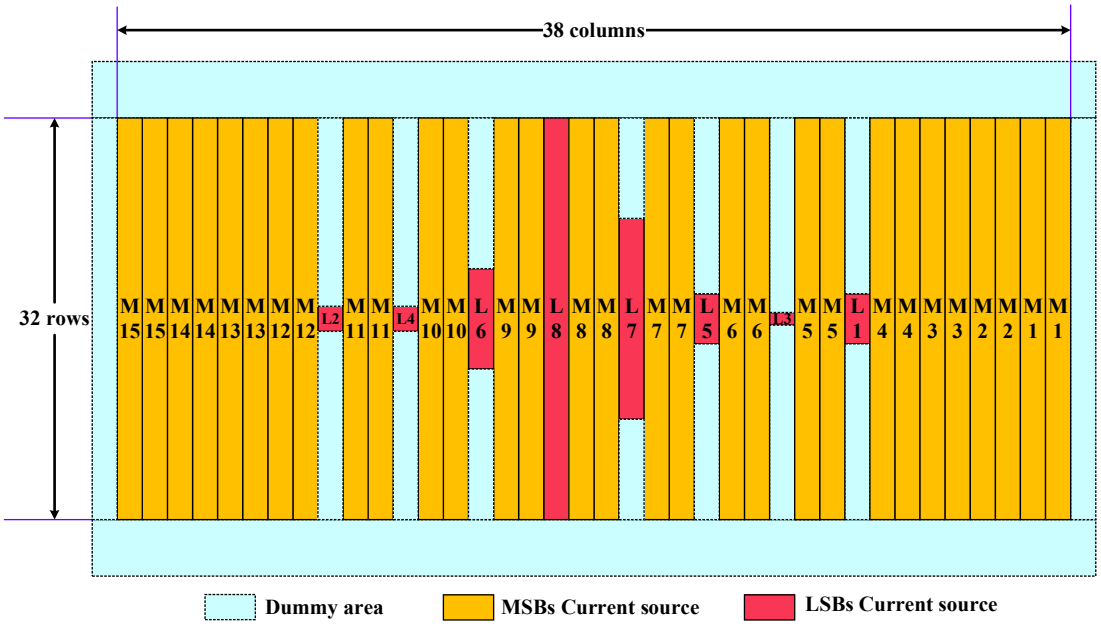


Figure 5. Current sources array layout floorplan.

Other modules such as switch array and cascode parts are similarly divided, floorplanned, and placed close to their corresponding current source groups. The final layout of the switching current array is shown in Figure 6.

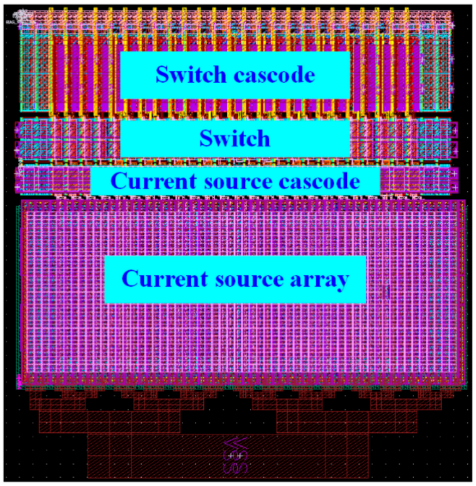


Figure 6. The switching current array layout.

4. Measured Results

The DAC prototype is manufactured in 55 nm CMOS technology with chip size of 2.95×2 mm^2, which is mainly limited by input/output (I/O) PADs, and the DAC core occupies only a small area of 0.2×0.48 mm^2. The micrograph is shown in Figure 7.

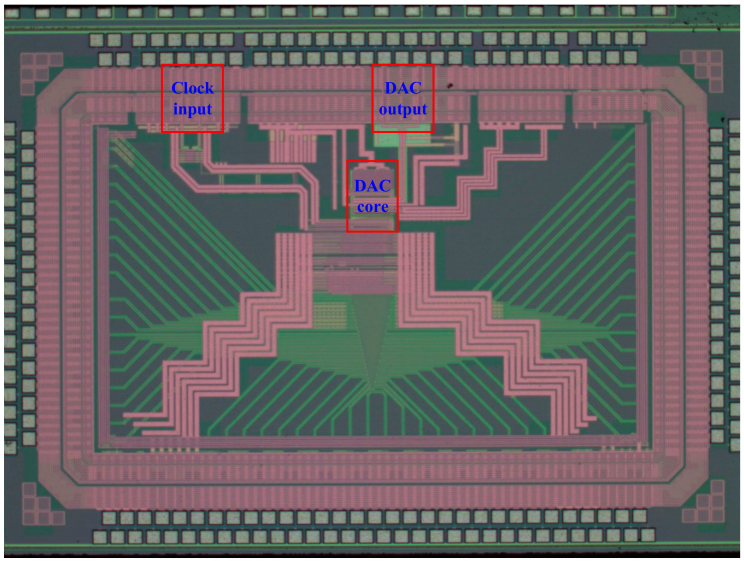
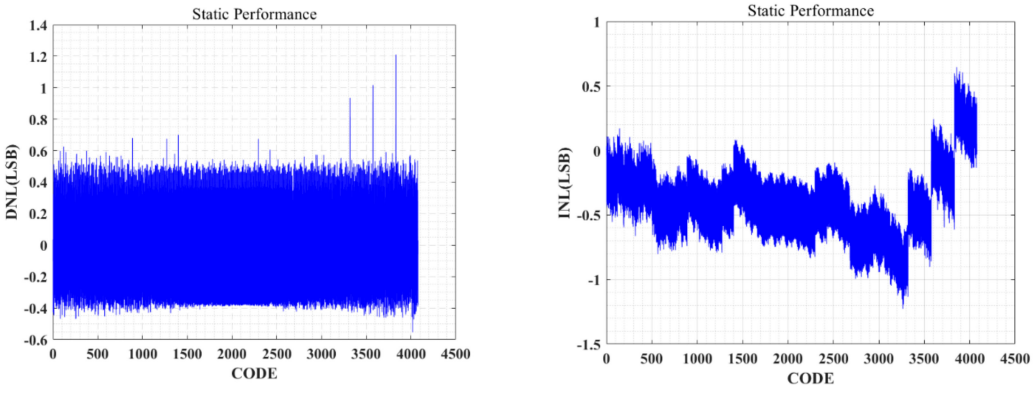


Figure 7. The micrograph of the DAC chip.

In the process of testing, the input digital codes are generated from a field progammable gate array (FPGA) board, and an on-board wideband balun is used to convert the differential output into single-ended signal. The total power dissipation is 495 mW.

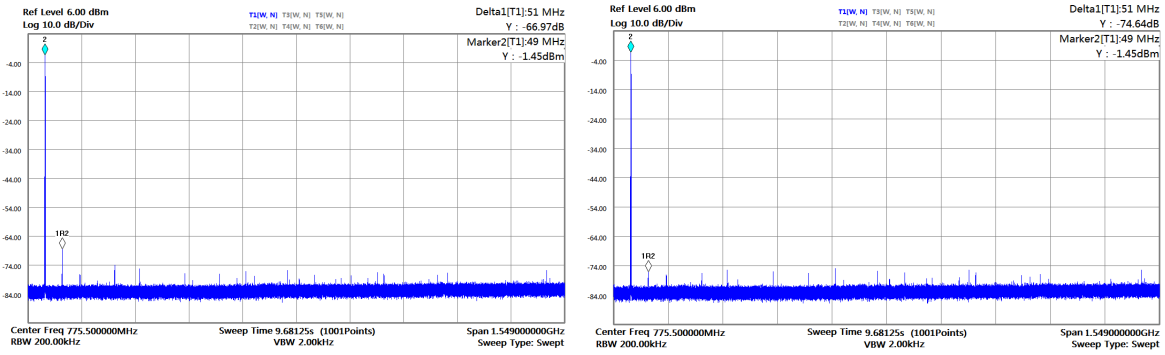
The static performance of differential nonlinearity (DNL) and INL is shown in Figure 8, where the DNL is −0.55/+1.21 LSB, and the INL is −1.22/+0.64 LSB.

The dynamic performance is measured at 3 GHz sample rate. Figure 9 shows the measured spectrum of the 49 MHz output with DEM on or off. The SFDR is 66.97 dBc with DEM off. When the DEM is on, the highest harmonic power is largely suppressed, and the SFDR is increased by 7.67 dB to 74.64 dBc.



(**a**) (**b**)

Figure 8. Measured static performance (**a**) differential nonlinearity (DNL); (**b**) integral nonlinearity (INL).



(**a**) (**b**)

Figure 9. Measured spectrum at the 49 MHz output (**a**) with dynamic element matching (DEM) off; (**b**) with DEM on.

The DEM effectiveness is illustrated in Figure 10, where the SFDR versus output frequency with DEM off and on are shown. When DEM is enabled, the SFDR is improved by 6–8 dB in low frequency range and 3–5 dB in high frequency region, and the SFDR stays above 50 dB across the entire Nyquist zone.

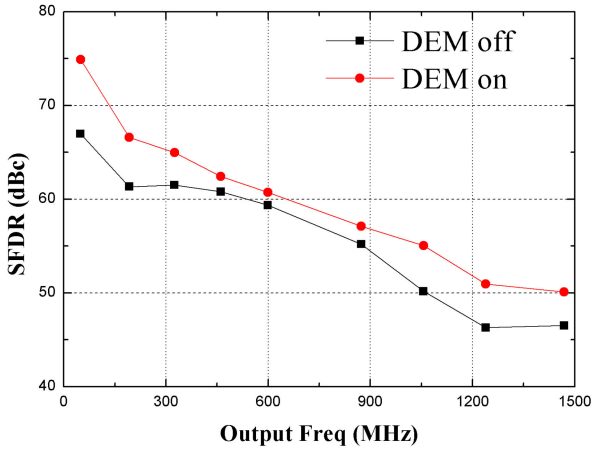


Figure 10. The spurious-free dynamic range (SFDR) comparison with DEM off and on.

A performance summary and a comparison with prior arts are shown in Table 2.

Table 2. Comparison of ultra-high speed DACs.

	2009 JSSC [10]	2014 JSSC [8]	2014 ISSCC [29]	2018 IEICE [30]	This Work
Technology	65 nm	40 nm	65 nm	65 nm	55 nm
Sample Rate (GS/s)	2.9	1.6/2.8	3.2	2	3
Resolution (bits)	12	12	16	14	12
Best SFDR (dBc) at low frequency	74	74/58	84	78.2	74.64
SFDR (dBc) at high frequency	50 at 650 MHz	70.3 at 0.8 GHz 48 at 1.4 GHz	58 at 600 MHz	53 at 310 MHz	50 at 1 GHz
DNL/INL (LSB)	0.3/0.5	N/A	N/A	N/A	1.21/1.22
Power consumption (mW)	188	40/47	240	490	Total: 495 Core: 284

5. Conclusions

A prototype of 3GS/s 12-bit current-steering DAC in 55 nm CMOS technology has been demonstrated. A hardware efficient PRDEM technique together with optimization strategy for current source switching sequence was adopted to improve the matching of current sources and SFDR. The switching current cell with "always-ON" characteristic was designed, and the relevant array layout was deliberately implemented. With DEM on, the measured SFDR improved by 6–8 dB in low frequency range and 3–5 dB in high frequency region, and the SFDR stayed above 50 dB across the entire Nyquist zone. The total power consumption was 495 mW, and the chip size was 2.95×2 mm^2 with the DAC core area of 0.2×0.48 mm^2.

Author Contributions: D.W. (Dong Wang) designed the circuits, analyzed the measurement data, and wrote the manuscript. X.G., L.Z. and D.W. (Danyu Wu) assisted the circuit implementation and simulation. J.L. and H.L. performed the chip test. J.W. contributed to the technical discussions and reviewed the manuscript. X.L. gave some valuable guidance and confirmed the final version of manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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