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A Semi-Floating Gate Memory with Tensile Stress for Enhanced Performance

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Abstract: With the continuous scaling down of devices, traditional one-transistor one-capacitor dynamic random access memory (1T-1C DRAM) has encountered great challenges originated from the large-volume capacitor and high leakage current. A semi-floating gate transistor has been proposed as a capacitor-less memory with ultrafast speed and silicon-compatible technology. In this work, a U-shaped semi-floating gate memory with strain technology has been demonstrated through TCAD simulation. Ultra-high operation speed on a timescale of 5 ns at low operation voltages (≤ 2.0 V) has been obtained. And the tensile stress induced in its channel region by using contact etch stop layer (Si_3N_4 capper layer) was found to significantly improve the drain current by 12.07%. Furthermore, this device demonstrated a favorable retention performance with a retention time over 1 s, and its immunity to disturbance from bit-line has also been investigated that could maintain data under the continuous worst writing disturbance operation over 10 ms.

Keywords: semi-floating gate transistor; contact etch stop layer; tensive strain; retention; disturbance

1. Introduction

The large volume capacitor of the one transistor (1T)-one capacitor (1C) DRAM has limited its further applications in advanced memory fields with shrinking cell size [1–3]. Various capacitor-less memory devices have thus been proposed to avoid the problems associated with the scaling of a capacitor and achieve high memory density [4–8]. One promising candidate is the semi-floating gate transistor (SFGT) with an embedded tunneling field-effect transistor (TFET) [8,9]. The structure of a semi-floating gate to restore charges and the embedded TFET for charging has enabled a high writing speed with low operation voltage. However, the drain current of the SFGT is relatively small leading to unsatisfactory sensing capabilities due to the tunneling mechanism which is similar to that of traditional TFET devices.

The employment of strain technologies in modern electronic devices to improve mobility and drive current has been developed for decades in advanced complementary metal-oxide-semiconductor (CMOS) transistors [10–15]. However, most of these technologies, such as embedded SiGe [10] and embedded Si:C [13], request complex process steps, making them not suitable or transferrable to a wider range of advanced processes. Hence, the tensile-stress contact etch stop layer (CESL) has gained popularity for its simplicity as well as good reliability and has been integrated into the CMOS fabrication process [14–19].

Here, we performed a 2D simulation study on a U-shaped channel SFGT memory by using Sentaurus TCAD [20] tool based on the 40 nm technology node. The mechanical stress introduced by tensile Si_3N_4 capper layer was found to be effective in enhancing the drain current by 12.07%. In

addition, the retention and disturbance performance of the U-shaped SFGT memory were systematically studied as well.

2. Simulation and Results

2.1. Device Structure and Operation

The structure and doping contour of the U-shaped SFGT memory with the Si_3N_4 capper layer are shown in Figure 1a. The channel of the U-shaped floating-gate metal-oxide-semiconductor field-effect transistor (FG-MOSFET) is recessed into the substrate to increase the physical channel length of the MOSFET, which is expected to alleviate the short channel effect and obtain larger Cox to store more charges. A PN junction is formed via a contact window between the p+ doped U-shaped semi-floating gate (SFG) and the n+ doped drain region. The control gate (CG) extended over the PN diode makes it an embedded TFET, which can regulate charges in the SFG. Moreover, to introduce mechanical stress in the channel of the FG-MOSFET, a 100 nm Si_3N_4 capper layer with intrinsic stress of 1 GPa is deposited over the device.

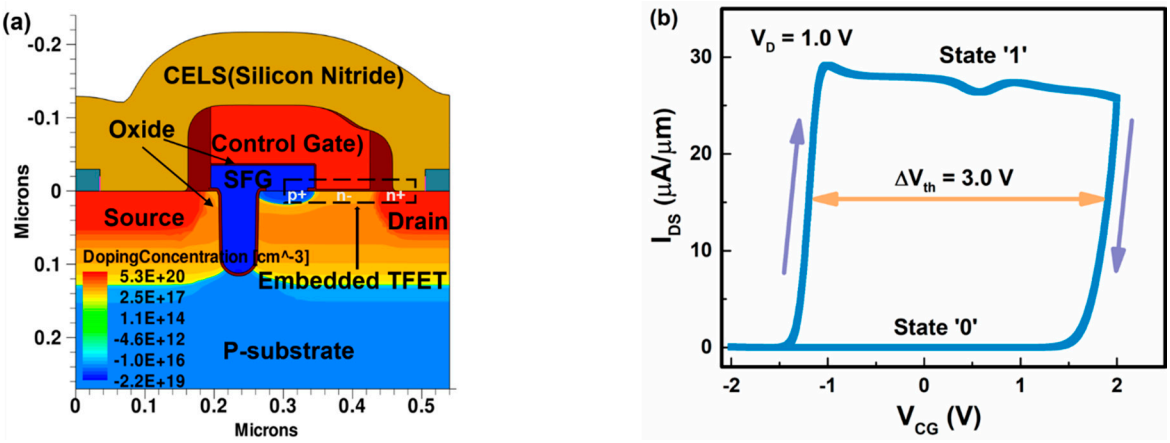

Figure 1. (**a**) Schematic of the U-shaped semi-floating gate transistor (SFGT) structure with tensile Si_3N_4 capper layer (CELS) and the doping contour used in the simulation; (**b**) The simulated transfer curve of the U-shaped SFGT device. The V_{th} has shifted 3.0 V when the device was switched between state 1 and state 0.

The simulated transfer characteristic of the U-shaped SFGT memory is presented in Figure 1b. The V_D is set to 1.0 V, and the V_{CG} is swept from −2 V to 2 V in dual sweep model. The embedded TFET is turned on at the initial time with V_{CG} of −2 V and positive charges are written into the SFG. Meanwhile, the increase of V_{CG} also contributes to a higher SFG potential to turn on the FG-MOSFET. And the TFET is nearly switched off when the V_{CG} becomes positive. However, the high potential of the SFG still keeps the FG-MOSFET at on state and the drain current almost keeps unchanged. With increasing V_{CG}, the PN junction of the embedded TFET becomes forwardly biased and the charges in the SFG are emptied resulting in a high threshold voltage (V_{th}). Then, the FG-MOSFET is turned off with a decreasing V_{CG} during back sweeping. As shown in Figure 1b, the threshold voltage has shifted ~3.0 V between state 0 and state 1 by modulating the amount of charges in the SFG through the embedded TFET.

The operation condition of the U-shaped SFGT memory is illustrated in Table 1. During the write-1 operation, the positive bias of 1.4 V for V_D lowers the energy band of the drain region while the control gate with a negative bias of −2.0 V inverts the n-doped drain extension region that boosts the energy band. Therefore, band-to-band tunneling (BTBT) occurs at the place where the energy band

bends the strongest. The rate contour of the BTBT generation is shown in Figure 2a. The Kane BTBT model [21,22] is used to calculate the band-to-band generation rate, which is expressed as follows:

$$G_{BTBT} = A_{BTBT} \times \frac{E^2}{E_g^{\frac{1}{2}}} \times \exp\left(-B_{BTBT} \times \frac{E_g^{\frac{3}{2}}}{E}\right) \quad (1)$$

where A_{BTBT} and B_{BTBT} are constants, E is the magnitude of the electric field, and E_g is the band-gap energy. Figure 2b has exhibited the corresponding energy band diagram along the horizontal cutline Y = 0.002 μm below extended control gate. Electrons from the valence band of the n− channel under the extended CG tunnel across the band gap to the conduction band of the n+ drain region, so that current flows from the drain region to the SFG. Then, the increased positive charges which are stored in the SFG cause a lower V_{th}.

Table 1. The operation condition of the U-shaped (semi-floating gate transistor) SFGT memory.

	Write-1	Write-0	Read	Standby
V_{CG} (V)	−2.0	1.5	0.7	0
V_D (V)	1.4	0.6	1.4	1.0
Time (ns)	5	5	5	8

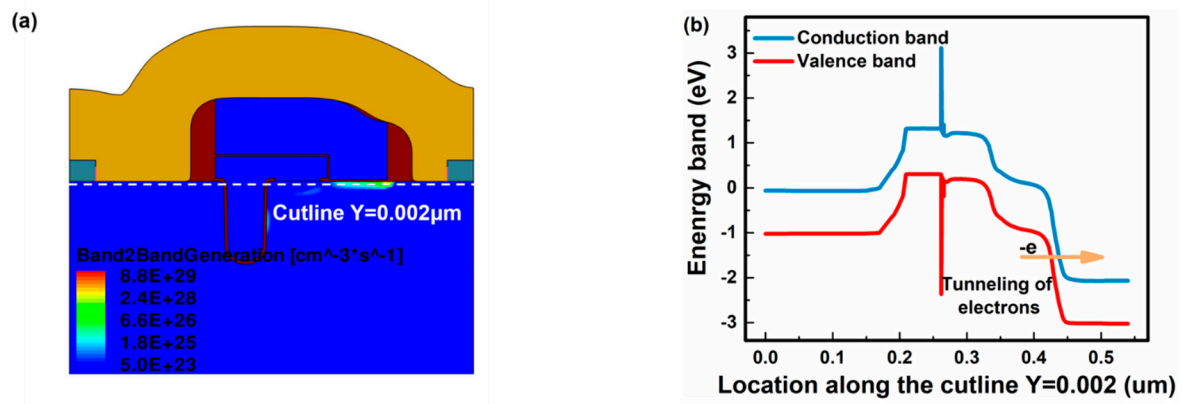

Figure 2. (**a**) Contour of the band-to-band tunneling generation rate of the embedded field-effect transistor (TFET) during the write-1 operation; (**b**) Energy band diagrams along the horizontal cutline Y = 0.002 μm shown in (a). The band-to-band tunneling occurs in the place where the band bending is strongest that electrons tunnel from the valence band of the inverted channel to the conduction band of the n+ drain region.

During the write-0 operation with 0.6 V V_D and 1.5 V V_{CG}, the electrostatic potential of the SFG is higher than that of the drain region. Therefore, the PN junction of the embedded TFET is forwardly biased and the current flows from the SFG to the drain region. And positive charges in the SFG that are emptied have resulted in a higher value of V_{th}. Additionally, reading is operated when the embedded TEFT is turned off with 1.4 V V_D and 0.7 V V_{CG}. The reading operation is nondestructive because the PN junction of the embedded TFET is reversely biased and the charges in the SFG are retained. The different read-out current between state 1 and state 0 is due to the different V_{th} of the FG-MOSFET, which depends on charges in the SFG because of capacitive coupling.

By optimizing the writing voltage V_{CG} and writing time of the write-1 operation, the U-shaped SFGT memory can obtain a sufficient sensing window for state 1 and state 0 as well as a high writing speed at low operation voltages. Figure 3a shows the dependence of electrostatic potential change (ΔEP) of the SFG on V_{CG} during write-1 operation. With a writing time of 5 s and the V_D of 1.4 V, a lower negative V_{CG} bends the energy band more significantly, resulting in more positive carriers written into the SFG. But when V_{CG} at −2.4 V and −2.8 V, the ΔEP changes a little since excessive

charges were written into the SFG that would diffuse out for its concentration gradient distribution. Hence it is better to choose the V_{CG} of −2.0V for write-1 operation. Figure 3b shows the relation between ΔEP of the SFG and the writing time for write-1 operation while keeping V_{CG} at −2.0 V and V_D at 1.4 V. Since the BTBT takes place during the entire writing time, a close-to-linear relationship has been observed between ΔEP and writing time. Therefore, to achieve an ultra-high writing speed and an adequate sensing window (~6.8 μA/μm in Figure 4b) at a relatively low operation voltage, −2.0 V and 5 ns are selected as the optimal values for control gate voltage V_{CG} and writing time of the write-1 operation, respectively.

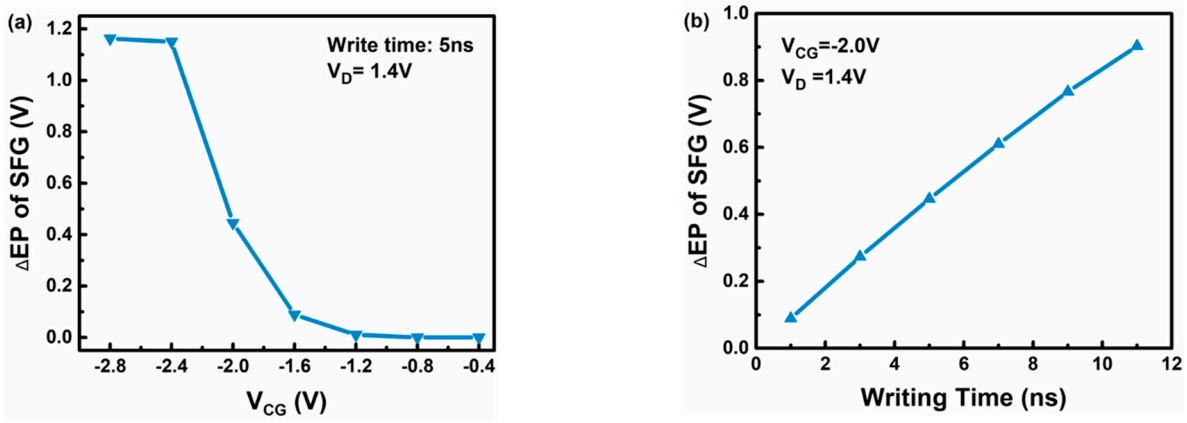

Figure 3. (**a**) The dependence of ΔEP of the semi-floating gate (SFG) on V_{CG} during the write-1 operation; (**b**) The relation between the ΔEP of the SFG and the writing time for write-1 operation. V_{CG} is −1.4 V and V_D is 2 V.

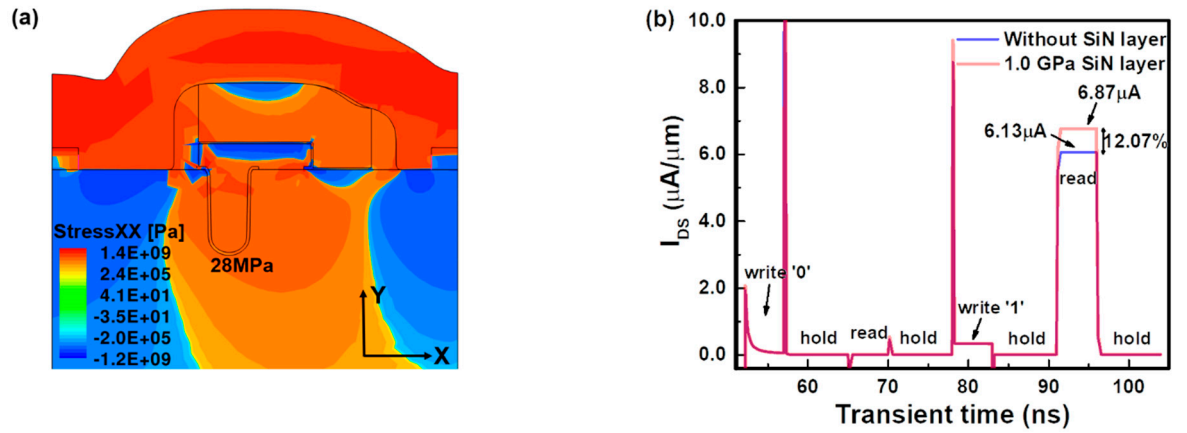

Figure 4. (**a**) Contour of stress XX along the channel direction; (**b**) Simulated drain current enhancement of SFGT memory with the tensive Si_3N_4 layer during a period of the operation sequence.

2.2. *Effect of the Tensile-Stress CESL*

The poly gate of the U-shaped SFGT is stretched laterally as the tensile Si_3N_4 capper layer are deposited on top of the device. Accordingly, tensive strain is introduced in the U-shaped channel region along the channel direction. In Sentaurus Process simulation, the stress-rebalancing step is conducted to re-establish the stress equilibrium in the structure to calculate the process induced mechanical stress. The effects of stress can be illustrated by employing the deformation potential model, strained effective mass and density of states (DOS) model for strained band gap as well as stress dependent mobility model in Sentaurus Device simulator [20,21]. As shown in Figure 4a of the lateral strain Stress XX distribution, there is compressive strain in the source and drain region while tensive strain exists in the channel region along the channel direction. The average value of lateral Stress XX under the U-shaped channel is 28 MPa. Benefited from the tensive strain, electrons transfer into the lower-energy level

conduction band with lower conductivity mass, and the intervalley scattering is also suppressed [11]. Both effects have contributed to a higher electron mobility., which further induces a higher drain current in the device.

Figure 4b shows the simulation results demonstrating the drain current improvement of the U-shaped SFGT by the tensive Si_3N_4 capper layer. The voltages of the operation sequence are applied according to Table 1. It is found that the read-out current of state 1 for the U-shaped SFGT memory with Si_3N_4 cap layer has reached up to 6.87 μA/μm which shows a 12.07% increase as compared with that in the conventional structure without the Si_3N_4 cap layer. Furthermore, the read-out current ratio of state 1 and state 0 is as high as 4.5×10^4 for the U-shaped SFGT memory with the Si_3N_4 cap layer.

2.3. Retention and Disturbance Performance

The retention performance of SFGT memory has also been systematically explored. As shown in Figure 5a, the retention time of state 0 and state 1 is both over 1 s which means that it is unnecessary to refresh the memory frequently. The simulation is executed as V_{CG} and V_D are kept at the standby condition after data "1" or data "0" has been written. For state 1, the amount of positive charges in the SFG is not sufficient enough to make the SFG potential higher than that in the drain region when the device is operated by V_{CG} ~0 V and V_D ~1.0 V. As a result, the PN junction between the SFG and the drain region is reversely biased. But at the same time, positive charges diffuse outside the SFG because of the concentration gradient, leading the degradation in the read-out current of state 1 after a long retention time. On the other side, the PN junction is also reversely biased for the retention situation of state 0 for the higher potential of drain region than the SFG. Thus, the reverse leakage current from the drain region to the SFG makes state 0 approaching state 1 over a long retention time of 1 s. The longer retention time can reduce the power consumption for frequent refresh operation of memory.

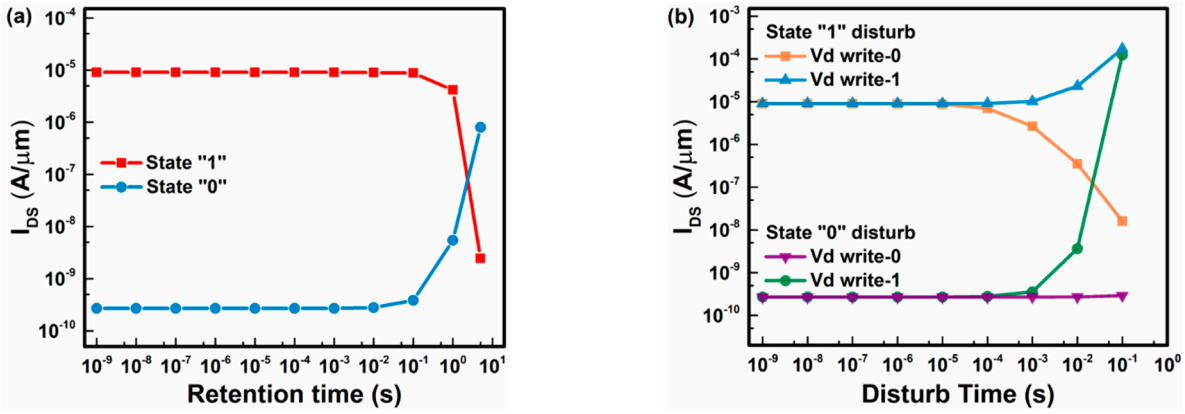

Figure 5. (**a**) Retention performance of the U-shaped SFGT memory. The retention time is over 1 s; (**b**) Disturbance performance of the U-shaped SFGT memory. The immunity time to the worst disturbance mechanism can be up to 10 ms.

Considering the U-shaped SFGT memory array programmed by page, cells connected to columns in the same row are simultaneously operated. Thus, each cell may be subjected to disturbances from the bit-line (V_D). The memory cell was first written to data 1 or data 0 and then kept in the hold state with the V_{CG} of 0 V and V_D of 1.0 V. When the neighboring cells from different rows but the same column were operated by write-0, write-1, or reading, disturbances occurred that V_D was kept in disturbance conditions because of a shared bit-line. The disturbance performance shown in Figure 5b was obtained by simulating a certain disturbance time.

There are six types of disturbances in total on state 1 and state 0 from the bit-line, but they can be simplified to four types for the same V_D of write-1 and reading operation. For state 1, the most serious disturbance is the V_D-write-0 disturbance with V_D of 0.6 V and V_{CG} of 0 V when the PN junction is weakly reversely biased for the relatively higher potential of the SFG with more positive

charges. However, state 1 is still weakened after 100 ms of disturbance time since there are diffusion currents flowing from the SFG to the drain region. The other type of disturbance on state 1, that is, the V_D-write-1 disturbance with V_D ~1.4 V and V_{CG} ~0 V does not degrade state 1. This is because more charges are written into the SFG as the embedded TFET is lightly turned on. Then, the read-out current increases slowly over a long period of time. As for the disturbance on state 0, the PN junction is reversely biased due to the low SFG potential of state 0 during the V_D-write-0 disturbance. Hence, the read-out current almost keeps unchanged. When it is disturbed by the V_D-write-1 operation, the embedded TFET is also weakly turned on such that charges are written into the SFG slowly. Thus, the read-out current of state 0 increases as the disturbance continues. As shown in Figure 4b, the state of the memory could still be distinguished when suffering from the worst disturbance over 10 ms, which means the SFGT memory is immune to at least 2×10^6 times of the continuous writing disturbance operations.

3. Conclusions

A novel U-shaped SFGT capacitor-less memory utilizing the CESL strain technology has been investigated in this work. It could be programmed with a low operating voltage ($\leq$ 2.0 V) and a short operation time (~5 ns). And the tensive strain in the U-shaped channel region which was introduced by the strained Si_3N_4 capper layer has improved the read-out current by 12.07%. More importantly, the SFGT memory cell obtained a retention time over 1 s that decreases the refresh rate and dynamic power consumption than the traditional 1T-1C DRAM with refresh time of 64 ms. And the device also exhibited a strong immunity to various disturbance that can maintain logic states over 10 ms even with the presence of continuous and worst writing disturbance operation. Thus, this U-shaped SFGT memory with the Si_3N_4 capper layer is believed to be a competitive candidate for future ultrafast, high-density and low-power random access memory.

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