electronics

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Electronic Circuit with Controllable Negative Differential Resistance and its Applications

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Received: 5 March 2019; Accepted: 3 April 2019; Published: 8 April 2019

Abstract: Electronic devices and circuits with negative differential resistance (NDR) are widely used in oscillators, memory devices, frequency multipliers, mixers, etc. Such devices and circuits usually have an *N*-, *S*-, or Λ-type current-voltage characteristics. In the known NDR devices and circuits, it is practically impossible to increase the negative resistance without changing the type or the dimensions of transistors. Moreover, some of them have three terminals assuming two power supplies. In this paper, a new NDR circuit that comprises a combination of a field effect transistor (FET) and a simple bipolar junction transistor (BJT) current mirror (CM) with multiple outputs is proposed. A distinctive feature of the proposed circuit is the ability to change the magnitude of the NDR by increasing the number of outputs in the CM. Mathematical expressions are derived to calculate the threshold currents and voltages of the N-type current-voltage characteristics for various types of FET. The calculated current and voltage thresholds are compared with the simulation results. The possible applications of the proposed NDR circuit for designing single-frequency oscillators and voltage-controlled oscillators (VCO) are considered. The designed NDR VCO has a very low level of phase noise and has one of the best values of a standard figure of merit (FOM) among recently published VCOs. The effectiveness of the proposed oscillators is confirmed by the simulation results and the implemented prototype.

Keywords: negative differential resistance; current-voltage characteristics; multiple simple current mirror; threshold voltage; oscillator; voltage-controlled oscillator

1. Introduction

Nowadays, negative differential resistance devices and circuits are widely used in oscillators, memory, frequency dividers, and multiplier circuits [1–5]. The presence of negative resistance in an electrical circuit makes it possible not to dissipate electrical energy in the form of heat, but to generate electrical power, even if it has only two terminals and not three as in transistors. There are two types of negative resistance, namely, differential and static. Sometimes NDR is also called negative dynamic resistance. The NDR is the first derivative of the voltage relative to the current at the operating point. The current-voltage characteristics with NDR region can be created in two ways. The first way involves the use of special electronic devices, such as a Gunn diode, a tunnel diode, three-terminal graphene NDR devices [6], and others. In the second way, the current-voltage characteristics with NDR region are created artificially with the help of special electronic circuits. However, the known NDR electronic circuits have some disadvantages that limit their use. Let us consider the well-known electronic circuits with NDR. The studies [7,8]

considered the NDR circuit based on complementary metal-oxide-semiconductor (CMOS) NDR inverters requiring two power supplies. Thus, to create the current-voltage characteristics with NDR region three terminals should be used. The study [9] considered an electronic oscillator based on a bipolar junction transistor (BJT)-metal-oxide-semiconductor field-effect transistor (MOSFET) structure with Λ-type current-voltage characteristics and two power supplies. The study [10] considered an NDR circuit composing three resistors and two BJT. The N-type current-voltage characteristics are achieved by selecting the appropriate resistor values. The study [11] considered a special connection of a BJT with a junction gate field-effect transistor (JFET) that has N-type current-voltage characteristics. However, this circuit is subject to thermal runaway, which makes it difficult to use the circuit in practice. The study [12] considered a novel sinusoidal NDR VCO for very high frequency band. The VCO circuit comprises a JFET in combination with a P–channel metal-oxide-semiconductor (MOS) improved Wilson current mirror (CM). The study [13] considered a new NDR circuit, which uses a FET and BJT transistors to create the S-type current-voltage characteristics. The study [14] considered a systematic method to design NDR circuits comprising two transistors and resistors only. The study [15] considered a comparison of five proposed NDR VCOs for microwave applications. The NDR circuits include a gallium-arsenide transistor and different BJT CMs. The study [16] considered a novel voltage-controlled NDR device, using complementary silicon-on-insulator four-gate transistors. The work experimentally demonstrated new circuits for the inductor-capacitor (LC) oscillator and Schmitt trigger based on the proposed NDR device. The study [17] considered a novel multiple NDR device with an ultra-high peak-to-valley current ratio by combining tunnel diode with a conventional MOSFET. The study [18] proposed complement double-peak NDR devices by combining tunnel diode with conventional CMOS and its compact five-state latch circuit by introducing standard ternary inverter. The study [19] considered four novel NDR circuits based on the combination of the standard n-channel MOS transistors and silicon-germanium heterojunction bipolar transistor (HBT). Depending on the design parameters, the proposed circuits can exhibit Λ- or N-type current-voltage characteristics. The study [20] considered a tri-valued memory circuit based on two cascoded MOS-BJT-NDR devices that can show the NDR current-voltage characteristic by adjusting the MOS transistor parameters. The study [21] considered a three-terminal voltage controlled Λ-type negative resistance MOSFET structure using the merged integrated circuit of a NELS (n-channel enhancement mode with load operated at saturation) inverter and an n-channel enhancement MOS driver.

It should be noted that in the reviewed NDR devices and circuits there is practically no possibility of increasing the negative resistance without changing the type of transistors or the dimensions of transistors. Moreover, some devices and circuits have three terminals assuming two power supplies. These circumstances significantly reduce the range of possible applications of NDR devices and circuits. For example, negative resistance may not be sufficient to start-up the oscillator circuit [22]. This paper proposes a new NDR circuit based on a FET in conjunction with multiple simple CMs, in which the magnitude of the negative resistance is easily controlled by changing the number of CM outputs. Description, mathematical and numerical modeling of the NDR circuit is given. The proposed NDR electronic circuit can be used in designing an oscillator, a VCO, an amplifier, etc. The most promising applications are related to generating ultrahigh-frequency signals with low phase noise.

2. Circuit Operation

Figure 1a shows the proposed NDR circuit, which consists of two bias resistors R_a and R_b, a FET (Q_0) and simple CM with $n-1$ outputs (collectors of transistors $\overline{Q_2, Q_n}$). We further assume that transistors $\overline{Q_1, Q_n}$ are matched. Figure 1b shows the current-voltage characteristics of the NDR circuit where the total current I_0 is a function of the power supply voltage V_{xy}. The steepness of the current-voltage characteristic between points β and γ depends on the number of outputs of the CM. Curve 1 corresponds to the one output of the CM, i.e., only transistors Q_1 and Q_2 are used. In this particular case, the differential resistance between points β and γ is positive, and the circuit does not

have an NDR region. When choosing the appropriate transistors, the circuit can have the NDR region even with one CM output.

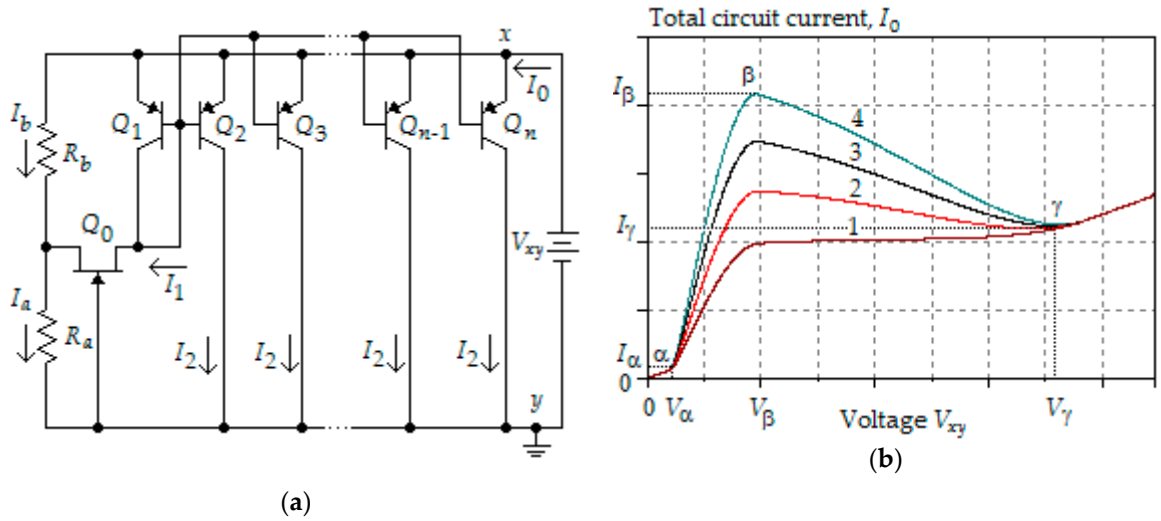


Figure 1. (**a**) Negative differential resistance circuit with multiple simple current mirror; (**b**) N-type current-voltage characteristics of the circuit.

As can be seen in Figure 1b, with an increase in the number of the CM outputs to two and further to four, the differential resistance becomes negative and the slope of the characteristic in the NDR region increases.

The current-voltage characteristics in Figure 1b include four regions, respectively, between points 0 and V_α, V_α and V_β, V_β and V_γ, and V_γ and ∞. The NDR region is located between points V_β and V_γ.

Let's look at the general principle of the circuit operation. When voltage V_{xy} varies from 0 to V_α, all transistors in the circuit are OFF. At the supply voltage V_α, all transistors are turning ON, and, up to the voltage V_β, the current I_1 rises, and the total current I_0 also increases. The current I_2 is a mirrored copy of I_1, and it behaves like I_1.When the supply voltage is V_β, the current I_1 reaches a maximum, which also corresponds to the maximum of the total current I_0. When the voltage V_{xy} changes from V_β to V_γ, the current I_1 decreases due to an increase in the negative voltage between the gate and the source of the transistor Q_0. At the same time, an increase in current I_b does not cover this decrease in current I_1. As a result, the total current I_0 decreases up to the voltage V_γ, at which the voltage between the gate and the source of the transistor Q_0 reaches a pinch-off voltage and Q_0 is turning OFF, and, consequently, the transistors $\overline{Q_1, Q_n}$ also turning OFF. When the supply voltage is higher than V_γ, the total current I_0 is entirely determined by the voltage V_{xy} and the resistances of R_a and R_b. Therefore, in the interval (V_γ, ∞) differential resistance of the current-voltage characteristics is positive.

Let us determine the coordinates of points α, β, and γ. In the first region of the current-voltage characteristics, between points 0 and V_α, all transistors are OFF, and the overall current depends on the resistor values R_a and R_b, and power supply voltage V_{xy}.

$$I_0 = \frac{V_{xy}}{R_a + R_b}. \tag{1}$$

The threshold voltage V_α is determined by applying Kirchhoff's voltage law (KVL) equation to the circuit of Figure 1a when transistor Q_0 is turning ON and $V_{DS0} = 0$, where V_{DS0} is the drain-source voltage of Q_0.

$$V_\alpha = V_{EB} + I_a R_a, \tag{2}$$

where V_{EB} is the emitter-base voltage of transistors $(\overline{Q_1, Q_n})$ and I_a is the current through resistor R_a. Since at voltage V_α the current I_a is equal to I_0, then Equation (2) transforms to the following form:

$$V_\alpha = \frac{V_{EB}(R_a + R_b)}{R_b}. \tag{3}$$

Combining (1) and (3), we obtain:

$$I_\alpha = \frac{V_{EB}}{R_b}. \tag{4}$$

When voltage V_{xy} a little exceeds V_α transistors $\overline{Q_1, Q_n}$ are turning ON, and transistor Q_0 starts to operate in the triode region where:

$$V_{DS0} < V_{GS0} + V_{P0}, \tag{5}$$

where V_{GS0} and V_{P0} are, respectively, the gate-source and pinch-off voltage of Q_0.

By applying KVL from $+V_{xy}$ to ground, we get:

$$V_{xy} = V_{EB} + V_{DS0} + I_a R_a. \tag{6}$$

From (6) we find current I_a as follows:

$$I_a = \frac{V_{xy} - V_{EB} - V_{DS0}}{R_a} \tag{7}$$

As it follows from the circuit of Figure 1a:

$$I_b = I_a - I_1. \tag{8}$$

Substituting (7) to (8) gives:

$$I_b = \frac{V_{xy} - V_{EB} - V_{DS0}}{R_a} - I_1. \tag{9}$$

Applying KVL around the loop $(R_b,\ Q_0,\ Q_1)$, we obtain:

$$-I_b R_b + V_{DS0} + V_{EB} = 0. \tag{10}$$

Substituting (9) into (10) and performing some mathematical transformations, we get:

$$V_{DS0} = \frac{R_b V_{xy}}{R_a + R_b} - I_1(R_a \| R_b) - V_{EB}. \tag{11}$$

The gate-source voltage of transistor Q_0 is given by:

$$V_{GS0} = -I_a R_a. \tag{12}$$

Voltage V_{GS0} we obtain by combining (7), (11), and (12) and performing necessary transformations.

$$V_{GS0} = -\frac{R_a V_{xy}}{R_a + R_b} - I_1(R_a \| R_b). \tag{13}$$

Substituting V_{DS0} from (11) to (7), we determine that:

$$I_a = \frac{V_{xy}}{R_a + R_b} + \frac{I_1 R_b}{R_a + R_b}. \tag{14}$$

We find the current I_0 by applying Kirchhoff's current law (KCL) to the node y in the circuit of Figure 1a.

$$I_0 = I_a + (n-1)I_2. \tag{15}$$

By substitution of (14) into (15), we obtain general equation for the circuit total current.

$$I_0 = (n-1)I_2 + \frac{I_1 R_b}{R_a + R_b} + \frac{V_{xy}}{R_a + R_b}. \tag{16}$$

Since the current I_2 is close to the reference current I_1, we can assume that $I_2 \approx I_1$. In this case Equation (16) transforms into the following form:

$$I_0 \approx I_1\left(n - 1 + \frac{R_b}{R_a + R_b}\right) + \frac{V_{xy}}{R_a + R_b}. \tag{17}$$

The slope of the current-voltage characteristics in the region of negative resistance is determined by the first derivative of the current I_0 with respect to the voltage V_{xy}.

$$\frac{dI_0}{dV_{xy}} \approx \left(n - 1 + \frac{R_b}{R_a + R_b}\right)\frac{dI_1}{dV_{xy}} + \frac{1}{R_a + R_b}. \tag{18}$$

As can be seen from (18), the slope is indeed proportional to the number of outputs of the current-mirror n. Therefore, by changing n, it is possible to reduce or increase the slope of the current-voltage characteristics between the voltage thresholds V_β and V_γ.

Substituting (11) and (13) into (5), we find that when transistor Q_0 operates in the triode mode, the following relationship holds between the supply voltage V_{xy} and the voltages V_{EB} and V_{P0}:

$$V_{xy} < V_{EB} - V_{P0}. \tag{19}$$

When voltage V_{xy} increases more, FET Q_0 reaches the saturation region where:

$$V_{DS0} \geq V_{GS0} + V_{P0}. \tag{20}$$

The threshold voltage V_β is reached at the boundary between the triode and the saturation region of transistor Q_0, i.e., when:

$$V_{DS0} = V_{GS0} + V_{P0}. \tag{21}$$

Substituting (11) and (13) into (21), we obtain the threshold voltage V_β.

$$V_\beta = V_{EB} - V_{P0}. \tag{22}$$

We determine the threshold current I_β by substitution of (22) into (17).

$$I_\beta \approx I_1\left(n - 1 + \frac{R_b}{R_a + R_b}\right) + \frac{V_{EB} - V_{P0}}{R_a + R_b}. \tag{23}$$

As can be seen in Figure 1b, the slope of the current-voltage characteristics in the regions $(0,\ V_\alpha)$ and $(V_\gamma,\ \infty)$ is the same. It means that at the voltage threshold V_γ the FET Q_0 is OFF and $I_1 = 0$. Transistor Q_0 is turning OFF when $V_{GS0} = V_{P0}$. Substituting V_{P0} instead of V_{GS0} into (13) and solving the obtained equation with respect to V_{xy}, we get:

$$V_{xy} = V_\gamma = -\left(1 + \frac{R_b}{R_a}\right)V_{P0}. \tag{24}$$

The threshold current I_γ we find by substituting V_{xy} from (24) into (1).

$$I_\gamma = \frac{|V_{P0}|}{R_a}. \tag{25}$$

As can be seen from (11), (13), (14), (16), (17), and (23), to calculate the currents and voltages related to the thresholds of the circuit current-voltage characteristics, it is necessary to know the current I_1. Modeling the current I_1 depends on the type of FET Q_0. Transistor Q_0 can be an N-channel JFET, metal-semiconductor field-effect transistor (MESFET), high-electron-mobility transistor (HEMT), or pseudomorphic high-electron-mobility transistor (PHEMT). In the voltage region (V_β, V_γ) transistor Q_0 operates in the saturation mode. Therefore, we should model the current I_1 for the case when Q_0 operates in the saturation mode.

As is well known, the operation of a JFET in the saturation mode is quite good described by the Shockley equation [23].

Substituting V_{GS0} from (13) to the Shockley equation gives:

$$I_1 = I_{DSS}\left(1 + \frac{AV_{xy} + BI_1}{V_{P0}}\right)^2, \tag{26}$$

where I_{DSS} is the saturation drain-source current at zero gate–source voltage, A and B are determined as follows:

$$A = R_a/(R_a + R_b), B = R_a \| R_b.$$

Solving (26) with respect to current I_1, we obtain the following quadratic equation:

$$\frac{I_{DSS}B^2}{V_{P0}^2} I_1^2 + \left[2I_{DSS}\left(1 + \frac{AV_{xy}}{V_{P0}}\right)\frac{B}{V_{P0}} - 1\right] I_1 + I_{DSS}\left(1 + \frac{AV_{xy}}{V_{P0}}\right)^2 = 0. \tag{27}$$

Equation (27) has two positive roots. The acceptable root is the value of the current I_1 that is less than I_{DSS}.

Figure 2a shows the dependence of the drain current I_1 versus power supply voltage V_{xy} in the interval (V_β, V_γ) when BF245B is used as a JFET Q_0 and Positive-Negative-Positive (PNP) BJT transistors BFT92W are used in the CM. Assume that $R_a = 0.5$ kΩ, $R_b = 2$ kΩ, and $n = 5$, i.e., the CM has four outputs. From the simulation program with integrated circuit emphasis (SPICE) model of the selected JFET transistor follows that $V_{P0} = -2.31$ V and $I_{DSS} = 6$ mA.

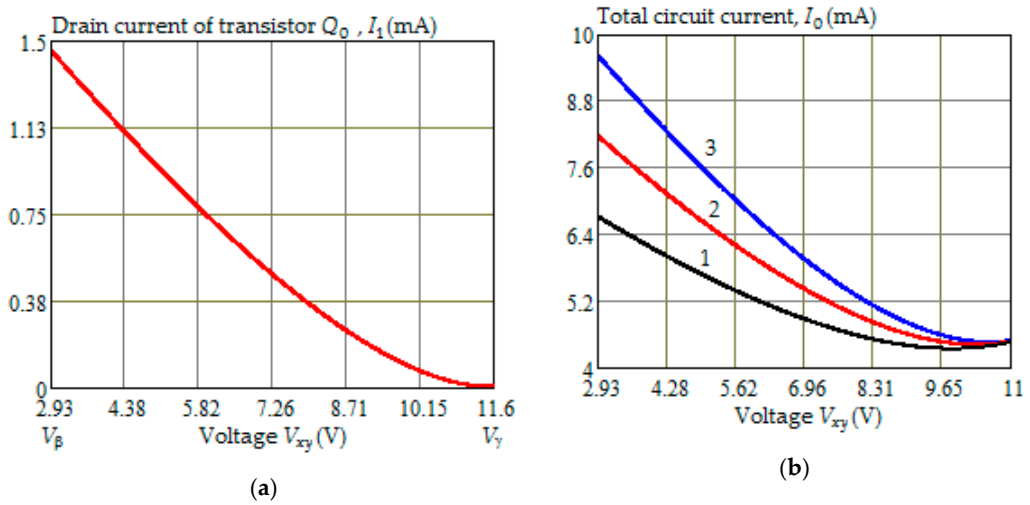


Figure 2. (**a**) Dependence of the drain current I_1 versus voltage V_{xy}; (**b**) Dependence of the total current I_0 versus voltage V_{xy} in the negative differential resistance region when $n = 4$ (curve 1), $n = 5$ (curve 2), and $n = 6$ (curve 3).

As can be seen in Figure 2a, in the NDR region the current I_1 changes from 1.47 mA to 0. Figure 2b shows the dependence of the total current I_0 versus voltage V_{xy} in the NDR region when $n = 4$ (curve 1), $n = 5$ (curve 2), and $n = 6$ (curve 3).

The curves in Figure 2b were calculated using (17) and (27). As can be seen in Figure 2b, the total current I_0 increases by the same value with each increase in the number of the CM outputs. At the same time, the threshold voltage V_γ shifts slightly to the right with increasing n.

Let us compare the calculated and simulated voltage and current thresholds for the circuit of Figure 1a for the same data as in Figure 2. From the interactive SPICE simulation of transistor BFT92W operation with the help of Multisim (ed. 14.1) follows that $V_{EB} = 0.52$ V (at threshold α) and $V_{EB} = 0.62$ V (at threshold β). The results of calculations and SPICE simulations are shown in Table 1.

Table 1. Calculated and simulated threshold voltages and currents with junction gate field-effect transistor (JFET).

Threshold	Calculated Value	Simulated Value	Error %
V_α (V)	0.65	0.62	−4.8%
I_α (mA)	0.26	0.28	7.1%
V_β (V)	2.93	2.89	−1.4%
I_β (mA)	8.22	8.30	1%
V_γ (V)	11.60	11.05	−5.0%
I_γ (mA)	4.62	4.50	−2.7%

As can be seen in Table 1, the absolute relative error for the calculated voltage thresholds of the NDR region does not exceed 5% and for current thresholds slightly exceed 2.5%. Such a high accuracy of calculating voltage and current thresholds testifies on the adequacy of the derived mathematical equations.

Let us now consider the case when Q_0 is a GaAs transistor, i.e., MESFET, HEMT, or PHEMT. We model the current of Q_0 by the Statz nonlinear model, which has a high accuracy in the approximation of the drain current [24].

Substituting V_{DS0} and V_{GS0} from (11) and (13) to the Statz model [24,25], we get the following nonlinear equations in respect to the drain current I_1:

$$\frac{\delta\left(AV_{xy}+BI_1+V_{P0}\right)^2}{1-\Delta\left(AV_{xy}+BI_1+V_{P0}\right)}\left[1+\lambda\left(CV_{xy}-BI_1-V_{EB}\right)\right]\left\{1-\left[1-\alpha\left(CV_{xy}-BI_1-V_{EB}\right)/3\right]^3\right\}-I_1=0,$$
$$\text{for } 0 < CV_{xy}-BI_1-V_{EB} < 3/\alpha, \tag{28}$$

$$\frac{\delta\left(AV_{xy}+BI_1+V_{P0}\right)^2}{1-\Delta\left(AV_{xy}+BI_1+V_{P0}\right)}\left[1+\lambda\left(CV_{xy}-BI_1-V_{EB}\right)\right]-I_1=0, \text{ for } CV_{xy}-BI_1-V_{EB} \geq 3/\alpha, \tag{29}$$

where α is the current saturation parameter, δ is the transistor transconductance, Δ is the doping profile parameter, λ is the channel length modulation coefficient, and C is determined as follows:

$$C = R_b/(R_a + R_b).$$

Let us again compare the calculated and simulated voltage and current thresholds for the circuit of Figure 1a when a low noise PHEMT ATF-33143 is used as transistor Q_0 and the same PNP transistors BFT92W are used in the CM. From the SPICE model of ATF-33143 [26] follows that $\alpha = 4$ [1/V], $\delta = 0.48$ $\left[\text{A/V}^2\right]$, $\Delta = 0.8$, $\lambda = 0.09$ [1/V], and $V_{P0} = -0.95$ [V]. The other circuit parameters have the same values as in the previous example.

To obtain the calculated values of the voltage and current thresholds, we solve Equations (28) and (29) and use Equations (3), (4), and (22)–(25). The results of calculations and SPICE simulations with the help of Multisim (ed. 14.1) are shown in Table 2.

Table 2. Calculated and simulated threshold voltages and currents with pseudomorphic high-electron-mobility transistor (PHEMT).

Threshold	Calculated Value	Simulated Value	Error %
V_α (V)	0.65	0.62	−4.8%
I_α (mA)	0.26	0.28	7.1%
V_β (V)	1.57	1.71	8.2%
I_β (mA)	7.18	6.92	−3.8%
V_γ (V)	4.75	4.73	−0.4%
I_γ (mA)	1.9	1.91	0.5%

As can be seen in Table 2, a good agreement exists between the theoretical and simulated values of the current and voltage thresholds, which proves the validity of the derived equations.

3. Circuit Applications

3.1. LC Oscillator

Oscillators are one of the main elements in modern communication, control, and navigation systems. Modern oscillators can be divided into two classes, namely oscillators with negative input impedance and oscillators with NDR. A distinctive feature of the first-class oscillators is the presence of a negative real part in the input impedance. Examples of such oscillators are numerous Colpitts, Clapp, Hartley oscillator circuits, and their modifications [27–30], as well as cross-coupled CMOS oscillators [31–34]. The second class of microwave oscillators supposes to use a tunnel diode or a Gunn diode [35,36], which have an NDR region in the N-type current-voltage characteristics. The location of the operating point in the NDR region leads to the creation of a negative resistance induced into the contour of the LC tank to compensate for its losses. The circuit of Figure 1a can also be used for designing an LC oscillator because it has an NDR region.

Figure 3 shows an LC oscillator on the base of the proposed NDR circuit. The oscillator tank circuit consists of an RF coil L and two series-connected capacitors C_1 and C_2. Small capacitor C_F is a feedback capacitor allowing to speed-up the oscillator start-up. Large capacitor C_0 reduces the noise level significantly at the nodes y, z, d, and s of the oscillator. This allows increasing the slope of the noise skirt around the fundamental harmonic, which in-turn reduces the oscillator phase noise.

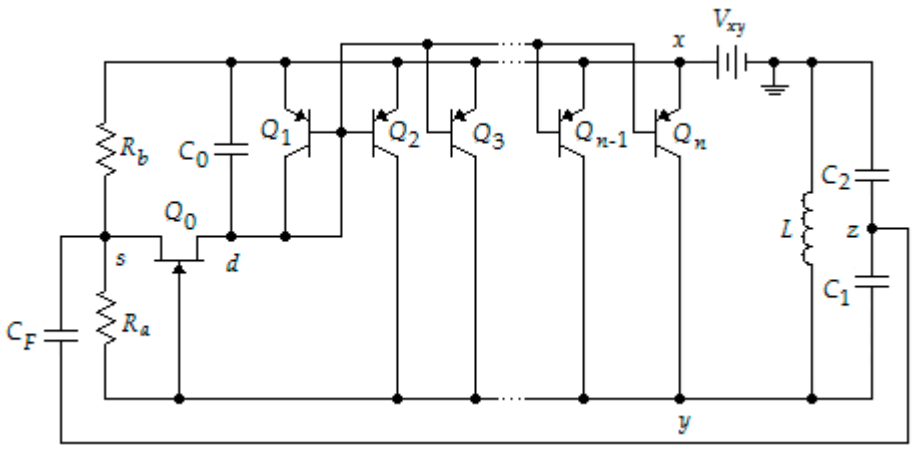


Figure 3. LC oscillator with NDR.

3.1.1. Simulation Results

Let us perform a SPICE simulation of the proposed oscillator circuit with the help of Multisim (ed. 14.1). Assume that $n = 3$, $R_a = 0.15$ kΩ, $R_b = 1$ kΩ, transistor Q_0 is a PHEMT ATF-33143, and all transistors in the CM are BFT92W. Figure 4 shows the simulated current-voltage characteristics. As can be seen in Figure 4, the NDR region has the following voltage and current thresholds: $V_\beta = 1.58$ V, $I_\beta = 15$ mA, $V_\gamma = 7.26$ V, and $I_\gamma = 6.33$ mA. We set the operating point at $\overline{V}_{xy} = 3.75$ V and $\overline{I}_0 = 12.5$ mA.

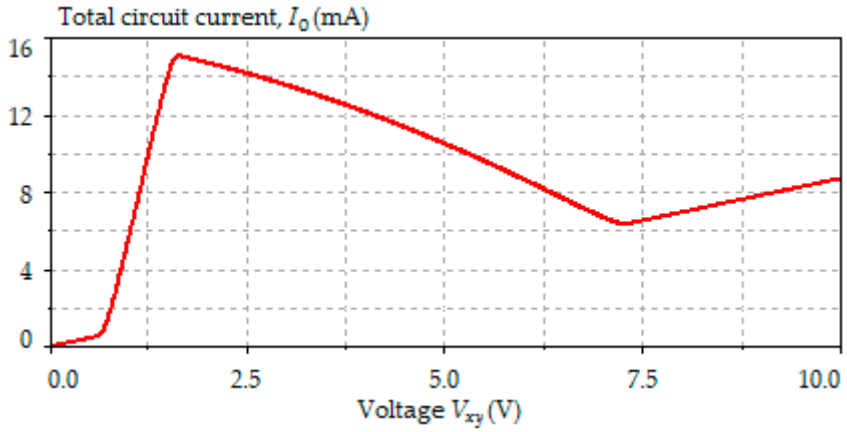


Figure 4. Oscillator current-voltage characteristics.

The selected circuit components have the following values: $L = 5$ nH, $C_0 = 10$ μF, and $C_1 = C_2 = 5$ pF. Figure 5 shows the oscillator starting voltage waveforms at the output node y for different values of the feedback capacitor C_F. The frequency of oscillations is 1.096 GHz. We can observe from Figure 5, that the oscillations reach the steady-state amplitude of 2.2 V at $t = 130$ ns and 2.4 V at $t = 55$ ns when $C_F = 5$ pF and $C_F = 10$ pF, respectively. Thus, an increase in the capacitance C_F leads to a significant reduction in the self-excitation time of the oscillator and an increase in the amplitude of the steady-state oscillations.

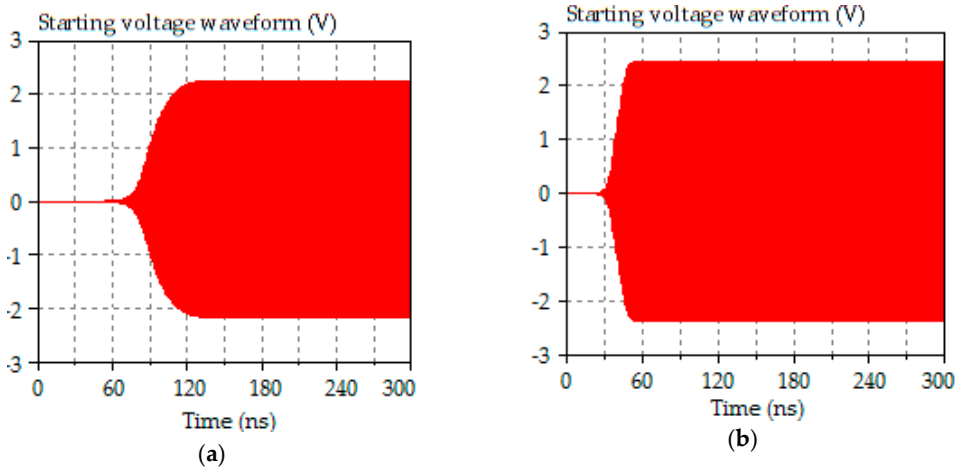


Figure 5. Oscillator start-up behavior at $C_F = 5$ pF (**a**) and $C_F = 10$ pF (**b**).

Figure 6 shows the amplitude spectrum of the oscillated voltage for $C_0 = 1$ nF and $C_F = 5$ pF (blue line) and $C_0 = 10$ μF and $C_F = 10$ pF (red line). As can be seen from comparison of two spectrums in Figure 6, the noise skirt of the fundamental harmonic at the level of -80 dBm is significantly narrower for larger values of capacitances C_0 and C_F. Moreover, the total harmonic distortion (THD) is 3.3% for

$C_0 = 10$ µF and $C_F = 10$ pF and 3.7% for $C_0 = 1$ nF and $C_F = 5$ pF, i.e., larger capacitances C_0 and C_F provide a smaller level of THD.

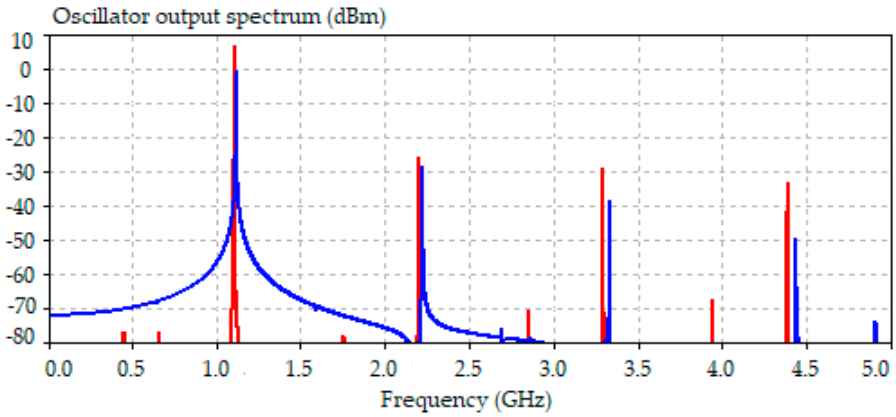


Figure 6. Oscillator output spectrum when $C_0 = 1$ nF and $C_F = 5$ pF (blue line) and $C_0 = 10$ µF and $C_F = 10$ pF (red line).

The decrease in the noise level of the oscillator output voltage in Figure 6 is explained by the fact that with an increase in the capacitances C_0 and C_F, the simulated spectral density of noise decreases significantly at the nodes y, z, d, and s of the oscillator circuit as shown in Figure 7. As can be seen in Figure 7c, the most substantial decrease in noise spectral density occurs at the drain of transistor Q_0, i.e., just where there is a large capacitance C_0. This observation confirms a similar conclusion concerning the effect of capacitance on noise in CMOS LC oscillators [37].

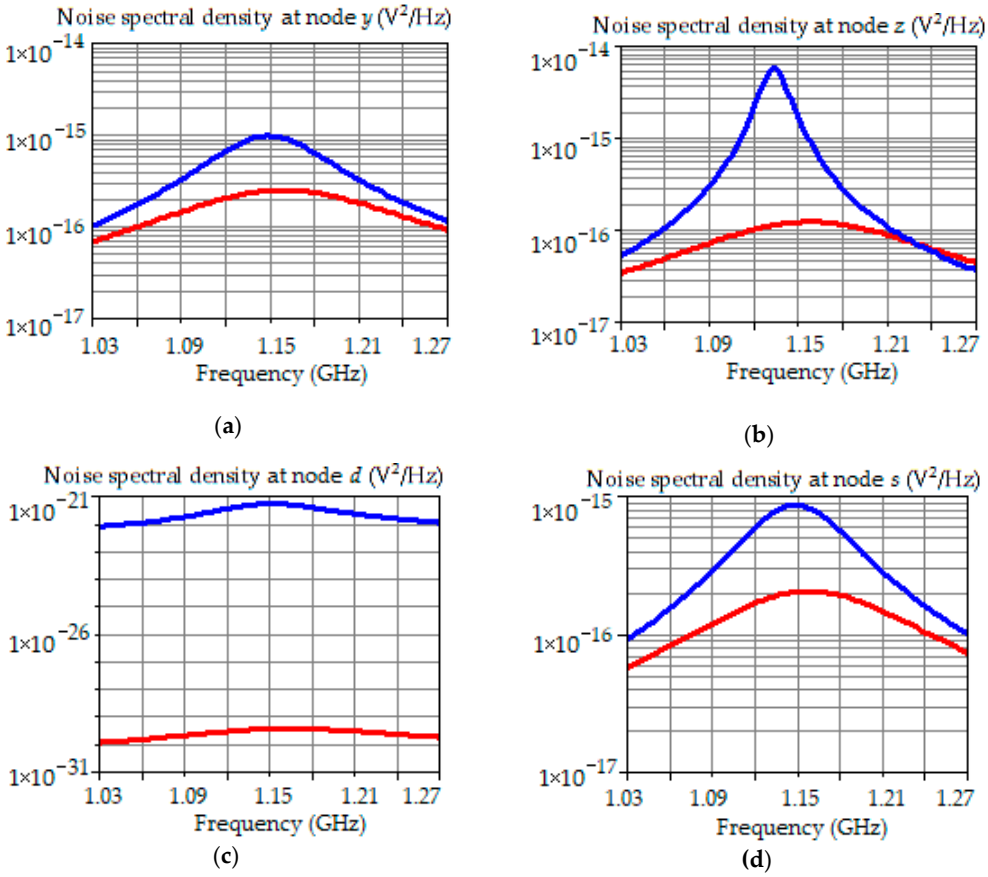


Figure 7. Noise spectral density at nodes y (**a**), z (**b**), d (**c**), and s (**d**) when $C_0 = 1$ nF and $C_F = 5$ pF (blue line) and $C_0 = 10$ µF and $C_F = 10$ pF (red line).

3.1.2. Oscillator Prototype Implementation

The oscillator circuit of Figure 3 was implemented using a JFET BF245B (NXP Semiconductors, Eindhoven, Netherlands) as transistor Q_0 and five transistors BFT92W (NXP Semiconductors, Eindhoven, Netherlands) in the CM, i.e., $n = 5$. We selected the following component values: $R_a = 0.5$ kΩ, $R_b = 2$ kΩ, $C_1 = C_2 = 82$ pF, $C_F = 2.2$ pF, $C_0 = 0$, and $L = 330$ nH.

Figure 8 shows the printed circuit board (PCB) assembly of the implemented NDR oscillator.

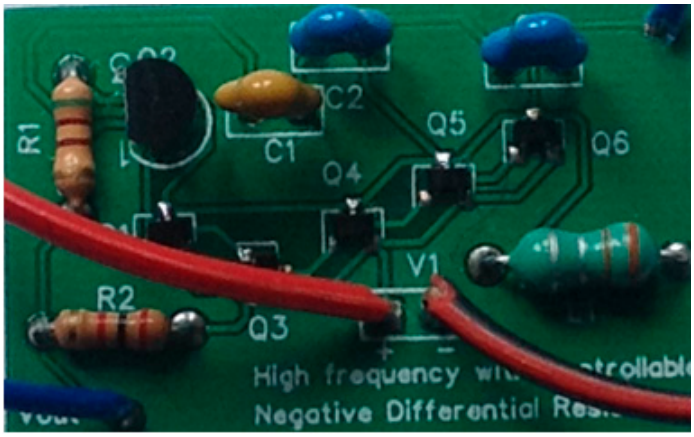


Figure 8. Photograph of the NDR oscillator printed circuit board assembly.

Figure 9 shows the measured current-voltage characteristics of the implemented NDR oscillator. The measured values of the threshold voltages in the NDR region are $V_\beta^* = 3$ V and $V_\gamma^* = 12$ V. The calculation of the theoretical voltage thresholds by Equations (22) and (24) gives $V_\beta = 2.93$ V and $V_\gamma = 11.55$ V. As can be seen, there is a perfect agreement between the measured and theoretical results. The dc operating point has the following coordinates: $\overline{V}_{xy} = 5.2$ V and $\overline{I}_0 = 7.6$ mA.

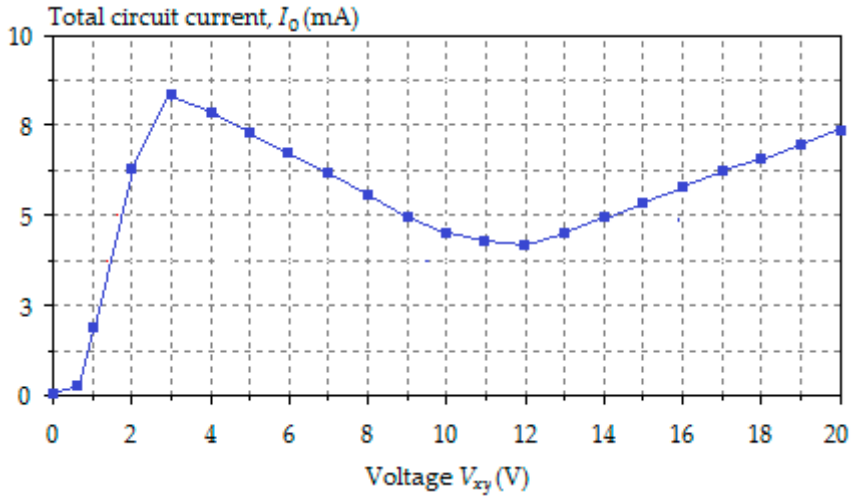
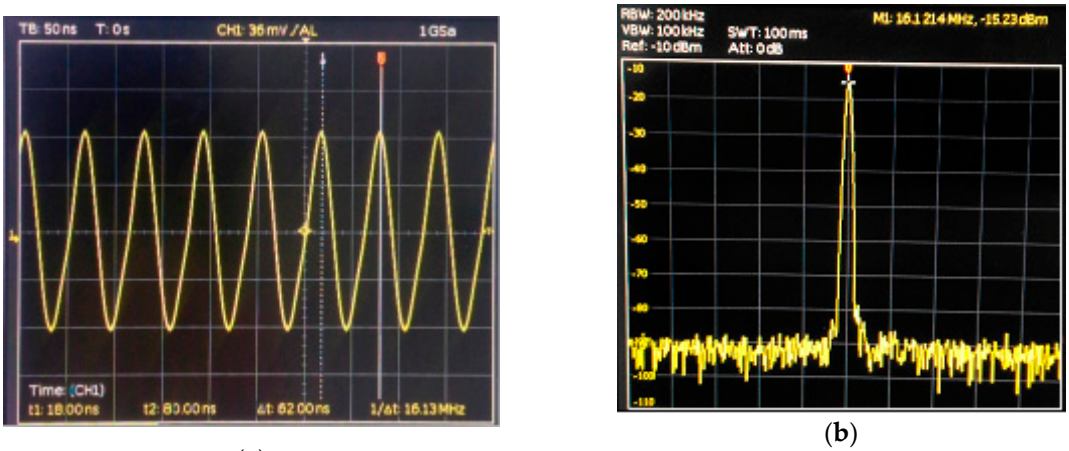


Figure 9. Measured current-voltage characteristics of the implemented NDR oscillator.

Figure 10 shows the photographs of the output voltage (a) and output power spectrum (b) of the implemented oscillator. We used the HMO1002 oscilloscope (Rohde & Swartz, Munich, Germany) and the HMS3000 spectrum analyzer (Rohde & Swartz, Munich, Germany) to measure the oscillator's output voltage in the time and frequency domain. To connect the oscillator output to oscilloscope and spectrum analyzer, we used, respectively, RF probes HZ154 (Rohde & Swartz, Munich, Germany) and P-20A (Auburn Technology Corporation, Wichita, Kansas, USA) with 20 dB attenuation. We can see from Figure 10 that the frequency and the peak-to-peak amplitude of oscillations are 16.1 MHz and

4.12 V, respectively. We can also observe in Figure 10b that the noise-floor power level is more than 75 dB below the fundamental harmonic power.



(**a**) (**b**)

Figure 10. (**a**) The oscillogram of the oscillator output voltage; (**b**) The measured spectrum of the oscillator output power with span of 20 MHz.

3.2. LC Voltage Controlled Oscillator

Voltage-controlled oscillators are fundamental building units in modern phase-locked loop synthesizers used in communication and navigation transceivers [38–40]. The NDR circuit of Figure 1a can also be used to design an LC VCO. Figure 11 shows the proposed LC VCO with a controllable slope of the NDR region. The varactor diodes VC_1 and VC_2 replace the capacitors C_1 and C_2 in the circuit of Figure 3. The control voltage V_c is applied to cathodes of varactor diodes VC_1 and VC_2 providing a frequency tuning of the VCO. Resistor R_c isolates the variable power supply from the VCO tank circuit.

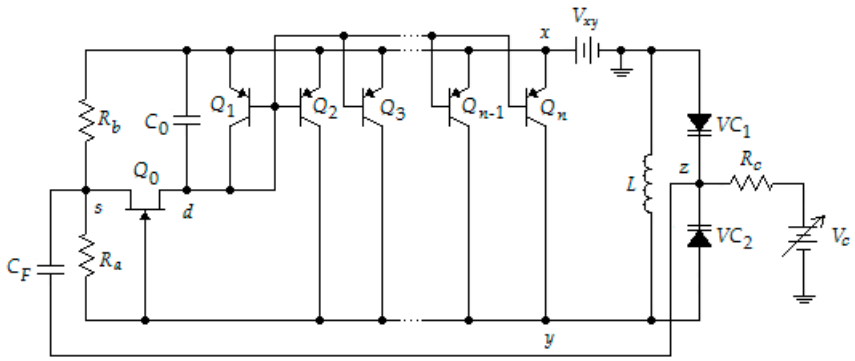


Figure 11. LC voltage-controlled oscillator with NDR.

The SPICE simulation of the VCO circuit with the help of Multisim (ed. 14.1) was conducted using varactor diodes ZC820 (Zetex) and the same transistors, inductor L, and resistors R_a and R_b as in Section 3.1.1. We set the VCO circuit elements C_0, C_F, and R_c to 10 µF, 10 pF and 10 kΩ, respectively. The control voltage V_c was varied from 1 to 25 V. Figures 12 and 13 show the VCO starting voltage waveform (a) and steady-state voltage waveform (b) when $V_c = 1$ V and $V_c = 25$ V, respectively. The oscillation frequency varied from 775 MHz (at $V_c = 1$ V) to 1.375 GHz (at $V_c = 25$ V). The THD is 4.6% at $V_c = 1$ V and 3.8% at $V_c = 25$ V.

From a comparison of voltage starting waveforms in Figures 12a and 13a, we can observe that voltage oscillations reach the steady-state mode at 160 ns and 80 ns, respectively. In the steady state operation mode, the voltage amplitude is around 2 V over the entire control voltage range.

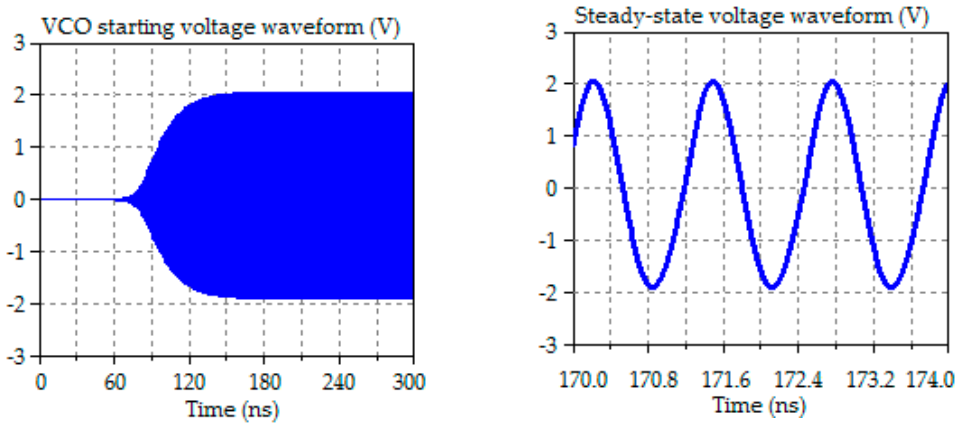


Figure 12. (**a**) Voltage-controlled oscillators (VCO) starting voltage waveform when $V_c = 1$ V; (**b**) VCO steady-state voltage when $V_c = 1$ V.

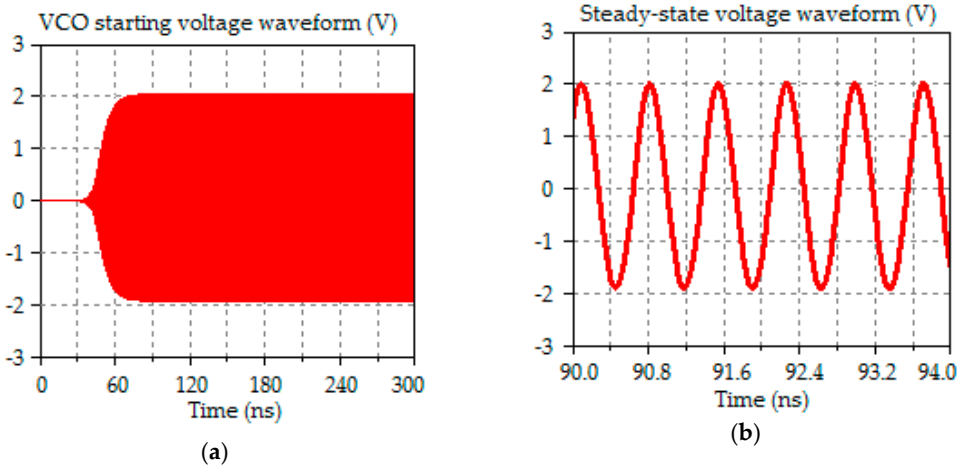


Figure 13. (**a**) VCO starting voltage waveform when $V_c = 25$ V; (**b**) VCO steady-state voltage when $V_c = 25$ V.

Figure 14 shows the tuning characteristic of the VCO. As can be seen in Figure 14, the simulated VCO covers a wide frequency range. The ratio of the maximum VCO frequency to minimum exceeds 1.75.

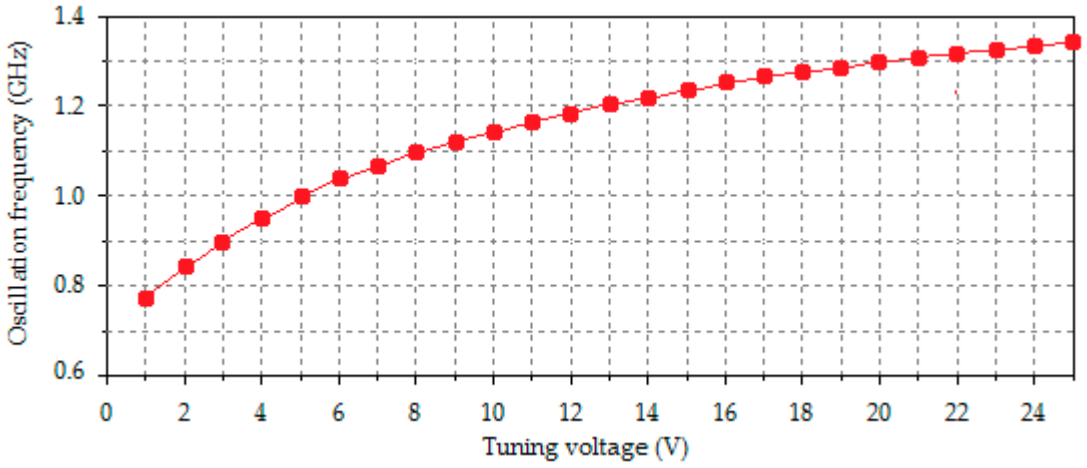


Figure 14. VCO tuning characteristic.

LC Voltage-Controlled Oscillator Performance

Let us compare the overall performance of the proposed NDR VCO with state of the art VCOs. The conventional FOM is used to evaluate the overall performance of the designed VCO, which includes phase noise at a particular frequency offset from the carrier $PN(\Delta f)$, power dissipation P_d, and the ratio of the carrier frequency f_c to the frequency offset Δf for comparing VCOs operating at different frequencies [41,42].

$$FOM = PN(\Delta f) - 20\log\left(\frac{f_c}{\Delta f}\right) + 10\log\left(\frac{P_d}{1\text{ mW}}\right). \quad (30)$$

Table 3 presents the part numbers of the VCO elements. In the simulation, we used the VCO circuit of Figure 11 when $n = 2$. The simulated values of the NDR threshold voltages are as follows: $V_\beta = 2.84$ V and $V_\gamma = 20.7$ V. The calculated thresholds are $V_\beta = 2.84$ V and $V_\gamma = 20.7$ V. The selected DC operating point has the following coordinates: $\overline{V}_{xy} = 6.5$ V and $\overline{I}_0 = 8.5$ mA. Thus, the VCO power dissipation is 55.25 mW. The control voltage V_c applied to the cathodes of the SMV1104-34 varactors varied from 2 V to 6 V. The frequency tuning range is from 1.225 GHz to 1.620 GHz. Figure 15 shows the dependence of the VCO phase noise versus Δf when $V_c = 2$ V. As can be seen in Figure 15, the use of large C_0 reduces phase noise for more than 20 dB in all range of offset frequencies. The low level of the phase noise is also due to the use of a high-Q coil L [43]. In the tuning VCO range, the inductor quality factor is varied from 50 to 60.

Table 3. Part numbers used in the designed voltage-controlled oscillator.

Circuit Elements	Part Numbers
Transistor Q_0	NE722S01
Transistors $\overline{Q_1, Q_n}$	MRF5211LT1
Inductor L	0201DS-3N3XJEU
Capacitor C_0	C1608X5R1E105K
Capacitor C_F	C0603C0G1E030C
Varactors	SMV1104-34
Resistor R_a	ERJ1GEJ471
Resistor R_b	ERJ2GEJ392

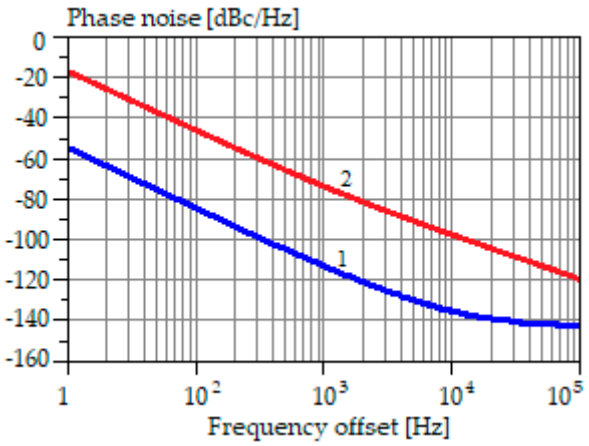


Figure 15. Phase noise versus offset frequency when $C_0 = 1$ μF (curve 1) and $C_0 = 1$ nF (curve 2).

Table 4 shows a comparison of the designed VCO with the VCOs in recently published studies in terms of the FOM (30). As can be seen in Table 4, the designed NDR VCO has one of the best FOM.

It should be noted that all previously published VCOs in Table 4, except [58,59], fabricated in CMOS or BiCMOS technologies.

Table 4. Performance of designed VCO and some recently published VCOs.

VCO	Frequency GHz	Frequency Offset MHz	Phase Noise dBc/Hz	Power Dissipation mW	FOM dBc/Hz
[44]	1.61	0.1	−121	2.7	−202
[45]	2.5	1	−119.7	0.515	−190.3
[46]	11.58	1	−112.62	6	−198.6
[47]	8	1	−134.3	6.6	−204
[48]	2.7	0.1	−121.3	3.9	−204
[49]	3.6	1	−124	2.05	−192
[50]	15.57	1	−116.6	6	−192.7
[51]	2.4	1	−120	0.267	−193.3
[52]	2.4	1	−135.6	6.17	−195.3
[53]	12.67	1	−120.6	17.7	−190
[54]	1.94	1	−153	20	−205.7
[55]	2.38	3	−132.7	1	−190.7
[56]	2.4	1	−124	2.86	−187.25
[57]	7	1	−132	198	−185.9
[58]	7.9	1	−135	1456	−181.3
This work	1.225	0.1	−141.1	55.25	−205.4

Oscillators manufactured using MESFET, HEMT, and PHEMT have significantly lower FOM values due to substantially higher power consumption [58,59]. However, as follows from Table 4, the proposed NDR VCO can even compete with the best CMOS oscillators due to the low level of phase noise and despite the significantly higher power consumption.

4. Discussion and Conclusions

There is a large number of electronic circuits [1–22], in which the current-voltage characteristics have an NDR region. The basis of these circuits is formed by various combinations of BJT and FET. Conventionally, the circuits with NDR can be classified into the following groups: circuits with MOS transistors [7,8,16–18,21], circuits with BJT transistors [10,14], circuits with BJT and JFET [11–15], circuits with JFET and MOS transistors [12,22], circuits with BJT and MOS transistors [9,20], and circuits with BJT and HBT [19]. It should be noted that in the known NDR devices and circuits it is practically impossible to change the angle of inclination of the current-voltage characteristics in the area of negative resistance. Therefore, it is not possible to increase the NDR of the device or circuit without changing the type or the size of the transistors.

This paper proposes a new NDR circuit based on the connection of a FET and a BJT simple current mirror with multiple outputs. A JFET, MESFET, HEMT, or PHEMT can be used as a FET. A distinctive feature of this circuit is the ability to control the NDR without changing the types or the size of transistors. This feature is based on the property of a simple current mirror to increase the current gain due to the parallel connection of transistors at the output of the mirror [59]. In the proposed circuit, the current-voltage characteristics are of the N-type with three threshold voltages. General mathematical equations for calculating the threshold voltages and currents have been derived. Since the threshold current related to the beginning of the NDR region depends on the FET drain current, a mathematical modeling of this current has been performed for a JFET and a gallium-arsenide FET, such as MESFET,

HEMT, or PHEMT. A comparison of the calculated voltage and current thresholds with the SPICE simulations showed perfect convergence as for the case of using a JFET as well as for PHEMT, which was modeled by the Statz nonlinear model. The latter indicates the adequacy of mathematical expressions derived for the calculation of current and voltage thresholds.

The proposed NDR circuit can be used to design various oscillators. By connecting a parallel LC tank to the output of the proposed NDR circuit, one can get a sinusoidal oscillator, which can operate in different frequency bands. When using an ultra-high frequency JFET, the maximum frequency is limited to several hundred MHz. When using a gallium-arsenide transistor such as MESFET, HEMT, or PHEMT, the maximum oscillation frequency lies in the region of several GHz. Self-excitation of the oscillator by the proposed NDR circuit depends on the magnitude of the negative resistance introduced into the parallel LC tank circuit. If the value of the introduced negative resistance is sufficient to compensate for losses in the tank circuit, then the amplitude of oscillations increases and reaches a steady-state value. However, if the magnitude of the introduced negative resistance is insufficient, the oscillator does not self-excite. In any other NDR oscillator, in this case, it is necessary to change the transistors or their sizes for increasing negative resistance. However, in the proposed NDR circuit, it is enough to add one or more transistors in the current mirror as shown in Figure 1a and in this case, according to formula (18), the NDR will increase, and hence the absolute value of the negative resistance introduced into the tank circuit will also increase. Then the oscillator will oscillate. A SPICE simulation of the LC oscillator with a PHEMT and a BJT current-mirror at the frequency of 1.096 GHz showed that the generated signal has a low level of distortion, as well as a low noise level when using additional capacitances in the positive feedback circuit and between the drain of the PHEMT and ground. The implemented LC oscillator prototype operating in the high-frequency band has confirmed theoretical results. The proposed NDR circuit can also be used to design a VCO. Depending on the transistors used, such VCO can operate in different frequency bands, ranging from high-frequencies and up to microwaves. Thus, the simulated VCO circuit with PHEMT covers the frequency range from 775 MHz to 1.375 GHz, i.e., the frequency overlap ratio is higher than 1.75. Moreover, the amplitude of oscillation is about 2 V and practically does not change in the whole range of tunable frequencies. A comparison of the performance characteristics of the designed VCO with VCOs in previously published studies has shown that it is about 20 dB more efficient than the HEMT VCOs and is not inferior to the best CMOS VCOs.

The proposed NDR circuit can also be used in laboratory works in the electronics departments of universities to study the properties of negative resistance, to model various oscillators and to analyze the conditions for self-excitation of oscillators.

Our future work will include an analysis of the use of various bipolar and MOS current mirrors instead of the simple current mirror in the proposed NDR circuit.

Author Contributions: This article presents the collective work of all authors. The first two authors (V.U. and A.R.) jointly participated in the conceptualization of the problem, development of mathematical models, simulation of the developed circuits, numerical calculations, and writing the article. The third author (H.O.) developed a printed circuit board of the oscillator prototype, soldered electronic components, and made the necessary measurements.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations exist in the manuscript:

BJT	Bipolar junction transistor
CM	Current mirror
CMOS	Complementary metal-oxide-semiconductor
FET	Field-effect transistor
FOM	Figure of merit
HBT	Heterojunction bipolar transistor
HEMT	High-electron-mobility transistor
JFET	Junction gate field-effect transistor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
MESFET	Metal-semiconductor field-effect transistor
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NDR	Negative differential resistance
NENS	N-channel enhancement mode with load operated at saturation
PCB	Printed circuit board
PHEMT	Pseudomorphic high-electron-mobility transistor
PNP	Positive-negative-positive
RF	Radio frequency
SPICE	Simulation program with integrated circuit emphasis
THD	Total harmonic distortion
VCO	Voltage controlled oscillator

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