A Simplified Methodology to Evaluate Circuit Complexity: Doherty Power Amplifier as a Case Study

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Abstract: This paper analyzes the circuit complexity using Doherty power amplifier (DPA) as a case study and proposes a simplistic model to characterize the design complexity of a DPA circuit. Various fundamental building blocks of the DPA circuit are discussed and modeled to formulate the model. In one of our experiments, it is observed that a reduction of up to 400% in the normalized complexity factor (NCF) could enhance the gain performance by approximately up to 40% for UHF applications. This work can be used as a common benchmarking tool to compare various types of DPA architecture and allow design teams to optimize their building blocks in the DPA circuit. This model can also potentially become a platform for the improvement of many integrated circuit design components, allowing ready integration on a wide range of next generation applications, not only limited to DPA circuits.

Keywords: complexity analysis; silicon CMOS; wireless communications; amplifier

1. Introduction

Optimizing circuit trade-offs is a highly challenging task for any design team. This challenge is further exacerbated with the additional design complexity of integrating multiple circuits. Today, with the increasing demand for newer wireless communication products, design teams face a shorter time-to-market (TTM) for every generation of their new products and each product requires major improvement in wireless capability. Hence, it is important for the design teams to have good evaluation benchmarking tools so that they can quickly evaluate the efforts of adopting a new circuit technique.

Any circuit design is largely divided into well-studied circuit technique and emerging circuit technique. For example, in a DPA circuit [1], there are some of the emerging circuit techniques introduced in the recent years, such as harmonic matching, inverted DPA, impedance combining and addition of offset lines. The new circuit techniques do come with design trade-offs, such as degradation of RF circuits from effects such as hot carrier injection (HCI), oxide breakdown (OBD) [2], and electromigration (EM) [3]. Before any design team decides to incorporate new techniques into their existing circuit, it is also important to understand the complexity for these techniques because the integration of new techniques requires an additional effort to integrate and optimize with their existing design. It may be well-known to keep the complexity of circuits as low as possible but in the pursuit of enhancing performance of circuits, it is often overlooked.

It has been observed that if circuit enhancement techniques are implemented at the expense of increased complexity, the circuit performance improvement could be marginal and it would result in a diminishing return for an investment of time into the optimization. For example, X. Fang et al. [4] employed 33 matching network (M/N) elements to achieve a P_{sat} of 42 dBm, power added efficiency (PAE) of 50.3% and a gain of 11 dB at around 2 GHz. However, C. H. Kim et al. [5] achieved slightly higher overall performance based on only 16 M/N elements with both of them utilizing GaN technology. As such, there is a need to analyze the complexity of circuits to benchmark against published designs so that it can be decided whether to continue with the work or to adopt the published design for a targeted parameter to enhance. An extensive overview of the different solutions to enhancing DPA has been presented by Vittorio et al. [6]. This paper aims to provide an alternative view from the perspective of complexity but not the details of the DPA designs such as the performance of the passive components or the area of the inductors for example. Complexity factor (CF), which is a function of the number of parameters of the individual blocks of circuits as a figure of merit is proposed. With this exemplary model, designers will be able to extend this concept, quantify a metric and evaluate before committing to any circuit design.

The outline of this paper is defined as follows. Section 2 introduces the architecture of conventional two and three-way DPA designs for understanding the formulation of CF. Section 3 introduces the proposed CF and its theoretical analysis. The discussion in Section 4 explored the relationship of CF with gain of DPA as an example and compared state-of-the-art DPAs as an illustration and last but not least, the conclusion in Section 5.

2. Complexity Analysis Using DPA

The complexity of circuits affects the design time and consequently the TTM for products. The CF of a DPA architecture is demonstrated and analyzed by studying the number of S-parameters of the power divider and power amplifiers which are the transistors shown in Figures 1 and 2, and the number of parameters of the M/N. The number of parameters for the M/N are the key parameters in these analyses and some of these blocks can be characterized through S-parameter models. The proposed CF is a function of complexity numbers of the individual blocks defined as

$$CF = f(C_{PD}, C_{PA}, C_{M/N}) \quad (1)$$

C_{PD} is the complexity number for the power divider

C_{PA} is the complexity number for the power amplifier

$C_{M/N}$ is the complexity number for the matching network.

Figure 1. Complexity paths for two-way DPA. The main and auxiliary paths are in parallel.

Figure 2. Complexity paths for three-way DPA. The main and two auxiliary paths are in parallel.

As shown in Figures 1 and 2, C_M and C_A are the aggregate complexity numbers for the paths of the main or carrier PA and auxiliary PA respectively. The fundamental building blocks for DPA are the power divider, the carrier and auxiliary PA branches, and the output quarter-wavelength line from the carrier to the auxiliary branches which can also be considered as the power combiner. The quarter-wavelength and delay lines are represented by Φ and δ respectively. These blocks can be designed to terminate with $50\ \Omega$ ports but co-designing some of them can reduce circuit complexity and improve performance such as PAE [7].

This could be done by tuning the variables with computer aided design (CAD) tools. The paths for analyses are shown with the individual branches in series while the power divider is a parallel block. The following sections briefly introduce the individual blocks and the simplified models used for the complexity analysis.

3. Proposed Complexity Factor For DPA

For a design with higher complexity, a deduction can be made that the optimization time will be longer whether done manually or by an optimization software. Consider a two-way conventional DPA, it is observed that it could be broken down into three sub-blocks which are the power divider, the main and auxiliary PA branches. As the power divider and the PAs can be designed as standalones before the integration, complexities with their S-Parameters can be quantified. For a two-way DPA, two output and one input ports are utilized for the power divider. Extending to a three-way DPA, three output and one input ports will be used. A conventional two-port PA would have four S-parameters and an equation can be derived to extend to multi-port PA (MPA). Therefore, the complexity numbers for the power divider and PA are

$$C_{PD} = (n + 1)^2 \quad (2)$$

$$C_{PA} = (n^2)^\gamma \quad (3)$$

where n is the number of ports in use for the power divider and the PAs in (2) and (3) respectively and γ is the number of stages of PA cascaded in the branch. For a conventional T-line, two parameters which are the width and length, can be optimized for the required impedance and phase shift. A discrete passive element would have only its inductance or capacitance. The complexity numbers of input and

output matching networks and delay lines shown in (4) and (5) respectively for a path can thus be represented by

$$C_{M/N,i/o} = (2n_{tl} + n_{de}) \quad (4)$$

$$C_{\sigma} = \alpha\sigma \quad (5)$$

$\alpha = 2$ for T-line model

$\alpha = 3$ for discrete model

where σ is the number of delay lines and phase shifters, n_{tl} is the number of T-line elements and n_{de} is the number of discrete elements in the matching circuit blocks. For the main and auxiliary branches, where the number of auxiliary branches can be increased up till the $(n-1)^{th}$ branch depending on design and application, the complexity number for each of the branch can be represented by a product of the building blocks' complexity numbers as calculated by

$$C_{M,A} = C_{PA}C_{M/N,i}C_{M/N,o}C_{\sigma} \quad (6)$$

For a given N-way DPA, the complexity numbers of the individual parallel branches are summed up and then multiplied by the complexity number of the power divider in series. As the 50 Ω impedance transformer is common for most DPA designs, it was excluded from the formulation. If a DPA is designed in a way that allows it to omit the impedance transformer at the output, the equation would still apply. The CF of an N-way DPA is then formulated to be

$$CF = C_{PD} \left(\alpha^{n-2} C_M + \sum_{i=2}^n \alpha^{n-i} C_{Ai-1} \right), n \geq 2 \quad (7)$$

Equation (7) can be applied on designs of DPA to quantify their complexities. After which, the values would be normalized by a figure depending on the type of passive components of the DPA design. By designing the basic DPA with the simplest L-type matching network together with a one stage two-ports PA in each branch, the CF of two-way DPA for the different types of passive components used in the circuits can be deduced. The numbers have been calculated and shown in Tables 1 and 2.

For example, if a reported two-way DPA design with passive discrete components has a CF of 3556, it would have a normalized CF (NCF) of 2. The NCF can be applied to an N-way DPA depending on the applications and designs but the prevalent designs currently are limited to mostly three-way DPA.

Table 1. Base figures for normalization.

DPA Blocks	Complexity Variables	Complexity Number		
		Discrete Passives	T-Line Passives	Hybrid Passives
Power Divider	C_{PD}	9	9	9
Main Branch	C_{PA}	4	4	4
	$C_{M/N,i}$	2	4	3
	$C_{M/N,o}$	2	4	3
	C_{δ}	6	4	4
	C_M	96	256	144
Auxiliary Branch	C_{PA}	4	4	4
	$C_{M/N,i}$	2	4	3
	$C_{M/N,o}$	2	4	3
	C_{δ}	6	4	4
	C_A	96	256	144
	CF	1728	4608	2592

Table 2. Complexity factor for conventional DPA designs.

Types of Passive Components	Complexity Factor
Discrete	1728
T-Line	4608
Hybrid	2592

4. Experiments and Discussions

In this case study of DPA, one of the ways performance is quantified is by the PA figure-of-merit (FoM), which was developed in 2005 by the International Roadmap for Devices and Systems (ITRS) for PA design. It includes the critical aspects of its performance and considers the gain roll-off at high frequency of operation. The PA FoM is calculated by

$$PA\ FoM = P_{out} * G * PAE * f^2 \quad (8)$$

where the P_{out} is output power or saturated power, G is gain, PAE is power added efficiency and f is frequency of operation in GHz. The NCF together with the PA FoM provide a quick assessment on the performance limitation of DPA, which can also be extended to other circuit components applying this complexity analysis. The NCF itself is a FoM that can be complemented with the PA FoM but not to replace it. It is a function of parameters such as number of passive elements, topology of circuits and circuit design techniques as opposed to PA FoM, which are parameters of the PA results such as power, gain, and PAE.

Applying the formulas of the proposed NCF and PA FoM on reported DPAs as shown in Table 3, the scatter plot of PA FoM against NCF as shown in Figure 3 was derived. A design which ideally has low NCF and high PA FoM is what designers would need to achieve to work towards to and it should warrant a higher tendency of adoption as the design cycle time would be reduced as well as achieving good performances overall. The plot in Figure 3 could also be used as a benchmarking tool for designers to decide whether the design is comparable to the state-of-the-art DPA for his process technology and whether to adopt a higher PA FoM design based on the calculated NCF or to continue to develop the current design.

Table 3. Reported DPAs with PA FoM and normalized complexity factor.

Freq (GHz)	P _{sat} (dBm)	PAE (%)	G (dB)	NCF	PA FoM	Ref.
1.55	42	58.4	14	8.4	558.9	[8]
1.95	33	48.5	12.2	1.3	61.1	[9]
2.0	43	55.8	12	4.4	705.6	[10]
2.0	42	50.3	11 *	6.4	401.2	[4]
2.14	33 *	74	10.5 *	1.0	76	[11]
2.14	41.2	56.2	19.7	1.0	3166.4	[12]
2.14	42	58.3	16.5	0.4	1890.2	[5]
2.14	46	72.5	12	6.0	2094.9	[13]
2.14	50.5	40 *	10	2.3	2055.4	[14]
2.4	25	61.3 *	25	10	353.3	[15]
2.6	44	61.2 *	18 *	0.9	6555.6	[16]
2.65	42 *	46.3	16 *	0.5	1629.0	[17]
3.3	43	45.0 *	12.5 *	16.7	1739.1	[18]
4.9	44.5	60 *	11 *	9.2	5111.4	[19]
5.5	20	34.2 *	10	1.17	10.3	[20]
7.65	35	43 *	9 *	0.8	632.1	[21]
25.8	25.1	16.5	7	2.0	178.1	[22]
29.5	27.8	38	10.5	6.1	2235.8	[23]
45	18	21	8	3.0	169.3	[24]

* Values are estimated from graphs or calculated from gain and drain efficiencies.

Figure 3. PA FoM and normalized complexity factor plot. Designs with high PA FoM and low NCF are preferred. The orange plots represent CMOS DPAs, blue plots represent GaAs DPAs, and red plots represent GaN DPAs.

With about 19 data from DPA designs due to limited published works with transparent circuit designs and possibly the difficulty in current design and fabrication techniques at the millimeter-wave spectrum, the model was simulated by classifying the frequencies of operations into three frequency bands which are ultra-high frequency (UHF), super high frequency (SHF), and extremely high frequency (EHF) meant for mobile phones, satellite links, or wireless communication and remote sensing applications respectively. However, due to insufficient data for EHF DPA designs and for the sake of discussion, they are omitted from the graphs. The data of average gain, PAE and P_{sat} are plotted against the NCF in Figures 4 and 5, with Figure 4 suggesting that decreasing the NCF by about 400% from 8 to 2 could possibly increase the average gain of the DPA designed by up to 40%. This further suggests that designs which are targeting for gain should have their DPA NCF to be below 2. Designs which fall into the group of $0 < \text{NCF} < 2$ are using techniques which are mostly employing merged passive components to reduce the area as well as number of passive elements in the circuit. This could possibly lead to the reduction of cost of production and design time due to the smaller area. Substituting (4) into (6) with the other parameters as constants would result in complexity number of the branches directly proportional to the number of passive elements. It could be deduced that the complexity number would decrease with the decrease in the number of passive elements. The reduced number of passive elements could also be one of the reasons that the average gain could be higher compared to published DPA designs with $2 \leq \text{NCF} < 8$ as they have inherent insertion losses which could reduce the overall gain of the DPA.

For SHF applications, the increased in NCF does not contribute to a significant drop in average gain as suggested in Figure 4. This shows that for SHF applications, to design DPA for gain, designs should target the region of $0 < \text{NCF} < 2$. As also shown in Figure 4, the separate groups of specific designs circled for UHF and SHF are not feasible if design time and hence complexity, is an important factor for the designers who are designing for gain enhancement. Employing multiple harmonic tunings done by Steffen et al. [19] could reach a gain of 11dB for SHF applications but at the expense of a high NCF. On the other hand, a cascading design as demonstrated by J. Kang et al. [15] might enhance the gain significantly but the designer has to weigh the trade-off with an NCF of about 10. A few stages of PAs could be cascaded but it would lead to an exponential increase in complexity of

the main and auxiliary branches as shown in (3) and (6), leading to possibly larger area of the chip and longer time to design and optimize. Designing with multiple harmonic tunings could lead to a high PAE and gain for SHF applications. However, this results in a very high NCF of more than 8. It might increase the cost of manufacturing as the number of passive components used in the design increases due to the increase in the NCF.

Figure 4. Plot of average gain against normalized CF for different applications. One-way ANOVA at 90% confidence level with statistically significant difference.

Figure 5. Plot of average P_{sat} and PAE against normalized CF for different applications.

By comparing the initial gain of the designs for UHF or SHF applications, if the gain of the design is more than the average gain, designers could choose to continue with the development. However, if it is lower, the designers could instead, adopt published designs and reduce the overall design time to meet the TTM. Designers designing for gain and targeting UHF applications utilizing silicon processes for example could opt for designs which rely on merging passive components to reduce the complexity and the insertion losses due to the reduction in the number of passive network elements. A similar approach and analysis can be applied by designers who are targeting for other parameters such as PAE and P_{sat} , which have their average values plotted against NCF for the different applications in Figure 5. An example could be the correlation of PAE with NCF and the impact on operation cost. This model and methodology could be implemented by foundries, which could potentially allow a scalable benchmarking database for circuit designers to differentiate their designs with current state-of-the-art, allowing quick evaluation of the efforts required to adopt new circuit design techniques. One other current potential applications could be to couple with algorithm to design DPA such as one demonstrated by Chenyu Liang et al. [25]. It could possibly improve the 95 s of production time for a functional DPA prototype with a Linux workstation and pave ways for new applications.

5. Conclusions

In this paper, a benchmarking methodology to characterize and analyze complexity of circuits is proposed. Design teams could leverage on the presented methodology to identify and differentiate circuit techniques which would thereafter be adopted to meet overall design targets such as RF circuit performance. As an illustration, the presented methodology was used to analyze the circuit complexity of DPA circuits, in which an example objective—that is, gain optimization—was chosen. The relationship of NCF versus gain was discussed and practical design implications of this relationship were explored in detail. The use of this methodology could potentially be adopted for any circuit design and any aspect of circuit performance. The adoption of such a methodology may open up novel design approaches contributing to improvements to future circuit design.

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