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Random Dopant Fluctuation-Induced Variability in n-Type Junctionless Dual-Metal Gate FinFETs

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Abstract: We investigate the effect of random dopant fluctuation (RDF)-induced variability in n-type junctionless (JL) dual-metal gate (DMG) fin field-effect transistors (FinFETs) using a 3D computer-aided design simulation. We show that the drain voltage (V_{DS}) has a significant impact on the electrostatic integrity variability caused by RDF and is dependent on the ratio of gate lengths. The RDF-induced variability also increases as the length of control gate near the source decreases. Our simulations suggest that the proportion of the gate metal near the source to the entire gate should be greater than 0.5.

Keywords: random dopant fluctuations (RDF); junctionless (JL) FinFETs; dual-metal gate (DMG); ratio of gate lengths

1. Introduction

The scaling of complementary metal oxide semiconductor (CMOS)-integrated circuits to the nanoscale encounters performance barriers which are imposed by short channel effects (SCEs). Fin field-effect transistors (FinFETs) have the most promising structures for overcoming this limit [1,2]. Additionally, high-k metal gates are selected to minimize both SCEs and gate leakages at sub-32 nm technology node [2–4]. A dual-metal gate (DMG) structure is effective in eliminating SCEs. Selecting a low work function (WF) metal near the drain allows DMG devices to have higher carrier transport efficiency and better immunity to SCEs in comparison with single-metal gate (SMG) [5–10]. In comparison with the monotonic growth of the SMG structure from the source to the drain, the potential distribution near the transition of the two metals for a DMG transistor changes abruptly, caused by the different gate WFs. More precisely, there are two electric field peaks in the DMG device and only one near the drain in the SMG device [11]. Therefore, the electron velocity increases by enhancing the electric field. Furthermore, the SCEs are suppressed as a result of the screening of the drain voltage by the second gate [5].

Aggressive scaling in MOSFET technology makes it difficult to realize ultra-small and shallow source/drain junctions [10–14]. To counter these fabrication limitations, a junctionless (JL) transistor was proposed. In a JL device, homogenous doping and uniform concentration are used in the source, channel, and drain regions. Therefore, there is no junction in the channel. In comparison with a conventional inversion-mode transistor, a JL transistor has a simpler fabrication process, lower ON-state electric field, lower leakage current, and better immunity to SCEs. These advantages make JL transistors promising candidates for future technology nodes [10,11,14–18].

However, random dopant fluctuations (RDF) significantly affect the performance of JL devices [14,19,20]. Although the effect of RDF on SMG JL FinFETs has been studied [12], there has been no report on RDF-induced variability in DMG JL FinFETs. Therefore, we investigate the RDF-induced performance variability in DMG JL FinFETs.

2. Device Structure and Simulation

The randomized doping profile and structure of the n-channel DMG JL FinFET utilized in this work is shown in Figure 1. The device dimensions of the DMG JL FinFET are as follows: a gate oxide thickness of 2 nm, a fin width of 5 nm, a fin height of 15 nm, and a channel length of 20 nm. The DMG JL FinFET has two different gate metals, M1 and M2, which correspond to MoN [4] and NiAl (110) [12], whose work functions are 4.76 eV near the source and 4.27 eV near the drain, respectively. To accurately investigate the effect of RDF-induced variability in DMG JL FinFET, we set the L_1/L ratio to 0, 0.2, 0.4, 0.6, 0.8, and 1 with gate-source voltage (V_{GS}) sweeping from 0 V to 1 V for both linear ($V_{DS} = 50$ mV) and saturated ($V_{DS} = 1$ V) device operation. The length of the channel region under M1 is L_1 ; the length of the channel region under M2 is L_2 , and the total gate length is $L = L_1 + L_2 = 20$ nm. In this work, all the simulations are carried out by Sentaurus, a three-dimensional technology, computer-aided design simulator. Using the dedicated randomization algorithm based on Sano's methodology provided in the simulator, the effect of RDF was explored according to the charge density equation, $\rho(r) = q\kappa_C^3[\sin(\kappa_C r) - \kappa_C r \cos(\kappa_C r)]/[2\pi^2(\kappa_C r)^3]$, where r is the radial distance from the center of the atom, and κ_C is screen factor assigned by the equation $\kappa_C \approx 2(N_{D/A})^{1/3}$ ($N_{D/A}$ is donor/acceptor concentration). First, we generated 200 random doping profiles [21,22]. Then, we used these doping profiles to solve the characteristic current–voltage curve for each L_1/L in both saturated and linear operation.

Figure 1. (a) Randomized doping profile and structure for dual-metal gate Junctionless FinFET, (b) Cross section along the x-axis at $x = 0$. The gate near the source is called the “control gate”, and the gate near the drain is called the “screen gate”.

In the simulation, the models selected or activated include the drift-diffusion model in combination with the density gradient for quantum corrections; the mobility model that incorporates the high-field saturation, doping dependence, and field perpendicular to the semiconductor–insulator interface; the Shockley Read Hall (SRH) model for recombination generation; and the evaluation of the SRH lifetimes according to the Scharfetter model [2,22].

3. Results and Discussion

The transfer curves for the simulated DMG JL FinFET with L_1/L from 1 to 0 in steps of -0.2 are shown in Figure 2. The dispersion of transfer curves indicates RDF-induced electrostatic integrity variability in the DMG JL FinFET. The left and the right axis show the drain current in log scale and linear scale, respectively. The linear scale shows the variability of saturation current, and the log scale shows the sub-threshold current. It can be observed that a decreasing L_1/L has a negative impact on the RDF-induced variability, and the variability for each L_1/L in the saturation region and the

linear region is different. Further, we find that, as L_1/L becomes smaller, off-state current increases significantly and the threshold voltage (V_{TH}) also decreases (see Figure 3), resulting in an increase in current. In the case of each given L_1/L , the ON-state current of the saturation region is larger than that of the linear region, i.e., the blue curve is higher than the red curve in Figure 2. Moreover, the dispersion of the saturation region curves is larger than that of the linear region, i.e., the set of blue curves occupy a larger area than the set of red curves in ON-state as shown in Figure 2. In the saturated region, performance fluctuation caused by RDF of DMG JL FinFET is more than that seen in the linear region.

Figure 2. RDF-induced dispersions of drain current versus gate voltage (V_{GS}) for DMG JL FinFET. (a–f) are transfer curves in L_1/L from 0 to 1 in steps of 0.2.

The frequency distribution of V_{TH} for each L_1/L at $V_{DS} = 0.05$ V and 1 V is shown in Figure 3. The standard deviations (σ), average (μ), and coefficient (σ/μ) of variation of V_{TH} for each case were also calculated. The V_{TH} of the device is extracted by the constant-current method, with the current set at $0.1 \mu\text{A}/\mu\text{m}$. In this case, because 4.27 eV is too small to be used as the work function of the metal gate of the n-channel JL FinFET, the V_{TH} at $L_1/L = 0$ is not considered. In Figure 3, when L_1/L is between 0.6 and 1, the V_{TH} fluctuation caused by RDF in the saturation region is larger than in the linear

region. However, when L_1/L is less than 0.4, the relative standard deviations of V_{TH} caused by RDF in the saturated region is smaller than in the linear region. In addition, when L_1/L is less than 0.4, the standard deviation of V_{TH} increases rapidly. In general, as L_1/L decreases, the average of V_{TH} becomes smaller, and the RDF-induced fluctuation becomes worse. As L_1/L becomes smaller, the dopant ions under the control gate decreases, causing the influence of RDF to increase. Further, the standard deviation of V_{TH} is inversely proportional to the square root of the channel area [23,24]. Therefore, as L_1 is continuously reduced, the fluctuation of V_{TH} increases. In Figure 4, a quantile-quantile (QQ) plot shows that the distribution of V_{TH} is approximately fitted to the Gaussian distribution.

Figure 3. Frequency distribution of V_{TH} with different L_1/L at $V_{DS} = 0.05$ V and 1 V.

Figure 4. Quantile-quantile plots of V_{TH} with $L_1/L = 0.2$ and 0.8.

The sub-threshold swing (SS) characteristics of the DMG FinFET at L_1/L from 0 to 1 in steps of 0.2 are shown in Figure 5. DMG FinFET has a larger SS in comparison with a corresponding SMG FinFET with a MoN gate. The SS is inversely proportional to the effective length [12,25], and the effective length of the DMG FinFET is only slightly larger than the length of the control gate L_1 in the sub-threshold region. On the other hand, the effective length of the SMG FinFET is slightly larger than the channel length L [12]. With a decrease in L_1 or L_1/L , the effective length decreases. Thus, the SS of the DMG FinFET increases gradually. When L_1/L is between 0.4 and 1, the SS and its fluctuation are small; however, when L_1/L is less than 0.4, they both increase sharply. Additionally, in comparison with the linear region, the value of SS can be lowered in the saturated region. Therefore, the SS fluctuation caused by RDF is suppressed in the saturated region.

Figure 5. Frequency distribution of sub-threshold swing with different L_1/L at $V_{DS} = 0.05$ V and 1 V.

Generally, RDF-induced variability is more serious as the length of L_1 decreases. At the same time, the effect of RDF in the channel under M2 is relatively weak in causing device performance fluctuations for the DMG JL FinFET. As shown in Figure 6, there are different conditions between the two channels under M1 and M2 near the source and the drain. Because M1 and M2 have different work functions, the effects of V_{GS} on the channel electrostatic potential near gate and drain regions are also different. The contour plots of normalized electrostatic potential in the channel, near the source and near the drain are shown in Figure 6a,b, respectively. The direction of the electric field is perpendicular to the equipotential line, and the electric field flows from a higher electrostatic potential to a lower electrostatic potential [26]. The electric field in the channel near the drain is larger, as seen in the difference in electric field distribution between Figure 6c,d. As a result, M2 has more control over the channel. Specifically, the overall device performance is affected by the RDF, predominantly from the channel under the M1. Therefore, where the overall L value is constant, L_2 will continue to grow longer as L_1 becomes shorter, which means that the area occupied by M1 is decreasing. Therefore, for a DMG, it is necessary to ensure that L_1/L is greater than a threshold value. Some studies regard $L_1/L = 0.5$ as a suitable value when the RDF effect is not considered [12]. However, our observations indicate, L_1/L should be slightly greater than 0.5 due to RDF.

Figure 6. Electrostatic potential (a,b), and electric field (c,d) in the DMG JL FinFET at $L_1/L = 0.4$ near the source (a,c) and drain (b,d).

4. Conclusions

The RDF-induced electrostatic integrity fluctuation in DMG JL FinFET has been explored in this paper. It was observed that the random variation of DMG performance due to RDF mainly originates from the channel under the control gate near the source. By introducing a second metal gate close to the drain, RDF-induced variability gradually worsens. Further, L_1/L has a considerable influence on the fluctuation caused by RDF. Specifically, as L_1/L is decreased, the fluctuation caused by RDF on device performance increases. Additionally, the RDF-induced performance fluctuations of the DMG JL FinFET are slightly different between saturated and linear regions. The introduction of a smaller work function gate metal near the drain has a significant influence on the performance of the entire device when L_1/L is too small. Therefore, it is possible to increase the value of L_1/L to more than 0.5.

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