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Standalone Operation of Modified Seven-Level Packed U-Cell (MPUC) Single-Phase Inverter

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Abstract: In this paper the standalone operation of the modified seven-level Packed U-Cell (MPUC) inverter is presented and analyzed. The MPUC inverter has two DC sources and six switches, which generate seven voltage levels at the output. Compared to cascaded H-bridge and neutral point clamp multilevel inverters, the MPUC inverter generates a higher number of voltage levels using fewer components. The experimental results of the MPUC prototype validate the appropriate operation of the multilevel inverter dealing with various load types including motor, linear, and nonlinear ones. The design considerations, including output AC voltage RMS value, switching frequency, and switch voltage rating, as well as the harmonic analysis of the output voltage waveform, are taken into account to prove the advantages of the introduced multilevel inverter.

Keywords: multilevel inverter; packed u-cell; power quality; multicarrier pwm; renewable energy conversion

1. Introduction

Power electronic inverters are key players in modern electric networks. They are installed wherever DC voltage exists (like in a battery and solar panels), while loads need AC voltage. Although a full-bridge inverter with four switches is the most common technology on the market, newly emerged multilevel inverters are replacing older products due to the reduced cost of the semiconductor devices [1,2].

Many studies have focused on multilevel inverter development, both in topology and control strategy aspects. Attention is mainly paid to the number of components employed in such inverters [3]. The fewer components that are used, the lower the power losses and the lower the costs. The two most popular topologies are called Cascaded H-bridge (CHB) [4] and Neutral Point Clamped (NPC) [5] multilevel inverters, which have found some industrial applications in high power motor drives. Moreover, various topologies have been introduced for different applications including single-phase, three-phase, medium power, and low voltage [6–13].

Apart from the number of levels, the appropriate application of multilevel inverters is very important. Most of the reported topologies have too many isolated DC sources, which make it very difficult to use them in practical applications. An AC transformer and a diode bridge are required to build an isolated DC source, which is costly and bulky to manufacture [14–17]. As a result, single-DC-source topologies like NPC and 5-level Packed U-Cell (PUC5) inverter [18,19] found industrial applications rather than the other new technologies. However, some other topologies like CHB are used at a very high power rating because they need isolated DC sources. This is because, at very high power and high voltage ratings, there are limitations on the switches available in the market and CHB helps divide the voltage between cells to use medium-voltage components in those high-power applications. Moreover, the modularity of the CHB is another feature that has induced the industry to employ it even with isolated DC sources [20–22].

Recently, a seven-level MPUC inverter has been introduced as a remedy for applications in which different PV panels are available to connect to separate DC links. In [23], the authors showed that different types of PV panels with different power and voltage ratings can be connected to 2 DC links of the MPUC inverter and the combined maximum powers are processed, controlled, and finally delivered to the grid at unity power factor. That paper was devoted to the grid-connected mode of operation of MPUC inverter, with a focus on PV applications.

In this paper, the MPUC inverter configuration is analyzed in detail, including the switching frequency and voltage rating of each single device. Moreover, the RMS value of the seven-level output AC voltage waveform is formulated and calculated as a practical design consideration for the standalone mode of operation. The practical implementation of the seven-level MPUC inverter is attempted and the experimental results are shown in Section 4. Various types of loads are connected in parallel to validate the good dynamic performance of the proposed topology. Eventually, the technical points and expected applications of MPUC inverter are discussed.

2. Seven-Level Modified Pack U-Cell Inverter

The seven-level MPUC inverter is shown in Figure 1. It has almost the same configuration as PUC5 but with a reversed direction of the lower DC source and two switches (T3 and T6). Unlike PUC5, which generates the maximum voltage level equal to its DC source [24], the MPUC inverter provides higher voltage amplitude by connecting two DC sources (V1 and V2) in series.

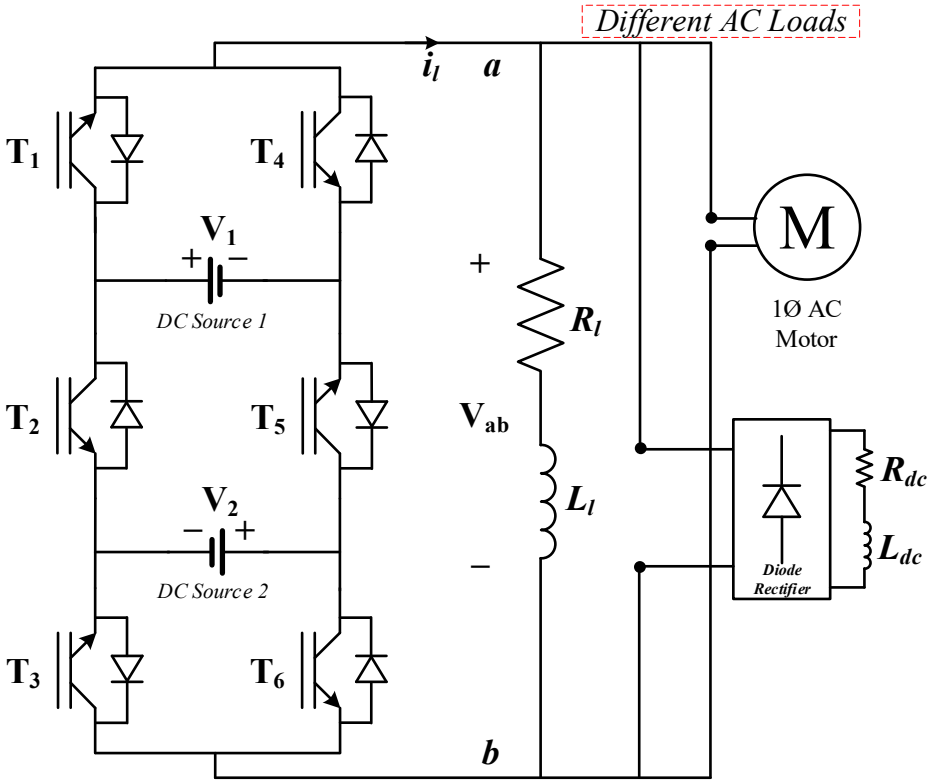

Figure 1. Single-phase seven-level MPUC inverter in standalone mode of operation.

All possible switching states of the MPUC inverter are listed in Table 1. It is observed that if V1 is twice V2, then seven identical voltage levels will be produced at the output. Considering $V_1 = 2V_2 = 2E$, all seven voltage levels would be 0, ±E, ±2E, ±3E. The highest voltage level of 3E is generated by connecting two DC sources in series (V1 + V2). 2E is produced through the upper DC source (V1). The voltage level of E is sent to the output by the lower DC source (V2).

Table 1. All possible switching states and voltage levels of MPUC inverter.

Switching State	T_1	T_2	T_3	T_4	T_5	T_6	V_{ab}
1	1	0	1	0	1	0	$V_1 + V_2$
2	1	0	0	0	1	1	V_1
3	0	0	1	1	1	0	V_2
4	0	0	0	1	1	1	0
5	1	1	1	0	0	0	0
6	1	1	0	0	0	1	$-V_2$
7	0	1	1	1	0	0	$-V_1$
8	0	1	0	1	0	1	$V_2 + V_1$

Paying attention to the switching states, it is clear that regardless of the switching and carrier frequency of PWM technique, T2 and T5 will work at the line frequency, which is 60 Hz in this work. This fact is proved through experimental results in the next sections. This helps to reduce the switching losses significantly. Moreover, having redundant states at 0 voltage helps reduce the switching frequency during the transition of the reference AC signal between positive and negative half cycles. Moreover, the modulation details have been provided in [23]. As a brief summary, a four-carrier level-shifted PWM has been used to modulate the reference signal and generate the switching pulses according to Table 1.

3. Design Consideration for Standalone Applications

An analysis has been performed in case of the stand-alone application of the MPUC inverter delivering energy to the single-phase loads.

Since a single-phase load needs a certain RMS voltage value (120 V 60 Hz or 220 V 50 Hz), the following analyses are done based on Figure 2 to achieve a general formula for RMS value calculation of a seven-level inverter's output AC voltage waveforms.

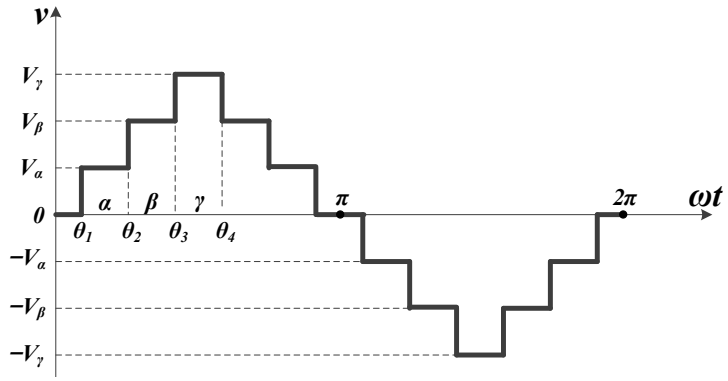

Figure 2. Seven-level AC waveform with specified angles for RMS calculation.

The RMS value of each alternating function ise given by:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}, \tag{1}$$

in which T is the alternating period and $v(t)$ is the alternating function, for which the RMS value would be V_{rms}.

Based on Figure 2, the seven-level output voltage waveform is a modified square wave with a period of 2π, which is symmetrical on two positive and negative half cycles. Thus, Equation (1) can

be rewritten for a seven-level waveform with the specified angles and level amplitudes demonstrated in Figure 2 as follows:

$$\begin{aligned} V_{rms} &= \sqrt{\tfrac{1}{T}\int_0^T v^2(t)\,dt} \\ &= \sqrt{\tfrac{1}{2\pi}\int_0^{2\pi} v^2(t)\,d\omega t} \\ &= \sqrt{\tfrac{1}{2\pi}\left[4\int_{\theta_1}^{\theta_2} V_\alpha^2\,d\omega t + 4\int_{\theta_2}^{\theta_3} V_\beta^2\,d\omega t + 2\int_{\theta_3}^{\theta_4} V_\gamma^2\,d\omega t\right]} \\ &= \sqrt{\tfrac{1}{2\pi}\left[4\alpha V_\alpha^2 + 4\beta V_\beta^2 + 2\gamma V_\gamma^2\right]} \end{aligned} \tag{2}$$

Considering the voltage values and levels in Table 1 for a seven-level MPUC inverter, the following formula will be derived for its output voltage RMS value:

$$\begin{aligned} V_{rms} &= \sqrt{\tfrac{1}{2\pi}\left[4\alpha V_1^2 + 4\beta V_2^2 + 2\gamma(V_1+V_2)^2\right]} \\ &= \sqrt{\tfrac{1}{2\pi}\left[4\alpha V_1^2 + 4\beta(2V_1)^2 + 2\gamma(3V_1)^2\right]} \\ &= V_1\sqrt{\tfrac{4\alpha+16\beta+18\gamma}{2\pi}} \\ &= V_1\sqrt{\tfrac{2\alpha+8\beta+9\gamma}{\pi}} \end{aligned} \tag{3}$$

Consider that α, β, and γ are the angles at which the reference wave crosses the voltage levels as fixed lines between carriers. For instance, in a seven-level inverter, there are six carriers to modulate the reference waveform. Since they have been shifted vertically between +1 and −1, then each level line will have values of 2/3, 1/3, 0, −1/3, and −2/3, respectively. The reference wave function is assumed to be:

$$V_{ref} = m_a \sin \omega t, \tag{4}$$

where m_a is the modulation index. As an example, α can be calculated by equaling the V_{ref} function and the level line of 1/3, where the amplitude is V_2 = E.

$$m_a \sin \omega t = \frac{1}{3} \rightarrow \alpha = \omega t = \arcsin\frac{1}{3m_a} \tag{5}$$

By similar calculations, all other angles can be computed and substituted in Equation (3). Consequently, the RMS voltage value for the proposed seven-level MPUC inverter, in terms of output maximum voltage amplitude ($V_{\max}$ = $3V_2$ = 3E) and modulation index, has been obtained voa the following formula:

$$V_{rms} = 0.725 \times m_a \times V_{\max}. \tag{6}$$

As a single-phase stand-alone application in a 120 V 60 Hz grid, the output maximum voltage should be around 170 and the RMS value is 120 V. One possible case for DC source amplitudes and m_a can be as follows:

$$\begin{cases} V_1 = 113.2\ V \\ V_2 = 56.6\ V \\ m_a = 0.98 \end{cases}. \tag{7}$$

That results in generating an output RMS value of 120 V and a maximum value of almost 170 V.

The other design consideration is described in the next section about the switching frequencies and voltage ratings of the switches using experimental test results.

4. Experimental Results and Discussion

The proposed seven-level MPUC inverter has been implemented in standalone mode to verify the above analysis. It has been tested under various load types including linear and nonlinear. Six IGBT

switches (600 V, 30 A, FGH30N60LSD) have been used in the experimental prototype. The designed switching algorithm was thoroughly explained in [23], which uses four level-shifted carriers to modulate the reference signal. It has been implemented on a dSpace 1103 real-time controller to generate switching pulses and fire the switches through gate drivers. Table 2 includes the complete system parameters. The whole setup was prepared based on Figure 1. Two DC sources are connected to the DC links V_1 and V_2 and different loads are connected at the output.

Table 2. Experimental setup parameters.

First DC bus voltage (V_1)	100 V
Second DC bus voltage (V_2)	50 V
Load Voltage Frequency (f_{grid})	60 Hz
Switching Frequency (f_{PWM})	2 KHz
AC Load Resistor (R_l)	40 Ω
AC Load Inductor (L_l)	20 mH
Rectifier Side Resistor (R_{dc})	20 Ω
Rectifier Side Inductor (L_{dc})	60 mH
Single-Phase AC Universal Motor	120 V, 3 A

In the first test, the MPUC inverter has been connected to an RL load with parameters of R_l and L_l shown in Table 2 and the results are illustrated in Figure 3. The V_{ab} waveform includes identical seven voltage levels with a maximum value of 150 V, which is the sum of two DC source amplitudes. The symmetrical load voltage and current waveforms prove the appropriate modulation technique. Moreover, the total harmonic distortion (THD) of the output voltage waveform without using any filters is 6%. With this low harmonic voltage, the required filters would be small and cost-effective for every application of the MPUC inverter, especially as a renewable energy interface.

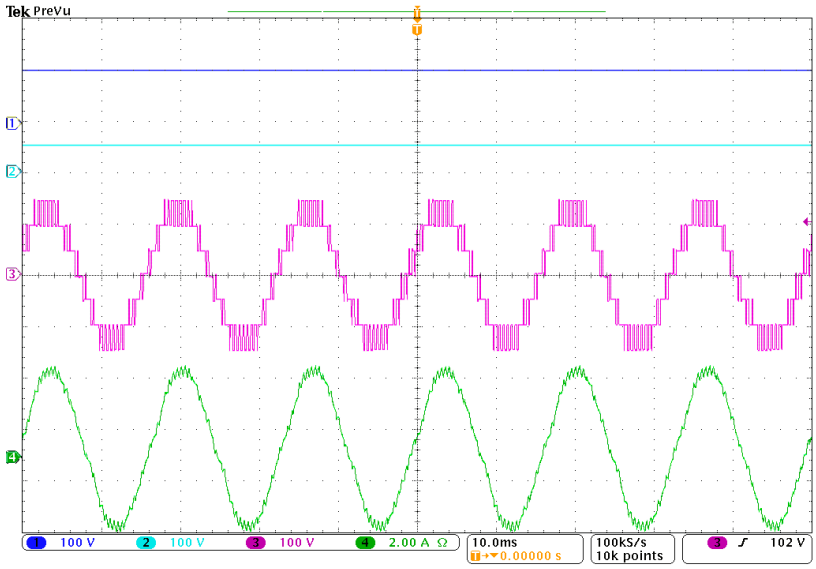

Figure 3. Seven-level MPUC inverter output voltage and current with DC source voltages. Ch_1: V_1, Ch_2: V_2, Ch_3: V_{ab}, Ch_4: i_l.

To investigate the switching frequency of the MPUC topology, the gate pulses of switches T_1, T_2 and T_3 as well as the output voltage have been captured for one cycle, which is illustrated in Figure 4. By counting the switching pulses in one cycle, the switching frequency of MPUC inverter IGBTs can be calculated, as presented in Table 3. Since each pair of switches is working complementarily, both switches in each cell would have an identical working frequency.

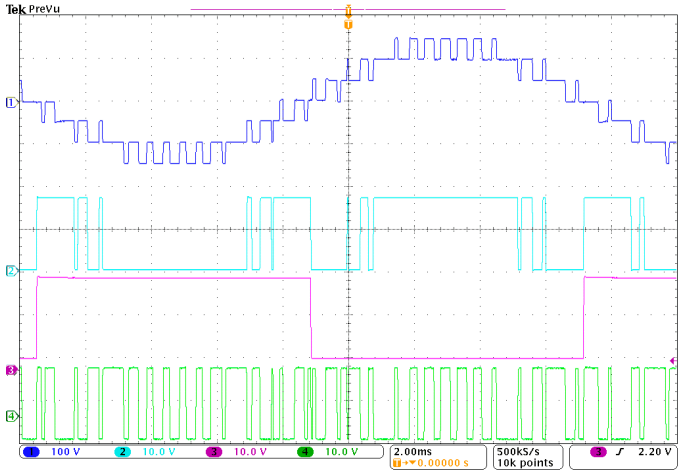

Figure 4. One cycle of output voltage and gate pulses of MPUC inverter switches. Ch_1: V_{ab}, Ch_2: T_1 gate pulses, Ch_3: T_2 gate pulses, Ch_4: T_3 gate pulses.

Table 3. Switching frequency of MPUC inverter switches.

T_1 & T_4	600 Hz
T_2 & T_5	60 Hz
T_3 & T_6	1920 Hz

The voltage rating of each switch has been measured and the results are depicted in Figure 5. From Figures 4 and 5, it is obvious that the two upper switches have a voltage rating of V_1 and the two lower switches have to suffer the V_2 during switching times. The advantage of the MPUC structure is that, although the two middle switches' voltage ratings are higher than those of the other switches and it is $V_1 + V_2$, they are working at grid frequency, thus high-power switches with low switching frequency can be used in the middle cell including T_2 and T_5.

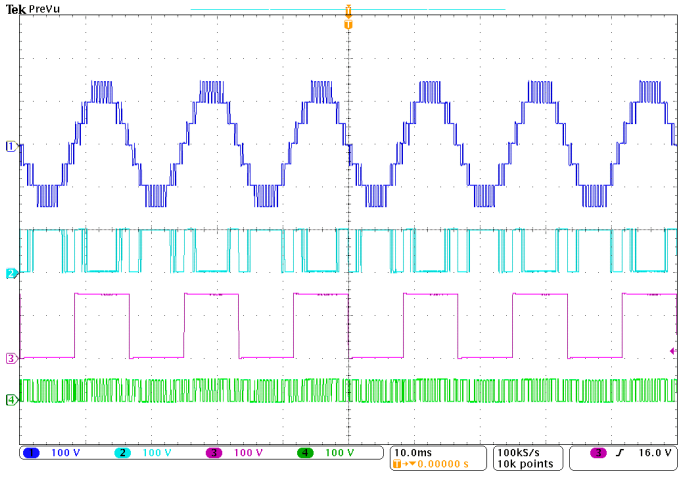

Figure 5. MPUC inverter switches' voltage ratings. Ch_1: V_{ab}, Ch_2: T_1 voltage, Ch_3: T_2 voltage, Ch_4: T_3 voltage.

In another test, a nonlinear load including a single-phase diode rectifier with resistor and inductor on its DC side (R_{dc} = 20 Ω and L_{dc} = 60 mH) has been added, as shown in Figure 1. The load voltage and current waveforms, as well as the rectifier DC side voltage and current, have been depicted in Figure 6.

Another test has been performed to show the performance of the proposed topology in real conditions. In this part, the MPUC was supplying the RL load to which the nonlinear load was

connected, and after a while a single-phase universal motor was paralleled with other loads (linear and nonlinear). The step-by-step process for connecting loads is depicted in Figure 7, which shows acceptable results in the case of UPS application.

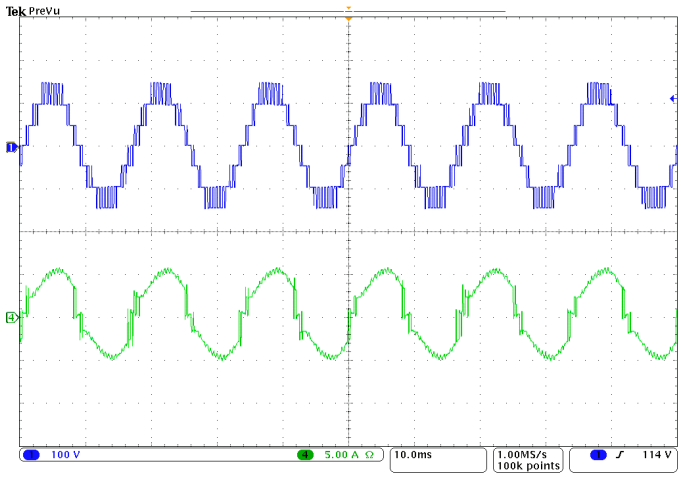

Figure 6. Test results when a nonlinear load is connected to the MPUC inverter. Ch_1: V_{ab}, Ch_4: i_l.

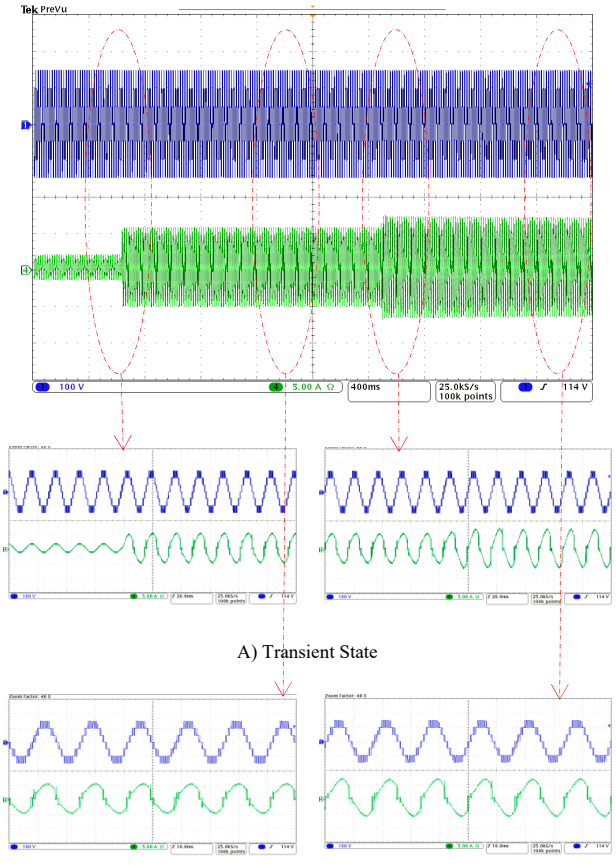

Figure 7. Output voltage and current waveform of MPUC inverter when different loads are added step by step. Ch_1: V_{ab}, Ch_4: i_l. (**A**) Transient state when nonlinear load is added to the RL load (left) and after a while a motor load is added to the system (right); (**B**) steady state when a nonlinear load is added to the RL load (left) and after a while a motor load is added to the system (right).

For the last test, the design consideration explained in Section 3 regarding the 120 V output AC voltage RMS value has been applied. Figure 8 shows the output voltage and current waveforms as well as RMS values that are near the expected value calculated earlier in Equation (7). In this case, the source values have been set to 113.2 V and 56.6 V, respectively, and the m_a is 0.98 to generate a voltage waveform with maximum 170 V and RMS value of 120 V 60 Hz useable for single-phase UPS applications.

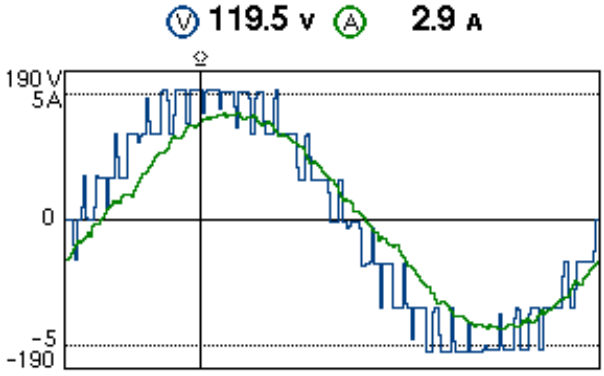

Figure 8. Voltage and current waveform of MPUC inverter with RMS calculation for 120 V system.

Finally, a comparison has been performed between a single-phase MPUC inverter and the popular topology of multilevel inverters called Cascaded H-Bridge (CHB), which contains full-bridge inverter cells including four semiconductor switches and one DC source in each cell [25]. The CHB inverter can generate different voltage levels based on the connected DC sources' amplitudes. If the DC sources are identical it would be called CHB with equal DC sources; if the sources are not identical, it is called CHB with unequal DC sources. Table 4 contains information to compare the seven-level MPUC inverter to the seven-level CHB inverters with equal and unequal DC sources.

Table 4. Comparison between seven-level MPUC topology and seven-level CHBs inverter.

Topologies	Active Switches	DC Sources
seven-level CHB with Equal DC Sources	12	3
seven-level CHB with Unequal DC Sources	8	2
seven-level MPUC	6	2

As shown in Table 4, the advantage of the proposed seven-level MPUC inverter is that it has fewer components, which makes it cost-effective for manufacturers. Moreover, the low THD of the output voltage requires small filters that can make the inverter package smaller than other conventional inverters. Finally, it should be mentioned that the low switching frequency of the MPUC switches leads to reduced power losses that increase the inverter efficiency and lifetime.

As a simple comparison with CHB and NPC, it could be mentioned that the MPUC converter uses only six switches and two DC sources to generate a seven-level voltage waveform. In a similar case, the CHB uses eight switches that increase the manufacturing costs and power losses. Moreover, NPC uses 12 active switches, 10 diodes, and six DC sources to produce a seven-level voltage waveform that is obviously much more expensive and makes more power losses.

Moreover, looking at Figure 1, it can be seen that the two pairs of switches have common emitter (T_2–T_3, T_4–T_5), so their gate drives need a common power supply, which entails a reduction in the size of the manufactured circuit boards.

5. Conclusions

In this paper a reconfigured PUC inverter topology has been presented and studied experimentally. The proposed MPUC inverter can generate a seven-level voltage waveform at the output with low

harmonic contents. The associated switching algorithm has been designed and implemented on the introduced MPUC topology with reduced switching frequency aspect. Switches' frequencies and ratings have been investigated experimentally to validate the good dynamic performance of the proposed topology. Moreover, the comparison of MPUC to the CHB multilevel inverter showed other advantages of the proposed multilevel inverter topology, including fewer components, a lower manufacturing price, and a smaller package due to reduced filter size.

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