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A Novel Three-Switch Z-Source SEPIC Inverter

Baocheng Wang * and Wei Tang

Department of Electrical Engineering, Yanshan University, Qinhuangdao 066004, China;
weitang@stumail.ysu.edu.cn

* Correspondence: bcwang@ysu.edu.cn

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Abstract: In this paper, a novel single-phase transformerless Z-source inverter (ZSI) derived from the basic SEPIC topology, which is named SEPIC-based ZSI, is proposed. The negative end of the input DC voltage of this topology is directly connected to the load and grounded, which can completely eliminate leakage current. Furthermore, this topology has some attractive characteristics such as buck–boost capability, impressive voltage gain, linear voltage gain is realized by a simple control method, and so on. The theoretical design and simulation results are demonstrated by corresponding experiments carried out on a 500 W laboratory prototype controlled by using a DSP TMS320F28335 controller combined with a FPGA SPARTAN-6.

Keywords: transformerless; SEPIC converter; single phase; Z-source inverter

1. Introduction

At present, with the consumption of fossil fuels and environmental pollution, people are increasingly persistent in the development of renewable distributed energy generation systems such as photovoltaic (PV), fuel cell (FC), and so on [1–5]. Among them, photovoltaic power generation, which is used to convert solar energy into electricity, is the most widely applied [6–8]. However, the output electricity is DC, and therefore an inverter is necessary for the photovoltaic power generation system [9].

Based on the availability of transformers, inverters are divided into isolated inverters and non-isolated inverters [10]. Isolated inverters have the advantage of isolating, which can eliminate leakage current and ensure the safety of staff. However, the isolated inverters will have a large volume and loss due to the existing transformers [11], which do not meet the concept of energy saving. As such, more people have turned their attention to non-isolated inverters [12].

Many interesting non-isolated topologies, such as H5 [13], H6 [14], and ZVR [15], have been presented in the literature. Although constantly improving topologies or control methods can reduce their leakage currents to a certain extent, the existing leakage currents in their topologies cannot be eliminated from the source. Furthermore, the voltage gain of these topologies is often unsatisfied.

A great deal of attention has been paid to the Z-source inverter (ZSI) since it was first proposed [16]. The characteristic of the Z-source inverter is that it has very high boost capacity. Therefore, many quasi and semi Z-source inverters have been developed [17–19], but they still cannot deal thoroughly with the problem of leakage current. As a result, some inverter topologies that are combined with Z-source topologies and have the feature of dual-grounding are proposed [20]. Based on the analysis of leakage current [21], dual-grounding can completely solve the problem of leakage current. Although the proposed inverters in [20] have their advantages, they are not suitable for some field applications; the buck–boost-based type of three-switch three-state (TSTS) ZSIs cannot produce reactive power and the boost-based type of TSTS ZSIs cannot filter well, due to the lack of a filter inductor, which results in higher total harmonic distortion (THD). A new Z-source inverter-based on a CUK converter is

proposed in [22], which has a better filter compared to the inverters in [20], but there is a current spark in the S1 switch when the topology starts. The SEPIC-based Z-source inverter is proposed in [23], but its performance is not verified by experiments.

According to the above analysis, this paper puts forward a novel Z-source inverter based on a SEPIC converter. Compared with traditional semi and quasi Z-source inverters, the proposed inverter has the feature of dual-grounding, which is valid for thoroughly eliminating leakage current. Furthermore, the voltage gain of the proposed inverter is more than 1, which can be applied well for a flexible output situation. Furthermore, the proposed inverter is based on a SEPIC converter. The SEPIC converter has the superiority of having the same polarity of input and output, the isolation of input and output, and a complete turn-off. At the same time, the proposed topology has solved the current spark problem in the S1 switch. Therefore, a new topology named “SEPIC-based ZSI” is presented. This topology can be used in situations where flexible control voltage is required. At the same time, the sine output is negative first and then positive, which can meet some application requirements.

This paper is organized as follows: Firstly, the operation modes of the proposed inverter are analyzed and the design of the components is presented in Section 2. Section 3 displays the control diagram of the proposed inverter and some key waveforms under the driven signal. Secondly, the theoretical analysis is proved through corresponding simulations and experiments, which are shown in Section 4. Finally, a complete summary of the proposed topology is given in Section 5.

2. Operation Mode and Analysis of the Novel Inverter

The operation mode, including the mode analysis and the design of the proposed SEPIC-based ZSI, including the parameters calculation, is discussed in this section.

2.1. Structure and Operation Mode

The structure of the proposed SEPIC-based ZSI, which is derived from a combination of a Z-source inverter and a SEPIC converter, is shown in Figure 1. Z-source inverters have an outstanding buck–boost capacity and the SEPIC converter has advantages including the same polarity of input and output, the isolation of input and output, and a complete turn-off. Furthermore, the negative terminal of the PV array is connected to the load side, which is necessary for eliminating leakage current, as shown in Figure 1. Three operation modes are shown in Figure 2.

Figure 1. Proposed SEPIC-based Z-source inverter (ZSI).

Figure 2. Equivalent circuits of the SEPIC-based ZSI in one switching period (a) S_1 and S_3 are ON, S_2 is OFF; (b) S_1 and S_2 are ON, S_3 is OFF; and (c) S_2 and S_3 are ON, S_1 is OFF.

The operation modes are discussed as follows: In mode I, as shown in Figure 2a, switch S_1 and switch S_3 are on, whereas switch S_2 is off. The inductor, L_f , is magnetized by input voltage V_{in} , and capacitors C_1 , C_2 , and C_3 are charged. According to Kirchhoff's law of voltage and current, the expression of this mode is shown in Equations (1) and (2). In mode II, switch S_3 is off and switches S_1 and S_2 are on, as shown in Figure 2b. The inductor, L_f , is magnetized by input voltage V_{in} , and capacitors C_1 , C_2 , and C_3 are discharged. Equations (3) and (4) show the expression of mode II. In mode III, switches S_2 and S_3 are turned on while switch S_1 is turned off, as depicted in Figure 2c. Capacitors C_1 , C_2 , and

C3 are charged. The equations of this mode are expressed as shown in Equations (5) and (6). In Figure 2, the dashed line direction represents the current direction of the inductors.

$$\begin{cases} V_{Lf} = V_{in} \\ V_{L1} = -(V_{C0} + V_{C2} + V_{C3}) \\ V_{L2} = -(V_{C0} + V_{C1} + V_{C3}) \\ V_{L3} = -V_{C3} \end{cases} \quad (1)$$

$$\begin{cases} i_{C1} = i_{L2} \\ i_{C2} = i_{L1} \\ i_{C3} = i_{L1} + i_{L2} + i_{L3} \\ i_{C0} = i_{L1} + i_{L2} - i_o \end{cases} \quad (2)$$

where V_{in} denotes the input voltage; V_{C0} , V_{C1} , V_{C2} , and V_{C3} are the voltage of capacitors C0, C1, C2, and C3; and i_{C1} , i_{C2} , and i_{C3} are the current of capacitors C1, C2, and C3. Similarly, V_{L1} , V_{L2} , V_{L3} , and V_{Lf} are the voltage of inductors L1, L2, L3, and input inductor Lf, and i_{L1} , i_{L2} , and i_{L3} are the current of inductors L1, L2, and L3. i_o is the output current.

$$\begin{cases} V_{Lf} = V_{in} \\ V_{L1} = V_{C1} \\ V_{L2} = V_{C2} \\ V_{L3} = -V_{C3} \end{cases} \quad (3)$$

$$\begin{cases} i_{C1} = -i_{L1} \\ i_{C2} = -i_{L2} \\ i_{C3} = -i_{L3} \\ i_{C0} = -i_o \end{cases} \quad (4)$$

$$\begin{cases} V_{Lf} = V_{in} - (V_{C0} + V_{C1} + V_{C2} + V_{C3}) \\ V_{L1} = V_{C1} \\ V_{L2} = V_{C2} \\ V_{L3} = V_{C0} + V_{C1} + V_{C2} \end{cases} \quad (5)$$

$$\begin{cases} i_{C1} = i_{Lf} - i_{L1} - i_{L3} \\ i_{C2} = i_{Lf} - i_{L2} - i_{L3} \\ i_{C3} = i_{Lf} \\ i_{C0} = i_{Lf} - i_{L3} - i_o \end{cases} \quad (6)$$

where i_{Lf} is the current of inductor Lf.

2.2. Voltage in Capacitors and Current in Inductors

In order to simplify calculation, we suppose that the value of inductor L1 is equal to the value of inductor L2, similarly, we suppose the value of capacitor C1 is equal to capacitor C2. At the same time, all passive components are ideal. Then, based on the volt-second balance principle, the voltage of capacitors and the current of inductors can be expressed easily as follows:

$$\begin{cases} \frac{V_{C1}}{V_{in}} = \frac{V_{C2}}{V_{in}} = \frac{1-D_2}{1-D_1} \\ \frac{V_{C3}}{V_{in}} = 1 \\ \frac{V_o}{V_{in}} = \frac{D_1+2D_2-2}{1-D_1} \end{cases} \quad (7)$$

$$\begin{cases} i_{L1} = i_{L2} = i_o \\ i_{L3} = -i_o \\ i_{Lf} = \frac{2-D_1-2D_2}{D_1-1} i_o \end{cases} \quad (8)$$

where D_1 is the duty cycle of switch S1, D_2 is the duty cycle of switch S2, and I_o is the output current.

2.3. Design of Inductors

According to mode I, the input inductor L_f is magnetized by input voltage, so the current ripple of inductor L_f can be calculated by combining the equations in mode I with the expression of inductor voltage, $V_L = L di_L / dt$. The equation of the current ripple of inductor L_f is shown as follows:

$$\Delta i_{L_f} = \frac{V_{in} D_1 T_s}{L_f}, \quad (9)$$

where Δi_{L_f} is the current ripple of inductor L_f and T_s denotes the switching period. Δi_{L_f} is related to the input voltage V_{in} , duty cycle D_1 , switching frequency, and the value of inductor L_f .

Then, according to Equation (9), inductor L_f can be calculated as follows:

$$L_f = \frac{V_{in} D_1 T_s}{\Delta i_{L_f}}. \quad (10)$$

Similarly, inductors $L1$ and $L2$ are related to D_2 . Then, combining Equation (7), inductors $L1$ and $L2$ can be calculated as follows:

$$L1 = L2 = \frac{V_{C1} D_2 T_s}{\Delta i_{L1}} = \frac{V_{in} (1 - D_2) D_2 T_s}{\Delta i_{L1} (1 - D_1)}, \quad (11)$$

where Δi_{L1} denotes the current ripple of inductor $L1$.

At the same time, by combining Equation (8), inductor $L3$ can be expressed as follows:

$$L3 = \frac{V_{C3} D_1 T_s}{\Delta i_{L3}} = \frac{V_{in} D_1 T_s}{\Delta i_{L3}}, \quad (12)$$

where Δi_{L3} denotes the current ripple of inductor $L3$.

2.4. Design of Capacitors

According to the above calculations of the inductors, the voltage ripple of the capacitor C1 is affected by the current of inductor $L1$, the duty cycle of switch S2, switching frequency, and the value of C1. Therefore, the same principle is applied to capacitors and, based on $i_c = C dV_c / dt$, the value of capacitors can be calculated as follows:

$$C1 = C2 = \frac{i_{L1} (1 - D_2) T_s}{\Delta V_{C2}}, \quad (13)$$

where ΔV_{C2} is the voltage ripple of capacitor C2.

As for the value of capacitor C3, it is associated with the current of inductor $L3$. The equation is shown as follows:

$$C3 = \frac{i_{L3} (1 - D_2) T_s}{\Delta V_{C3}}, \quad (14)$$

where ΔV_{C3} is the voltage ripple of capacitor C3.

Finally, the value of output capacitor C0 can be calculated as follows:

$$C0 = \frac{2I_o D_3 T_s}{\Delta V_{C0}}, \quad (15)$$

where ΔV_{C0} is the voltage ripple of capacitor C0.

2.5. Peak Voltage and Current in Switches and Analysis

According to Figure 2 and Equations (1), (2), (7) and (8), the peak voltage and current of switches can be concluded as follows:

$$V_{S-\max} = (1 + k)V_{in}, \quad (16)$$

$$I_{S-\max} = (A + 1)I_o, \quad (17)$$

where $V_{S-\max}$ and $I_{S-\max}$ are the maximum voltage stresses and current stresses, respectively. k and A represent maximum boost ratio and voltage gain, respectively. I_o is the output current, which can be expressed as follows:

$$I_o = I_m \sin \omega t, \quad (18)$$

where I_m is the maximum output current.

3. Control Method

The expression of the duty cycle, key waveforms, and control diagram are displayed in this section. At the same time, the implementation of control in MATLAB is also shown.

3.1. Expression of Duty Cycle

The output voltage of the SEPIC-based TSTS Z-source inverter is defined as follows:

$$v_o = V_o \sin \omega t = AV_{in} \sin \omega t, \quad (19)$$

where A , or the peak voltage gain, is defined as $A = V_o / V_{in}$ and the maximum output voltage is V_o .

Regarding boost, D_1 is set as a constant value and k as the maximum boost ratio, defined as follows [20]:

$$k = \frac{D_1}{1 - D_1} \Rightarrow D_1 = \frac{k}{1 + k}. \quad (20)$$

Regarding the inversion part, the sinusoidal output voltage, v_o , is generated by D_2 as a varied sinusoidal value. D_3 can be written from D_1 and D_2 , and they are defined as follows [20]:

$$D_2 = \frac{k + 2}{2(k + 1)} - \frac{A}{2(k + 1)} \sin \omega t, \quad (21)$$

$$D_3 = 2 - D_1 - D_2. \quad (22)$$

3.2. Key Waveforms in the Switching Cycle and Analysis

According to the above analysis, it is easy to get the key theoretical waveforms of the proposed topology, as shown in Figure 3. The values v_{gs1} , v_{gs2} , and v_{gs3} are the switching statuses of switches S1, S2, and S3, respectively. The values V_{s1} , V_{s2} , and V_{s3} are the voltages of switches S1, S2, and S3. When the switch is turned on, the voltage of the switch will be equal to zero. In contrast, there will be voltage in the switch when it is turned off and the value of voltage is equal to $V_{in}(1 + k)$, based on Equation (16). Furthermore, V_{Lf} , V_{L1} , and V_{L3} are the voltages of inductors L_f , $L1$, and $L3$, respectively. According to the operation modes in Figure 2, when D_1 is at a high level, L_f is magnetized by V_{in} , so $V_{Lf} = V_{in}$. When D_1 is at a low level, according to the loop analysis, $V_{Lf} = V_{in} - V_{s1}$. As for V_{L1} and V_{L3} , the same analysis method is applied and the value is shown in Figure 3. Similarly, i_{Lf} , i_{L1} , and i_{L3} represent the inductors' currents and they are changed following their voltage.

Figure 3. Key waveforms in one switching period.

3.3. Control Diagram

Figure 4 shows the control diagram of the proposed inverter. The result of Equation (20) is a constant, it is then compared with the carrier signal to produce the switch S1 pulse, which is used to boost the input voltage. However, the result of Equation (21) is a sinusoidal variable. The driven signal of switch S2 is generated by comparing the resulting varying duty cycle with the carrier signal, which generates a sinusoidal output. According to the operation modes, only two switches are turned on at the same time. Therefore, the pulse of switch S3 can be determined by the driven signal of switches S1 and S2. The pulse of switch S3 is obtained by the XOR gate. Through the XOR gate, it is guaranteed that only two switches are turned on at a time.

Figure 4. Control block diagram of the proposed inverter.

4. Simulation and Experimental Results

The simulation and experimental results of the proposed inverter are displayed in this section.

4.1. Simulation Results

The proposed inverter, under resistive load, was simulated in MATLAB/Simulink, assuming the current ripple of all inductors was calculated by $\Delta i_L = 20\%I_L$. Similarly, $\Delta V_C = 7\%V_C$ was used to calculate the voltage ripple of all capacitors. Therefore, based on Equations (7)–(15), the value of inductors and capacitors could be calculated as shown in Table 1. Considering the laboratory conditions, in order to experiment conveniently, the switches were IGBT and the switching frequency, f_s , was 20 kHz. The output of the simulation was 124 V, 50 Hz under the condition of 100 V input voltage.

Table 1. Parameters selected for the inverter simulation.

Parameters	V_{in} (V)	V_o (rms, V)	f_s (kHz)	A (Voltage Gain)	k	$L3$ (mH)	Lf (mH)	$L1, L2$ (mH)	$C0$ (μ F)	$C1, C2$ (μ F)	$C3$ (μ F)
value	100	124	20	1.75	2	1.5	0.5	1.65	37.6	15	9

Figure 5 shows the key waveforms of the proposed inverter in MATLAB/Simulink. Figure 6 shows the output voltage, output current, and Fast Fourier transform (FFT) analysis of the proposed inverter. The voltage of the capacitors is shown in Figure 7. Additionally, to better test the proposed inverter the output results of the proposed inverter are displayed in Figure 8, under the condition that the load changed suddenly.

Based on the above results, the simulation results verified the theoretical analysis. According to Figure 5, the key waveforms were consistent with the theoretical waveforms shown in Figure 3 and, at the same time, the values of the voltage satisfied the theoretical calculation. The output voltage satisfied the voltage gain and the voltage of the switches was about 300 V, which is consistent with Equation (16). Similarly, Figure 7 demonstrates Equation (7). Furthermore, the THD = 1.48%, which is well below 5%. According to Figure 8 it still worked normally, although there will be fluctuations and harmonics in the process of change. In summary, the proposed inverter can operate with satisfying performance under complex conditions.

Figure 5. Cont.

Figure 5. Cont.

Figure 5. Key waveforms of the proposed inverter in MATLAB.

Figure 6. Cont.

(b)

(c)

(d)

(e)

Figure 6. Input voltage at 100 V and load at 30 Ω for SEPIC-based ZSI: (a) load voltage, (b) load current, (c) Fast Fourier transform (FFT) analysis, (d) output voltage with inductive load, and (e) output current with inductive load.

(a)

(b)

(c)

(d)

Figure 7. Input voltage at 100 V and load at $30\ \Omega$ for SEPIC-based ZSI. Voltage wave of (a) capacitor C1, (b) capacitor C2, (c) capacitor C3, and (d) capacitor C0.

Figure 8. Input voltage at 100 V and load changed (30–10–30 Ω) for SEPIC-based ZSI: (a) load voltage and (b) load current.

4.2. Experimental Results

The corresponding experiments were also done. The IGBT, named K40T1202 IGBT, was used for each switch in the experiment. The experimental key waveforms are shown in Figure 9. Figure 10 shows the experimental results of output voltage and output current, which correspond with Figure 6. Similarly, Figure 11 shows the experimental results of the voltage of capacitors. The experimental output waveforms of half load changed to full load and full load changed to half load are shown in Figure 12. Furthermore, in order to verify that the proposed inverter can suppress the leakage current well, a capacitor with the value of 0.15 μF was used for C_{PV} . Figure 13 shows the experimental waveform of the leakage current.

Figure 9. Cont.

Figure 9. Experimental waveforms: (a) driven signal of the switches; (b) the voltage of switch S1 (CH1: Time (10 μ s/div), V_{s1} (50 V/div)); (c) the voltage of switch S2 (CH2: Time (10 μ s/div), V_{s2} (50 V/div)); (d) the voltage of switch S3 (CH3: Time (10 μ s/div), V_{s3} (50 V/div)); (e) the voltage and current of inductor L_f (CH1: Time (10 μ s/div), V_{L_f} (50 V/div), CH2: Time (10 μ s/div), i_{L_f} (5 A/div)); (f) the voltage and current of inductor L_1 (CH1: Time (10 μ s/div), V_{L_1} (50 V/div), CH2: Time (10 μ s/div), i_{L_1} (5 A/div)); and (g) the voltage and current of inductor L_3 (CH1: Time (10 μ s/div), V_{L_3} (50 V/div), CH2: Time (10 μ s/div), i_{L_3} (5 A/div)).

The experimental waveforms in Figure 9 prove the theoretical key waveforms in Figure 3 and the simulation waveforms in Figure 5. Since the switches in the simulation were ideal and the experimental switches were not ideal, there are voltage spikes in Figure 9. The output voltage and current satisfied the analysis and simulation results. Furthermore, it can be seen from Figure 12 that the proposed inverter still worked well when the load changed suddenly. According to Table II in [24], compared to the traditional single-phase H4 inverter with UPWM and BPWM, the HERIC and H5 topology has

lower leakage current. According to the experimental results of the HERIC topology, the max value of leakage current was more than 100 mA under the output power of 160 W. However, the leakage current of the proposed inverter was only about 48 mA under the output power of 500 W which had a good performance for eliminating leakage current and benefited from the dual-grounding.

Figure 10. Input voltage at 100 V and load at 30 Ω . Experimental waveforms of v_o (CH1: Time (5 ms/div), v_o (50 V/div)) and I_o (CH2: Time (5 ms/div), I_o (5 A/div)).

(a)

(b)

Figure 11. Input voltage at 100 V and load at 30 Ω . Experimental waveforms of (a) V_{c1} (CH1: Time (5 ms/div), V_{c1} (50 V/div)) and V_{c2} (CH2: Time (5 ms/div), V_{c2} (50 V/div)); (b) V_{c3} (CH3: Time (5 ms/div), V_{c3} (50 V/div)) and V_{c0} (CH4: Time (5 ms/div), V_{c0} (50 V/div)).

(a)

(b)

Figure 12. Input voltage at 100 V and sudden load changes: (a) from 60 to 30 Ω , (b) from 30 to 60 Ω . Experimental waveforms of v_o (CH1: Time (5 ms/div), v_o (50 V/div)) and I_o (CH2: Time (5 ms/div), I_o (5 A/div)).

Figure 13. The waveform of leakage current (CH2: I (50 mA/div)).

Table 2 shows the efficiency of the proposed inverter. However, the efficiency of this topology was relatively low due to the use of IGBT as the switches, which are not appropriate for low–medium power converters, and the limitation of the laboratory conditions. A good device can be used to enhance the efficiency of the proposed topology.

Table 2. The measured efficiency of the proposed inverter.

Output power (W)	120	204.5	311	358	431
Efficiency (%)	89.9	90.08	91.17	91.70	89.58

In conclusion, from the above experimental results, it can be observed that the experimental results were in good agreement with the theoretical analysis and the simulation results, again verifying the effectiveness of the proposed inverter.

4.3. Comparison

In conclusion, the existing Z-source-based inverter topologies have some of the following disadvantages: complex control techniques [25–27], high semiconductor device counts [28,29], high numbers of capacitors and inductors [30], ripples in the capacitor voltage and inductor current [31–33], unsatisfactory voltage gain [34], and leakage current [35]. Table 3 shows the characteristics of different Z-source inverters. In addition, a transformer [36,37] is used to boost input voltage and isolate input and output, which will increase the cost, weight, and volume of the inverter. So, the inverter with a common ground can deal well with these problems.

Table 3. Comparison between different Z-source inverters. EMI: electromagnetic interference.

	L	C	D	S	Control Method	Voltage Gain	Common Ground	EMI	Soft Switch
Semi-ZSI [25]	2	2	0	2	nonlinear	<1	Yes	high	complex
Semi-ZS-based [34]	3	3	0	2	linear	<1	Yes	high	complex
Basic SBI [35]	1	1	2	2	linear	>1	No	high	complex
Embedded-type qSBI [35]	1	1	2	2	linear	>1	No	high	complex
DC-linked-type qSBI [35]	1	1	2	2	linear	>1	No	high	complex
CUK-based ZSI [22]	4	4	0	3	linear	>1	Yes	low	complex
Boost-based ZSI [20]	3	3	0	3	linear	>1	Yes	high	complex
Buck–boost-based [20]	3	3	0	3	linear	>1	Yes	high	complex
Proposed in [23]	4	4	0	3	linear	>1	Yes	low	simple

In Table 3, it is easy to see that the CUK converter has low input current ripple and output current ripple, and the SEPIC converter has low input current ripple, so both CUK-based ZSI and SEPIC-based ZSI have low electromagnetic interference (EMI) [38]. Furthermore, SEPIC has the possibility of a series of resonant operations between the balancing capacitor and the parallel inductor, which can be beneficial for a soft-switching operation [39]. Therefore, SEPIC-based ZSI makes it easy to achieve a soft-switching operation.

5. Conclusions

A novel SEPIC-based Z-source inverter that eliminates leakage current is proposed in this paper. The feature of the proposed topology is a combination of a Z-source inverter and a SEPIC converter, so the current inverter has the advantages of both a SEPIC converter and a Z-source inverter, which has a high voltage gain. Furthermore, the proposed inverter is controlled by a simple linear control method, which is easy to achieve, and the proposed inverter has a low voltage stress in the switch, which is beneficial for choosing switches. Furthermore, compared with traditional single-phase H4, H5, and HERIC topologies, the proposed topology has features including fewer switches and very low leakage current, which is helpful for the application of transformerless inverters. However, the proposed topology also has the merits of the SEPIC converter. It can be seen in Figures 6 and 10 that the proposed inverter has large output harmonics, due to the lack of a filter inductor. The simulation results verified the theoretical analysis. Furthermore, experiments with a laboratory prototype, using a DSP controller combined with FPGA, showed good results that were in agreement with the simulation results. The future research direction will be to study new control methods to reduce the output harmonics.

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Abbreviations

The following abbreviations are used in this manuscript:

Acronyms

ZSI	Z-source inverter
VSI	Voltage source inverter
TSTS	Three-switch three-state
FFT	Fast Fourier transform
THD	Total harmonic distortion
SBI	Switched Boost Inverters
QSBI	Quasi-Switched Boost Inverters
UPWM	Unipolar Pulse Width Modulation
BPWM	Bipolar Pulse Width Modulation
HERIC	Highly Efficient Reliable Inverter Concept
IGBT	Insulated Gate Bipolar Transistor
SEPIC	Single Ended Primary Inductor Converter

Nomenclature

A	Peak voltage gain
k	Maximum boost ratio
D_1, D_2, D_3	Duty cycle functions
ω	Output voltage angular frequency
$S1, S2, S3$	Semiconductor switches
V_{in}	DC input voltage
V_{Li}	Voltage of inductors
V_{Ci}	Voltage of capacitors
V_{si}	Voltage of switches
i_{Li}	Current of inductors
i_{Ci}	Current of capacitors
I_o	Output peak current
Δi_{Li}	Current ripple of inductors
ΔV_{Ci}	Voltage ripple of capacitors
T_s	Switching period
f_s	Switching frequency
EMI	Electromagnetic Interference

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