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Voltage Multiplier Cell-Based Quasi-Switched Boost Inverter with Low Input Current Ripple

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Abstract: A novel single-phase single-stage voltage multiplier cell-based quasi-switched boost inverter (VMC-qSBI) is proposed in this paper. By adding the voltage multiplier cell to the qSBI, the proposed VMC-qSBI has the following merits; a decreased voltage stress on an additional switch, a high voltage gain, a continuous input current, shoot through immunity, and a high modulation index. A new pulse-width modulation (PWM) control strategy is presented for the proposed inverter to reduce the input current ripple. To improve the voltage gain of the proposed inverter, an extension is addressed by adding the VMCs. The operating principle, steady-state analysis, and impedance parameter design guideline of the proposed inverter are presented. A comparison between the proposed inverter and other impedance source-based high-voltage gain inverters is shown. Simulation and experimental results are provided to confirm the theoretical analysis.

Keywords: input current ripple; voltage multiplier; shoot through state; quasi-switched boost inverter; Z-source inverter

1. Introduction

In recent years, many dc–ac power conversion topologies have attracted the interest of researchers for various applications, such as ac motor drives, uninterruptible power supplies, hybrid electric vehicles, and renewable energy systems [1]. Voltage source inverters (VSIs) and current source inverters (CSIs) are two basic dc–ac power conversion devices. In [2], the design of a single-phase photovoltaic VSI model and the simulation of its performance were presented. Two problems associated with VSIs are that the output voltage cannot exceed the input dc voltage, and both power switches in the same leg cannot be simultaneously turned on. Similarly, the output voltage of CSIs cannot be lower than the source voltage, and both power switches in the same leg cannot be turned off at the same time.

To solve these problems associated with VSIs and CSIs, impedance source inverters [3–10] have been proposed. The classical Z-source inverter (ZSI) uses two inductors and two capacitors in the impedance source network to step-up/down the input voltage. In order to improve the discontinuous input current disadvantage of the ZSI, a class of quasi-ZSIs (qZSIs) was proposed in [3]. Nevertheless, with ZS/qZSIs, it is very difficult to achieve a high voltage gain owing to the limitation of the modulation index and the shoot through (ST) duty cycle. The voltage gain in the ZS/qZSIs can be improved by adding an inductor, capacitor, and diode to the impedance source network, as presented in the continuous/ripple input current switched-inductor (SL) qZSIs [5,6], the enhanced-boost qZSI [7], and the modified switched-capacitor ZSI [8]. However, passive element-based qZSIs [4–8] increase the volume and loss of the power inverter because of the use of a large number of passive components. Coupled-inductor-based qZSIs [9] can reduce the size of the inverter, but the coupled inductor must

be well designed to avoid voltage spikes on the dc-bus. A current ripple damping control scheme for single-phase quasi-Z-source system was introduced in [10] to minimize passive elements in the impedance source network.

To decrease the volume and loss of the power inverter, active impedance source inverters have been recently proposed in [11–20]. The switched boost inverter (SBI) [11] uses fewer passive elements and more semiconductors to produce a smaller voltage gain than ZSIs. A family of quasi-switched boost inverters (qSBIs) was presented in [12] to overcome the disadvantages of the SBI. Compared with the qZSI, the qSBI in [12] produces the same voltage gain. In [13], the qSBI was compared with the qZSI in terms of size, loss, and voltage/current ripple on passive elements. Similar to the ZSIs, passive elements, including the capacitor, inductor, coupled inductor, and diode, were also added to the qSBIs to increase the voltage gain. For instance, the topologies in [14–16] were introduced by applying the SL structure to the switched-boost network. In [17], a high-voltage gain switched-ZSI (SZSI) was introduced by using one more inductor, one more capacitor, and two more diodes when compared with the qSBI. To reduce the voltage stress on the capacitor, diode, and switch of the impedance-source network, a high voltage gain qSBI was proposed in [18]. An active switched-capacitor qZSI (ASC-qZSI) was proposed in [19], where only one inductor and one capacitor were added to the qSBI to obtain the same voltage gain as the SZSI. Coupled-inductor-based qSBIs were also presented in [20], with a spike generated on the dc-bus voltage owing to the effect of the leakage inductance in the coupled inductor. To enhance the performance of the qSBIs, a family of PWM control strategies for a single-phase qSBIs has been introduced in [21]. Because the additional states are inserted in the extra switch, the switching loss of the qSBIs under these PWM control methods is increased. A control-based approach to suppress the low-frequency harmonic component in the input inductor current of the single-phase qSBI has been presented in [22]. Even though the active impedance source inverters in [11–22] have good performance, where there is a reduced volume and loss with a high voltage gain, the voltage stress on the additional switch is very high because it equals the dc-bus voltage. To decrease the voltage stress on devices, switched-capacitor qSBIs were investigated in [23].

A voltage multiplier cell (VMC) is used in the dc–dc power conversion process [24–26] to provide a high voltage gain and reduce the voltage stress on semiconductor devices. In [27], the pulsating dc voltage is rectified by the voltage multiplier to boost the output voltage without using magnetic elements. In this study, the VMC is applied to the qSBI to achieve a high dc–ac voltage gain with a high modulation index. Compared with other active impedance source inverters, the voltage stress on the extra switch is reduced significantly. A new PWM control method is presented for the proposed inverter to reduce the input current ripple. By adding the VMC, the proposed inverter can extend to n-cells in order to achieve a high voltage gain requirement. Because of the advantages of the proposed solution, the proposed inverter can replace the qZSI for the photovoltaic generator applications where a low dc voltage needs to invert into a high grid-connected ac voltage. Section 2 proposes the inverter with the operating principle, PWM control technique, and steady-state analysis. The design of the proposed inverter is presented in Section 3. A comparison with other high voltage gain qZS/qSBIs is made in Section 4, while simulation and experimental results are shown in Section 5.

2. Proposed Inverter Topologies

The single-phase qSBI with a continuous input current [12] is presented in Figure 1a. It includes one boost inductor (L_B), one capacitor (C_0), six diodes (D_a, D_0, and four body diodes in the H-bridge circuit), five active switches (S_1–S_5), a passive filter (L_f and C_f), and a resistive load (R). The qSBI uses the ST mode to step-up the input voltage. The following formulas of the qSBI are obtained as given in [12].

$$\begin{cases} V_{PN} = V_{S5} = \frac{1}{1-2D_{ST}} V_{dc} = B \cdot V_{dc} \\ \hat{v}_o = M \cdot B \cdot V_{dc} = \frac{M}{1-2D_{ST}} V_{dc}, \end{cases} \quad (1)$$

where V_{PN}, V_{S5}, $\hat{v}_o$, B, M, and D_{ST} are the dc-bus voltage, the voltage stress on the additional switch S_5, the amplitude of the output voltage, the boost factor, the modulation index, and the ST duty cycle, respectively.

From Equation (1), it can be seen that the voltage gain of the qSBI is low because $D_{ST} \leq (1–M)$. Moreover, the voltage stress on the additional switch S_5 is high because it equals the dc-link voltage. Therefore, the qSBI is not suitable for high voltage gain applications.

Figure 1b shows the proposed single-phase VMC-qSBI with a single VMC, where two capacitors (C_{11} and C_{12}) and two diodes (D_{11} and D_{12}) are added to the switched-boost network. The proposed single-VMC-qSBI uses one boost inductor (L_B), three capacitors (C_0, C_{11}, and C_{12}), eight diodes (D_a, D_0, D_{11}, D_{12}, and four body diodes in the H-bridge circuit), five active switches (S_1–S_5), a passive filter (L_f and C_f), and a resistive load (R). A combination of C_{11}–C_{12}–D_{11}–D_{12}–S_5 plays a role as a VMC. It should be noted that the proposed single-VMC-qSBI will become the 2-cell SC-qSBI in [23] if the negative node of C_0 is connected to the positive node of C_{11} in Figure 1b. Like other VMC-based converters, the proposed inverter has high current transients of the capacitor across S_5, D_{11}, D_{12}, and D_0. To reduce the current transients of capacitors and achieve soft-switching operation, a resonant inductor can be used, as reported in [24] and [25]. Figure 1c shows an n-cell extension of the proposed VMC-qSBI. Each VMC, including two capacitors and two diodes, is connected in cascade to obtain an n-cell topology. When $n > 1$, a multiple of two capacitors and two diodes is added to the proposed inverter. Consequently, the size, weight, and loss of the proposed inverter are increased. Note that, a three-phase H-bridge circuit can be used in the proposed converter for the three-phase inverter system.

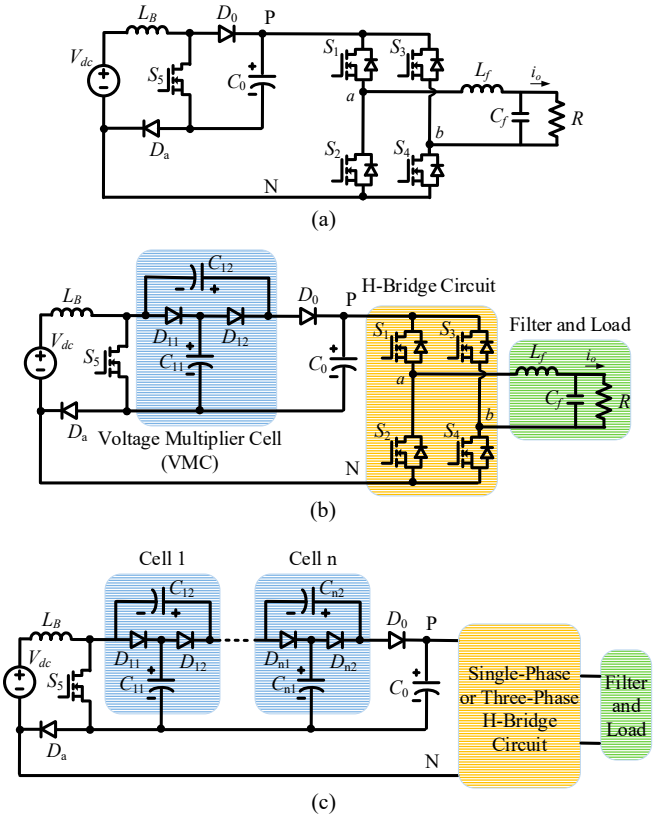


Figure 1. Conventional and proposed inverter topologies. (**a**) Conventional quasi-switched boost inverter (qSBI), (**b**) proposed single voltage multiplier cell (VMC-qSBI), and (**c**) proposed n-VMC-qSBI extension topologies.

2.1. Operating States

As an example, the operating principle and steady-state analysis of the proposed single-phase single-VMC-qSBI are presented in this paper. Figure 2 shows the three operating states of the proposed single-phase single-VMC-qSBI. In the non-ST states, as shown in Figure 2a,b, the H-bridge circuit and the load side are equivalent to a current source. When the switch S_5 is turned on, diodes D_{11} and D_0 are reversed-biased, while the diodes D_a and D_{12} are forward-biased. The inductor L_B and the capacitor C_{12} are charged, while the capacitors C_{11} and C_0 are discharged. The inverter operates in the non-ST state 1, as shown in Figure 2a. The time interval in the non-ST state 1 is $D_5 \cdot T$, where D_5 is the duty cycle of the switch S_5 during one switching period, T. The following equations can be written as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_{dc} \\ V_{C11} = V_{C12} \\ V_{PN} = V_{C0} \end{cases} \text{and} \begin{cases} C_{11} \frac{dv_{C11}}{dt} = -i_{C12\_Non1} \\ C_{12} \frac{dv_{C12}}{dt} = i_{C12\_Non1} \\ C_0 \frac{dv_{C0}}{dt} = -I_{PN}, \end{cases} \tag{2}$$

where I_{PN} and i_{C12_Non1} are the average dc-link current and the instantaneous current through capacitor C_{12} in the non-ST state 1.

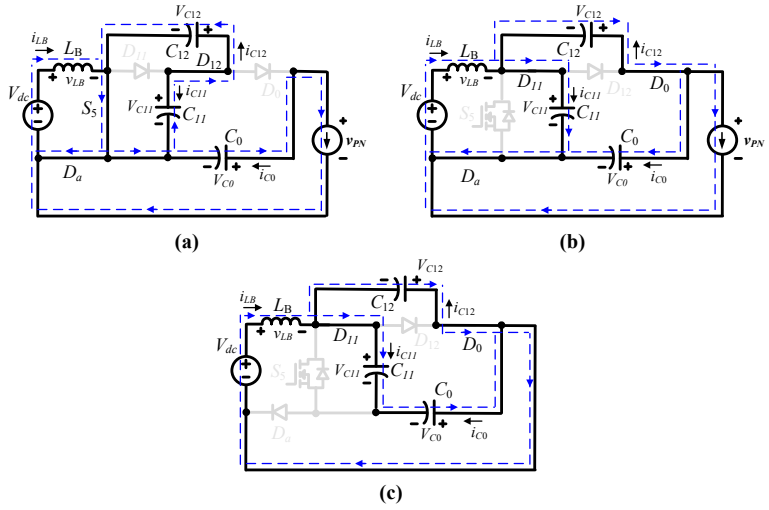


Figure 2. Operating states of proposed single-VMC-qSBI. (**a**) Non-ST state 1, (**b**) non-ST state 2, and (**c**) ST state.

When the switch S_5 is turned off and the H-bridge circuit generates the active or zero vectors and the inverter operates in the non-ST state 2, as shown in Figure 2b. During this state, diode D_{12} is reversed-biased, while the diodes D_a, D_{11}, and D_0 are forward-biased. Inductor L_B and capacitor C_{12} are discharged, while capacitors C_{11} and C_0 are charged. The following formulas can be obtained as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_{dc} - V_{C11} \\ V_{C0} = V_{PN} = V_{C11} + V_{C12} \end{cases} \text{and} \begin{cases} C_{11} \frac{dv_{C11}}{dt} = I_{LB} + i_{C12\_Non2} \\ C_{12} \frac{dv_{C12}}{dt} = i_{C12\_Non2} \\ C_0 \frac{dv_{C0}}{dt} = -I_{PN} - i_{C12\_Non2}, \end{cases} \tag{3}$$

where i_{C12_Non2} is the instantaneous current through capacitor C_{12} in the non-ST state 2.

In the ST state, as shown in Figure 2c, the H-bridge circuit is shorted by the switches on the same H-bridge leg. Meanwhile, switch S_5 is turned off during the ST state. Diodes D_{11} and D_0 are forward-biased, while diodes D_a and D_{12} are reversed-biased. The time interval is $D_{ST} \cdot T$. The inductor

L_B and capacitor C_{11} are charged, while the capacitors C_{12} and C_0 are discharged. The following equations can be obtained as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_{dc} + V_{C12} \\ V_{C0} = V_{C11} + V_{C12} \\ V_{PN} = 0 \end{cases} \text{ and } \begin{cases} C_{11} \frac{dv_{C11}}{dt} = I_{LB} + i_{C12\_ST} \\ C_{12} \frac{dv_{C12}}{dt} = i_{C12\_ST} \\ C_0 \frac{dv_{C0}}{dt} = -I_{LB} - i_{C12\_ST}, \end{cases} \quad (4)$$

where i_{C12_ST} is the instantaneous current through capacitor C_{12} in the ST state.

2.2. PWM Technique with Low Input Current Ripple

Figure 3 shows a PWM control technique for the proposed single-phase VMC-qSBI. As shown in Figure 3a, two sinusoidal voltages—v_{sin} and $-v_{sin}$—are compared to a high-frequency triangle waveform, v_{tri1}, to produce PWM signals for the H-bridge switches (S_1–S_4). A fixed voltage, V_5, is compared to the triangle waveform (v_{tri2}) with the double frequency of v_{tri1}, as shown in Figure 3, to produce the control signal for the switch S_5. To produce an ST control signal, another fixed voltage, V_{ST}, is also compared to v_{tri2}. This ST control signal (ST in Figure 3b) is then inserted into the H-bridge switches through OR logic gates.

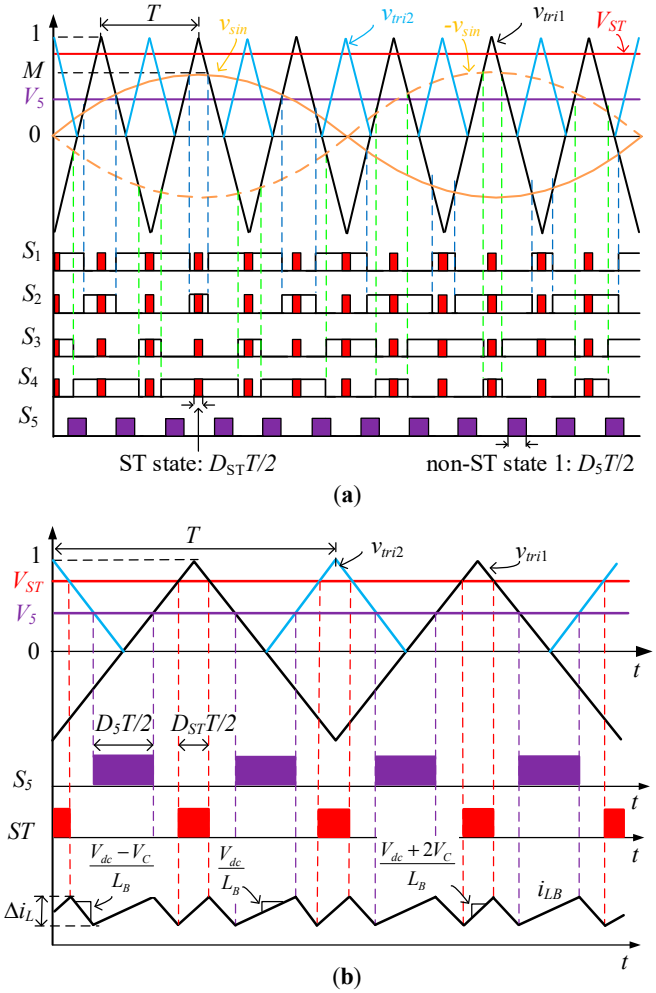


Figure 3. Pulse-width modulation (PWM) control technique for the proposed single-phase inverter. (**a**) Signal generation and (**b**) enlargement waveforms.

2.3. Steady-State Analysis

By using the volt-second balance to the inductor L_B, in steady-state, from Equations (2) to (4), the voltage on the capacitors is calculated as

$$\begin{cases} V_C = V_{C11} = V_{C12} = \frac{1}{1-2D_{ST}-D_5} V_{dc} \\ V_{C0} = 2V_C = \frac{2}{1-2D_{ST}-D_5} V_{dc}. \end{cases} \tag{5}$$

Applying the charge-second balance principle to the capacitors C_{11}, C_{12}, and C_0, from Equations (2) to (4), the following equations are obtained as Equation (6).

$$\begin{cases} -D_5 i_{C12\_Non1} + (1 - D_{ST} - D_5) i_{C12\_Non2} + D_{ST} i_{C12\_ST} + (1 - D_5) I_{LB} = 0 \\ D_5 i_{C12\_Non1} + (1 - D_{ST} - D_5) i_{C12\_Non2} + D_{ST} i_{C12\_ST} = 0 \\ -(1 - D_{ST} - D_5) i_{C12\_Non2} - D_{ST} i_{C12\_ST} - D_{ST} I_{LB} - (1 - D_{ST}) I_{PN} = 0. \end{cases} \tag{6}$$

Solving Equation (6), the instantaneous current through capacitor C_{12} in the non-ST state 1 and the average inductor L_1 current are given as

$$\begin{cases} i_{C12\_Non1} = \frac{1-D_5}{2D_5} I_{LB} \\ I_{LB} = \frac{2(1-D_{ST})}{1-2D_{ST}-D_5} I_{PN}. \end{cases} \tag{7}$$

The inductor is charged during both non-ST state 1 and ST state. From Equations (2) and (4), the inductor current ripple can be rewritten as follows.

$$\begin{cases} \Delta I_{L\_NST1} = \frac{V_{dc}}{L_B} \frac{D_5 T}{2} \\ \Delta I_{L\_ST} = \frac{V_{dc}+V_C}{L_B} \frac{D_{ST} T}{2}. \end{cases} \tag{8}$$

From Equation (8), it can be seen that the slope of the inductor current in the ST state is higher than that in the non-ST state 1. The inductor current ripple depends on the ST duty cycle. Further, the inductance selection is based on the maximum ST duty cycle. If we select $D_5 = D_{ST}$ or $2D_{ST}$, the high-frequency (HF) inductor current ripple is too high, and the voltage gain of the inverter is not high at a high modulation index. In this paper, we select $D_5 = 3D_{ST}$ to obtain a low inductor current ripple with a high voltage gain. Substituting $D_5 = 3D_{ST}$ in to Equation (5), the peak dc-link voltage in the non-ST states is

$$V_{PN} = V_{C0} = 2V_C = \frac{2}{1 - 5D_{ST}} V_{dc}. \tag{9}$$

The boost factor of the proposed VMC-qSBI is calculated as

$$B = \frac{V_{PN}}{V_{dc}} = \frac{2}{1 - 5D_{ST}}. \tag{10}$$

The peak ac voltage is defined as

$$\hat{v}_o = M \cdot B \cdot V_{dc} = \frac{2M}{1 - 5D_{ST}} V_{dc}. \tag{11}$$

For the proposed n-cell VMC-qSBI, as shown in Figure 1c, the capacitor voltage is determined in the steady-state as

$$\begin{cases} V_C = V_{C11} = V_{Cn2} = \frac{V_{dc}}{1-(n+1)D_{ST}-D_5} \\ V_{Cn1} = nV_C \\ V_{C0} = (n+1)V_C = \frac{(n+1)V_{dc}}{1-(n+1)D_{ST}-D_5}. \end{cases} \tag{12}$$

The peak ac voltage of the n-cell VMC-qSBI is expressed as

$$\hat{v}_o = \frac{(n+1)M}{1-(n+1)D_{ST}-D_5} V_{dc}. \tag{13}$$

3. Parameter Design Guideline

For the single-phase inverter, there will be a pulsating power at double the fundamental frequency, which will pose a significant challenge to the front-end boost converter. Similar to other single-phase inverter topologies, the proposed single-phase VMC-qSBI also generates the double fundamental frequency ripple at the dc side. The double fundamental frequency ripple on the inductors and capacitors at the dc side can be mitigated by using a feedback control method, as reported in [10] for qZSI and [22] for qSBI. Therefore, in this study, the effect of the pulsating power can be ignored in the design stage. Then, the inductance and capacitance are only selected according to the HF ripple. The ac side circuit of the proposed VMC-qSBI is described by its equivalent dc load [12]. The average dc-link current depends on the equivalent dc load (R_l), and is calculated as [12]

$$I_{PN} = \frac{(1-D_{ST})V_{PN}}{R_l}. \tag{14}$$

3.1. Parameter Design of Inductor

The inductor current waveform of the proposed VMC-qSBI is shown in Figure 3b. The peak-to-peak current ripple of the inductor L_B is calculated as Equation (8). To limit the peak-to-peak inductor current ripple by $r_{LB}\%\cdot I_{LB}$, the inductance of L_1 should be

$$L_1 > \frac{3D_{ST}(1-5D_{ST})^2 R_l}{8r_{LB}\%(1-D_{ST})^2 f}, \tag{15}$$

where $f = 1/T$ is the switching frequency of the inverter.

3.2. Parameter Design of Capacitor

To select the C_{11}, C_{12}, and C_0 capacitances of the proposed VMC-qSBI, the peak-to-peak capacitor voltage ripples can be rewritten from Equation (2) as

$$\begin{cases} \Delta V_{C11} = \frac{-i_{C12\_non1}}{C_{11}} \cdot \frac{D_5 T}{2} \\ \Delta V_{C12} = \frac{i_{C12\_non1}}{C_{12}} \cdot \frac{D_5 T}{2} \\ \Delta V_{C0} = \frac{I_{PN}}{C_0} \cdot \frac{D_5 T}{2}, \end{cases} \tag{16}$$

Substituting Equations (6) and (14) into Equation (16), the C_{11}, C_{12}, and C_0 capacitances of the proposed VMC-qSBI are calculated as

$$\begin{cases} C_{11} = C_{12} = \frac{2(1-3D_{ST})(1-D_{ST})^2}{r_{C1}\%(1-5D_{ST})R_l f} \\ C_0 = \frac{3D_{ST}(1-D_{ST})}{2r_{C0}\%R_l f}, \end{cases} \tag{17}$$

where $r_{C1}\%$ and $r_{C0}\%$ are the voltage ripple percentages of capacitors C_{11} and C_{12} and capacitor C_0, respectively.

3.3. Parameter Design of Switches

From Figure 3, the voltage stress of the diodes is calculated as

$$\begin{cases} V_{S1-S4} = V_{C0} = \frac{2V_{dc}}{1-5D_{ST}} \\ V_{S5} = V_{C11} = \frac{V_{dc}}{1-5D_{ST}}. \end{cases} \tag{18}$$

Because the ST state turns on all of the H-bridge switches S_1–S_4, as shown in Figure 2c, the peak current of switches S_1–S_4 equals a half of the ST current, which is the inductor current. Consequently, the current stress of the switches S_1–S_4 is

$$I_{S1-S4} = \frac{I_{LB}}{2} = \frac{2(1-D_{ST})^2}{(1-5D_{ST})^2}\frac{V_{dc}}{R_l}. \tag{19}$$

The peak current of switch S_5 is determined based on the non-ST state 1 in Figure 2a as

$$I_{S5} = I_{LB} + i_{C12\_Non1} = \frac{2(1+3D_{ST})(1-D_{ST})^2}{3D_{ST}(1-5D_{ST})^2}\frac{V_{dc}}{R_l}. \tag{20}$$

3.4. Parameter Design of Diodes

From Figure 2, the voltage stress of the switches is calculated as

$$\begin{cases} V_{D0} = V_{D11} = V_{D12} = V_{C11} = \frac{V_{dc}}{1-5D_{ST}} \\ V_{Da} = V_{C0} = \frac{2V_{dc}}{1-5D_{ST}}. \end{cases} \tag{21}$$

The peak current of the diodes D_0, D_{11}, and D_a should be selected such that it equals the inductor L_B current, and the peak current of the diode D_{12} equals the instantaneous current through capacitor C_{12} in the non-ST state 1. Therefore, the peak current of the diodes is calculated as

$$\begin{cases} I_{Da} = I_{D0} = I_{D11} = I_{LB} = \frac{4(1-D_{ST})^2}{(1-5D_{ST})^2}\frac{V_{dc}}{R_l} \\ I_{D12} = i_{C12\_Non1} = \frac{2(1-3D)(1-D_{ST})^2}{3D(1-5D_{ST})^2}\frac{V_{dc}}{R_l}. \end{cases} \tag{22}$$

4. Comparison with Other Active Impedance Source Inverters

In this section, the proposed VMC-qSBI is compared with other active impedance source inverters. The selected topologies for comparison are the qSBI [12], the SL-qSBI [14], the SZSI [17], ASC-qZSI [19], and 2-cell SC-qSBI [23]. Table 1 shows the overall comparison between the proposed VMC-qSBI and other active impedance source inverters.

4.1. Input Current Ripple

As shown in Table 1, the input current ripple of the SL-qSBI is very high because the input current is either the inductor current in the non-ST state or the twofold inductor current in the ST state. Note that as shown in Figure 3, the PWM control method cannot be applied to the SL-qSBI [13], ASC-qZSI [19], and 2-cell SC-qSBI [23] because of the increasing harmonic distortion of the output voltage. Therefore, the input current ripple of these inverters is high. Under the same PWM control method, as shown in Figure 3, the qSBI [11], SZSI [17], and the proposed inverter have a low input current ripple.

Table 1. Overall comparison of the proposed VMC-qSBI and other active impedance source inverters using the same PWM method.

	qSBI [12]	**SL-qSBI* [14]**	**SZSI [17]**	**ASC-qZSI* [19]**	**2-cell SC-qSBI* [23]**	**Single-VMC-qSBI**
Boost factor (B)	$\frac{1}{1-4D_{ST}}$	$\frac{1+D_{ST}}{1-3D_{ST}}$	$\frac{1}{1-5D_{ST}+D_{ST}^2}$	$\frac{1}{1-3D_{ST}+D_{ST}^2}$	$\frac{2}{1-3D_{ST}}$	$\frac{2}{1-5D_{ST}}$
Gain voltage (G)	$\frac{M}{4M-3}$	$\frac{2M-M^2}{3M-2}$	$\frac{M}{M^2+3M-3}$	$\frac{M}{M^2+M-1}$	$\frac{2M}{3M-2}$	$\frac{2M}{5M-4}$
Input current ripple	Low	Very high	Low	High	High	Low
I_{LB}/I_{PN}	$(1-D_{ST})B$	$(1-D_{ST})B/(1+D_{ST})$	$(1-D_{ST})B$	$(1-D_{ST})B$	$(1-D_{ST})B$	$(1-D_{ST})B$
I_{L2}/I_{PN}	NA	$(1-D_{ST})B/(1+D_{ST})$	$(1-D_{ST})^2B$	$(1-D_{ST})^2B$	NA	NA
I_{S5}/I_{PN}	$(1-D_{ST})B$	$\frac{2(1-D_{ST})B}{1+D_{ST}}$	$(1-D_{ST})B$	$(1-D_{ST})B$	$\frac{(1-D_{ST})}{D_{ST}(1-3D_{ST})}$	$\frac{(1-D_{ST})(1+3D_{ST})}{3D_{ST}(1-5D_{ST})}$
ST current (I_{sh}/I_{PN})	$(1-D_{ST})B$	$\frac{2(1-D_{ST})B}{1+D_{ST}}$	$(1-D_{ST})(2-D_{ST})B$	$(1-D_{ST})(2-D_{ST})B$	$(1-D_{ST})B$	$(1-D_{ST})B$
V_{C0}/V_{dc} and V_{Da}/V_{dc}	B	B	B	B	$B/2$	B
V_{C11}/V_{dc}	B	B	B	B	$B/2$	$B/2$
V_{C12}/V_{dc}	NA	NA	$D_{ST}B$	$(1-D_{ST})B$	$B/2$	$B/2$
V_{DS5}/V_{dc} and V_{D0}/V_{dc}	B	B	B	B	$B/2$	$B/2$
Switch	5	5	5	5	5	5
Diode	6	9	8	6	8	8
Inductor	1	2	2	2	1	1
Capacitor	1	1	2	2	3	3

where V_{DS5} is the drain-source voltage stress on S_5. *NA*: Not applicable; *Note that the PWM control method in Figure 3 cannot be applied to these inverters.

4.2. Voltage and Current Stresses

Figure 4 shows the respective ratios of the voltage stress to the equivalent dc voltage under the same PWM control method. As shown in Figure 4a, the voltage stress on capacitor C_0 and diode D_a of the proposed VMC-qSBI is higher than that of the 2-cell SC-qSBI. However, the voltage stress on switch S_5, capacitors C_{11} and C_0, and diodes D_0 and D_a of the proposed VMC-qSBI are smaller than that of the other active impedance source inverters, as shown in Figure 4a,b. The capacitor C_{12} voltage stress of the proposed VMC-qSBI is smaller than that of the ASC-qZSI and 2-cell SC-qSBI, but it is higher than that of SZSI.

The inductor current stress comparison is shown in Figure 5a. Because the qSBI, ASC-qSBI, 2-cell SC-qSBI, and the proposed VMC-qSBI have a single inductor, their inductor current stress is highest and is equal to the source current. Figure 5b shows the ST current stress comparison. The proposed VMC-qSBI, qSBI, and 2-cell SC-qSBI have the lowest ST current stress.

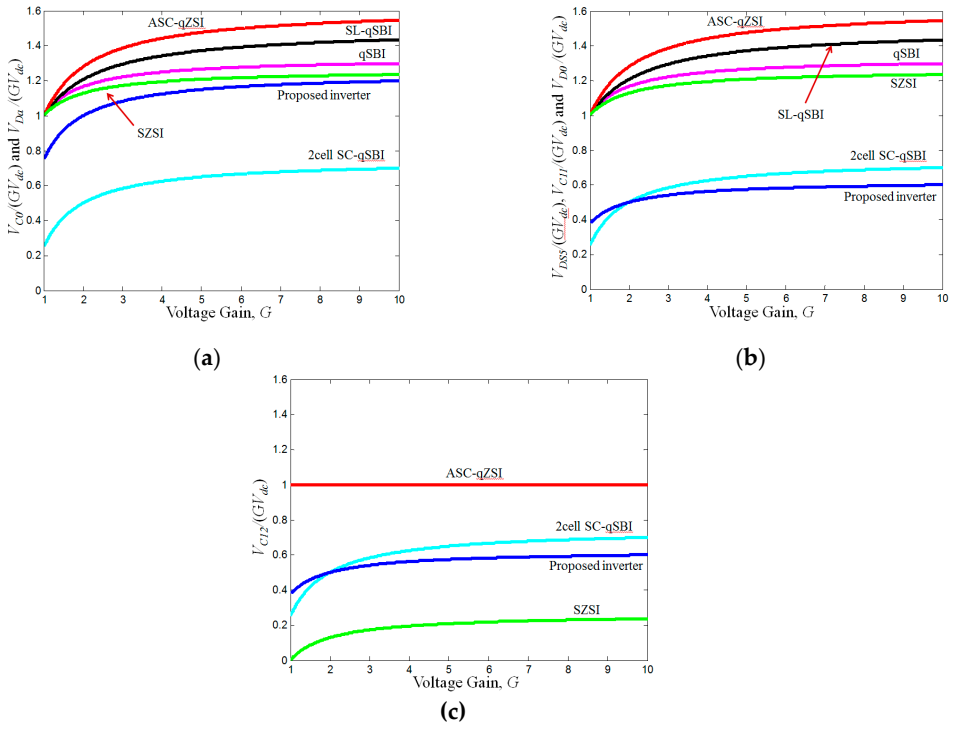


Figure 4. Voltage stress comparison. (**a**) Voltage stress on capacitor C_0 and diode D_a, (**b**) voltage stress on switch S_5, capacitor C_{11}, and diode D_0, and (**c**) capacitor C_{12} voltage stress.

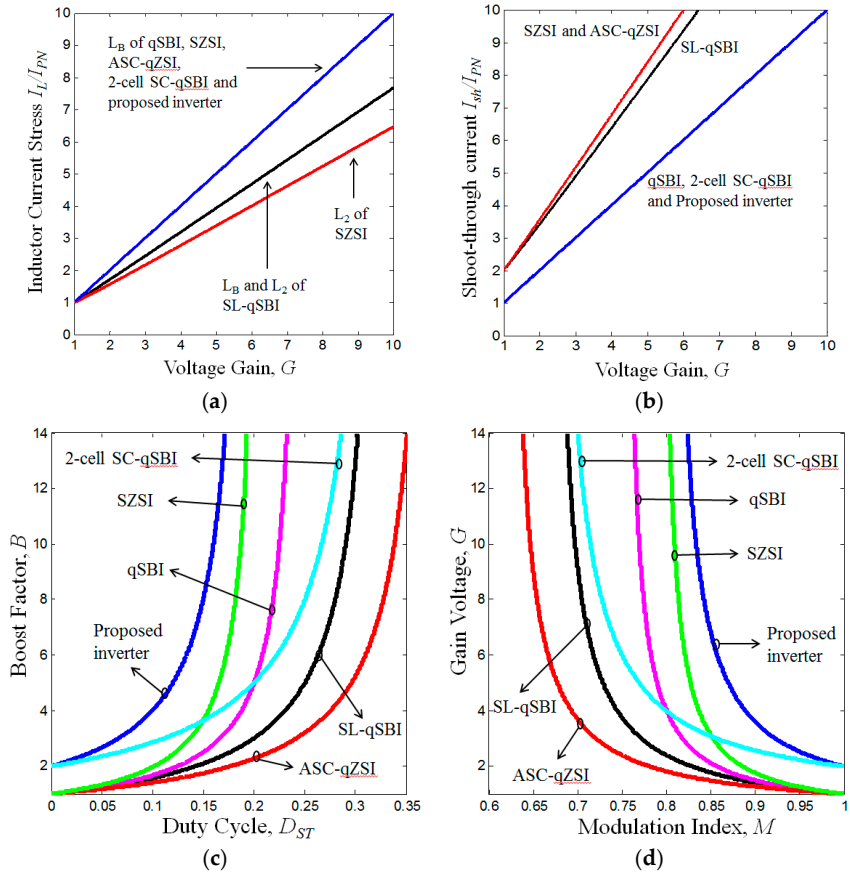


Figure 5. Voltage and current stress comparison. (**a**) Inductor current stress, (**b**) ST current stress, (**c**) boost factor, and (**d**) voltage gain.

4.3. Voltage Gain and Boost Factor

Figure 5c,d compares the boost factor and the voltage gain of the proposed VMC-qSBI with those of the active impendence source inverters, respectively. The voltage gain of the proposed VMC-qSBI is greatest for the same modulation index. The high modulation index is very important to achieve a high output waveform quality with a low total harmonic distortion (THD).

4.4. Element Count

Table 1 also compares the number of elements required for the inverters. Although the proposed VMC-qSBI adds one active switch, it results in savings of a large number of passive devices compared with the high voltage gain qZSIs in [17,19,20]. The proposed VMC-qSBI has the same number of semiconductors as the SZSI, but it uses one more capacitor and one less inductor. Compared with the SL-qSBI, the proposed VMC-qSBI uses two more capacitors, one less diode, and one less inductor. The proposed inverter uses the same number of components as the 2-cell SC-qSBI. Note that the number of diodes in Table 1 includes four body diodes of the H-bridge switches.

5. Simulation and Experiment Results

5.1. Simulation Results

To validate the performance of the proposed inverter, PSIM simulation software was used. The simulation parameters for the single-phase VMC-qSBI are given in Table 2. The drain-to-source on-resistance of the switches S_1–S_4 and the switch S_5 was set to 0.2 Ω and 8 mΩ, respectively. The body diode threshold voltage of the switches S_1–S_4 and the forward voltage of the diodes D_a, D_0, D_{11}, and D_{12} are 1.5 V and 0.73 V, respectively. The fundamental frequency of the ac output voltage and the switching frequency are 50 Hz and 20 kHz, respectively. An inductor-capacitor (LC) filter of 1 mH and 20 μF was connected to the inverter output. A purely resistive load of 40 Ω was used in the simulation.

Table 2. Parameters used for simulation and test.

Parameters		Values
Input voltage range (V_{dc})		50–72 V
Maximum input current		8 A
Output power (P_o)		350 W
Output voltage (V_o)		110 Vrms/50 Hz
Input inductor		0.37 mH
Capacitors	C_{11}, C_{12}	1000 μF/100 V
	C_0	2 × 680 μF/200 V
Output filter	L_f	1 mH
	C_f	20 μF
Switching frequency		20 kHz
Modulation index (M)		0.9
MOSFETs	S_5	IRFP4668 (200 V, 140 A)
	S_1~S_4	IRFP460 (500 V, 20 A)
Diodes	D_{11}, D_{12}, D_0	STPS60SM200C (200 V, 30 A)
	D_a	IXYS30-60A (600 V, 37 A)

Figure 6 shows the simulation results for the single-phase VMC-qSBI when V_{dc} = 50 V, D_{ST} = 0.1, D_5 = 0.3, and M = 0.9. Because of the existing passive components in the impedance-source network, an inrush current has appeared at the start-up process, as can be seen in Figure 6a. Figure 6b,c shows

the simulation results in the steady-state. The voltage of capacitors C_{11}, C_{12}, and C_0 in the steady-state are boosted to 97.1 V, 96.2 V, and 193 V, respectively. The ac output voltage is 121 V_{rms}. The input current is continuous and has a small peak-to-peak ripple of 0.92 A.

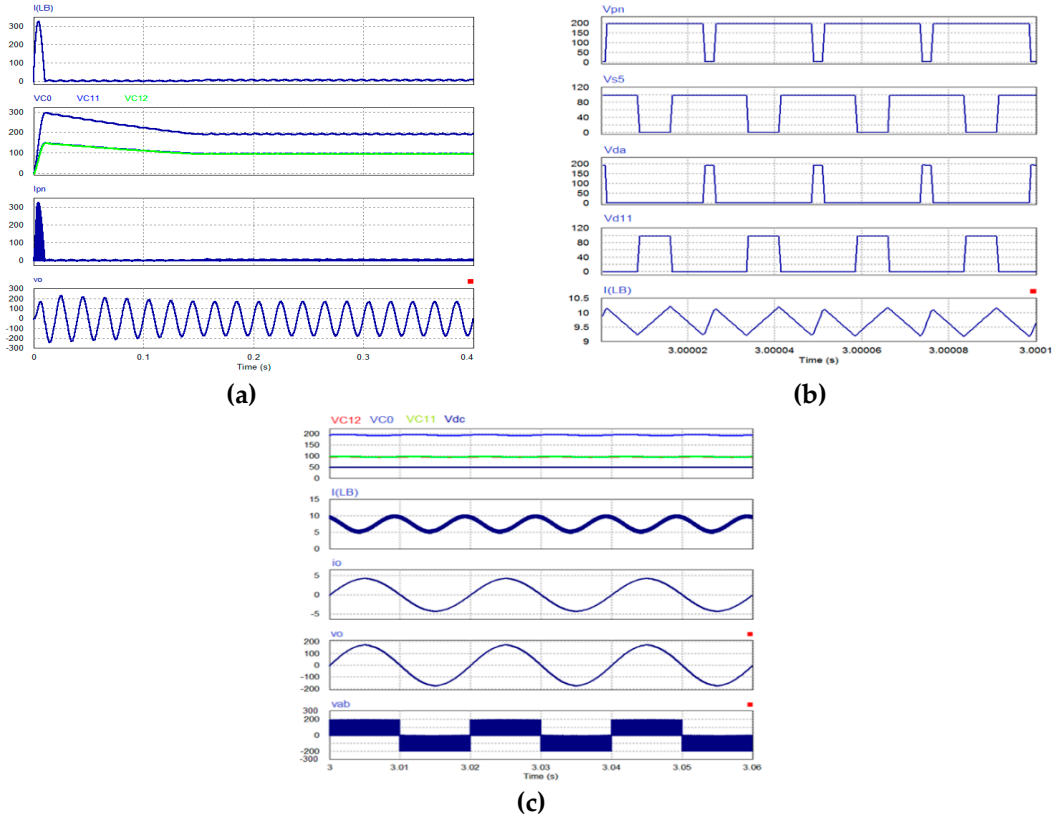


Figure 6. Simulation results for the proposed single-phase VMC-qSBI when V_{dc} = 50 V. From top to bottom: (**a**) input current, capacitor voltages, dc-link current, and output voltage; (**b**) dc-link voltage, drain-source voltage of S_5, diodes D_a–D_{11} voltage, and input current; and (**c**) input voltage and capacitors voltages, input current, output current, and output voltages before and after the L-C filter.

The three-phase VMC-qSBI as shown in Figure 7 is used to test the PWM technique with low input current ripple as presented in Section 2.2. All parameters of the three-phase VMC-qSBI including capacitance, inductance, diodes, MOSFETs, and load are the same as those of the single-phase VMC-qSBI. The maximum constant boost PWM control method in [28] is used to control three-phase H-bridge switches, while the additional switch S_5 is controlled by the constant voltage V_5 as shown in Figure 3b. Figure 8 shows the simulation results for the three-phase VMC-qSBI when V_{dc} = 50 V, D_{ST} = 0.1, D_5 = 0.3, and M = 0.9 × 1.15. As shown in Figure 8a, the capacitors C_{11}, C_{12}, and C_0 voltage are boosted to 98 V, 97 V, and 195 V in the steady-state, respectively. The three phase currents are 1.8 A in RMS. Under resistive load of 40 Ω, the simulated output phase voltage is 72 V in RMS, whereas the calculated value of the output phase voltage is 73 V in RMS. The input current is continuous. As shown in Figures 6b and 8b, the D_a diode reverse voltage is zero in non-ST states, and is equal to capacitor C_0 voltage in the ST state. The voltage stress on the additional switch S_5 is a half of dc-link voltage. All of the simulation results are in agreement with the theoretical analysis.

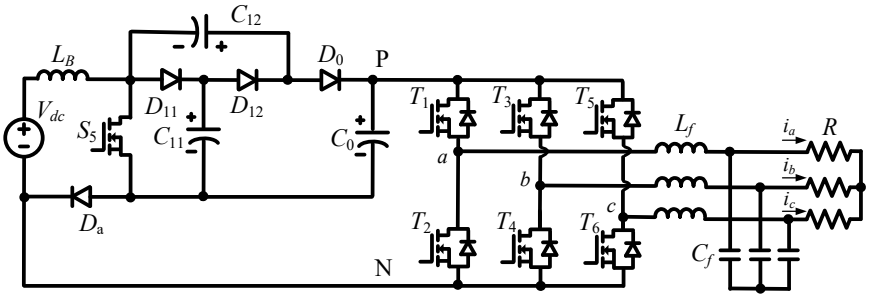
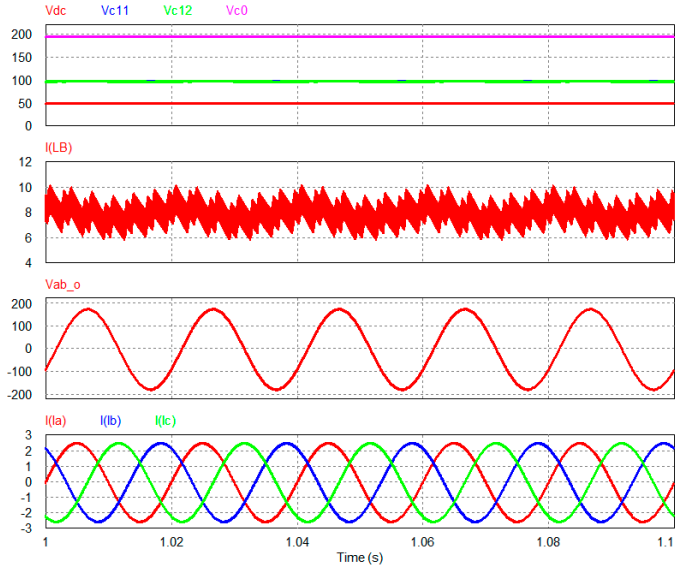
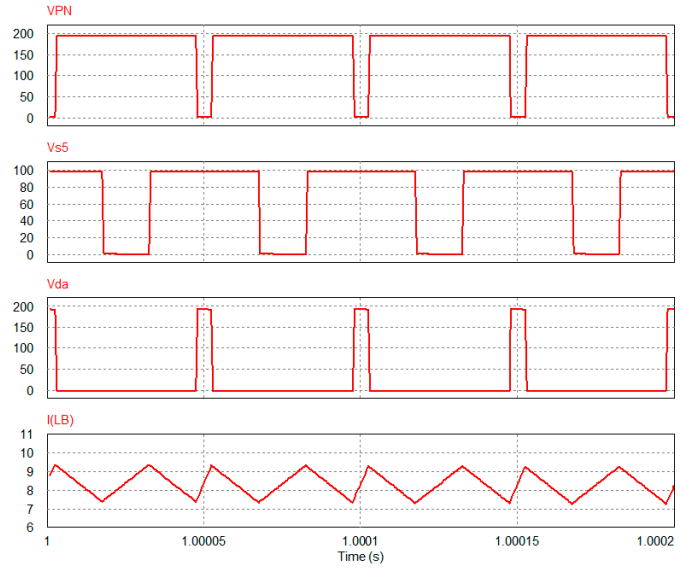


Figure 7. Proposed three-phase VMC-qSBI in simulation.



(**a**)



(**b**)

Figure 8. Simulation results for the proposed three-phase VMC-qSBI when V_{dc} = 50 V, D_{ST} = 0.1, D_5 = 0.3, and M = 0.9 × 1.15. From top to bottom: (**a**) input voltage and capacitors voltages, input current, line-to-line voltage, and output currents and (**b**) dc-link voltage, drain-source voltage of S_5, diode D_a voltage, and input current.

5.2. Experimental Results

The experimental prototype was built to test the proposed VMC-qSBI. A 0.37 mH boost inductor was used, and the dc input voltage is supplied by 61604 Chroma Programmable ac Sources with a current limit of 8 A. The voltage stress on switch S_5 is equal to the capacitor C_{11} and C_{12} voltages; thus, for switch S_5, the IRFP4668 MOSFET was chosen with a voltage limit of 200 V. The switches on the H-bridge circuit are IRFP460 MOSFETs. Three diodes D_{11}, D_{12}, and D_0 are Schottky STPS60SM200C diodes, and one IXYS30-60A is used as the diode D_a. Capacitors C_{11} and C_{12} are 1000 µF/100 V. The capacitor C_0 was obtained by connecting in parallel two 680 µF/200 V capacitors. The parameters of the experiment are listed in Table 2. The switching frequency of the H-bridge switches is 20 kHz, and the switching frequency of switch S_5 is 40 kHz. The PWM control signals of the switches are generated by TMS320F28335 DSP, and are driven by isolated TLP250 amplifiers.

Figure 9 shows the experimental results of the proposed VMC-qSBI when V_{dc} = 50 V, M = 0.9, V_o = 110 V_{rms}, and P_o = 300 W. The dc-link voltage is boosted to 181 V from the input voltage of 50 V. The voltages of capacitors C_{11}, C_{12}, and C_0 are boosted to 91.6 V, 89.7 V, and 181 V, respectively, in the steady-state. The boost factor of the experiment is 3.62, while the calculated value for D_{ST} = 0.1 from Equation (10) in the ideal case is 4. The ac output voltage is 110 V_{rms}/50 Hz. The input current is continuous. The current THD at the output is 0.9%. The HF peak-to-peak inductor current of 1.1 A is presented in Figure 9c.

Then, the input voltage is increased to 72 V. To obtain the same 110-V_{rms} output voltage while the modulation index is kept at 0.9, the ST duty cycle is decreased to 0.05. Figure 10 shows the experimental results of the VMC-qSBI when V_{dc} = 72 V, M = 0.9, V_o = 110 V_{rms}, and P_o = 300 W. The voltages of capacitors C_{11}, C_{12}, and C_0 are boosted to 91.2 V, 90.2 V, and 181 V, respectively, from a 72 V input voltage. The HF peak-to-peak inductor current is 0.8 A. The measured THD of the output current is 1%.

Figure 11a,b shows the gate-pulse waveforms for switches S_1–S_3 when V_{dc} is 50 V and 72 V, respectively. As shown in Figure 11a,b, the overlap duty cycle (D_{ST}) of the gate pulse for switches S_1–S_3 is one-third of the duty cycle of switch S_5. The waveforms from top to bottom in Figures 9a and 10a are the output voltage after the L-C filter, the load current, the input current, and the input voltage. The waveforms from top to bottom in Figures 9b and 10b are the voltages across capacitors C_{11}, C_{12}, and C_0, and the output voltage before the L-C filter. The waveforms from top to bottom in Figures 9c and 10c are the drain-source S_5 voltage, the diode D_a voltage, the input current, and the dc-link voltage. The waveforms from top to bottom in Figures 9d and 10d are the voltages across diodes D_{11}, D_{12}, and D_0, and the drain-source S_1 voltage. The waveforms in Figure 11a,b are the control gate signals of S_5 and S_1–S_3.

Figure 12a shows the boost factor comparison between the calculation and the experiment for the VMC-qSBI. In this experiment, the duty cycle was varied from 0.05 to 0.12, while the output voltage and the output power were kept at 110 V_{rms} and 300 W, respectively. Because of the parasitic elements in the experimental setup, the experimental values are lower than the calculated values. Figure 12b shows the efficiency of the VMC-qSBI with various power loads. The maximum efficiency value of the VMC-qSBI at a load power of 165 W and an input voltage of 72 V is 91.3%.

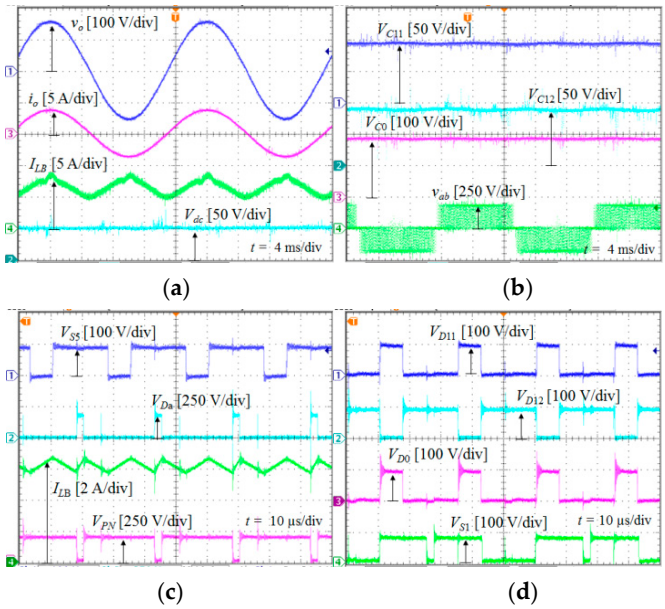


Figure 9. Experimental waveforms for the proposed inverter when V_{dc} = 50 V. From top to bottom: (**a**) output voltage after the L-C filter, load current, input current, and input voltage; (**b**) voltages across capacitors C_{11}, C_{12}, and C_0, and output voltage before the L-C filter, (**c**) drain-source S_5 voltage, diode D_a voltage, input current, and dc-link voltage; and (**d**) voltages across diodes D_{11}, D_{12}, and D_0, and the drain-source S_1 voltage.

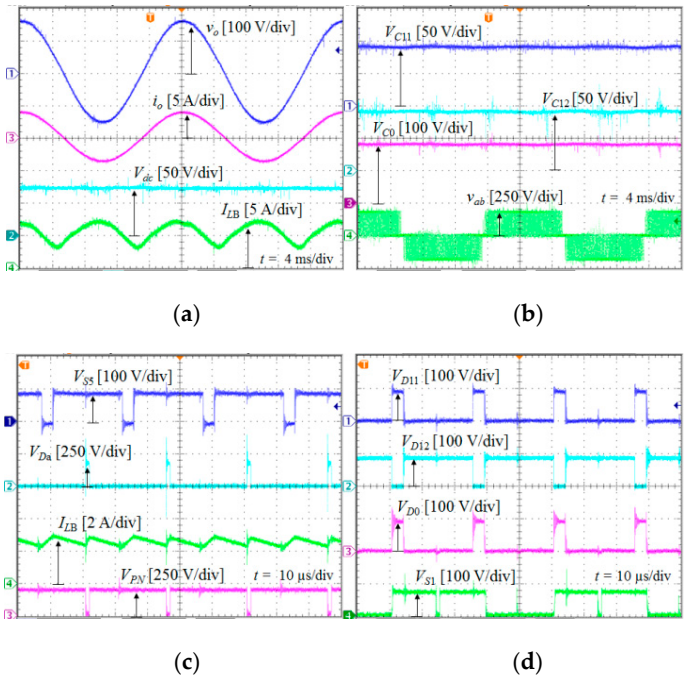


Figure 10. Experimental waveforms for the proposed inverter when V_{dc} = 72 V. From top to bottom: (**a**) output voltage after the L-C filter, load current, input current, and input voltage; (**b**) voltages across capacitors C_{11}, C_{12}, and C_0, and output voltage before the L-C filter, (**c**) drain-source S_5 voltage, diode D_a voltage, input current, and dc-link voltage; and (**d**) voltages across diodes D_{11}, D_{12}, and D_0, and the drain-source S_1 voltage.

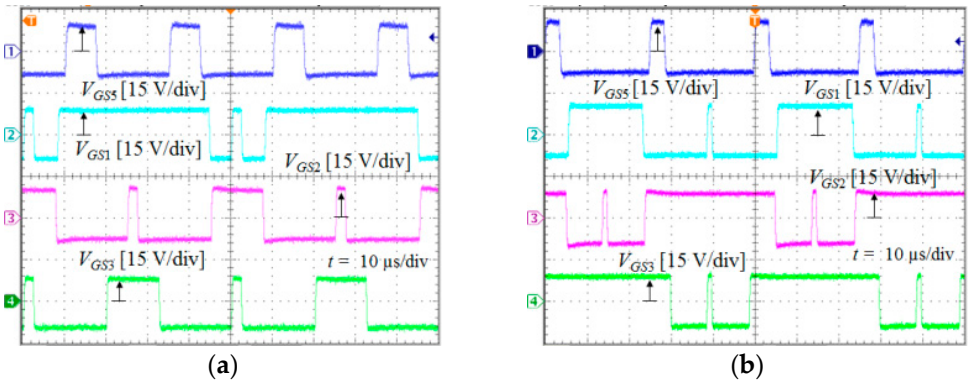


Figure 11. Control signal waveforms when (**a**) V_{dc} = 50 V and (**b**) V_{dc} = 72 V.

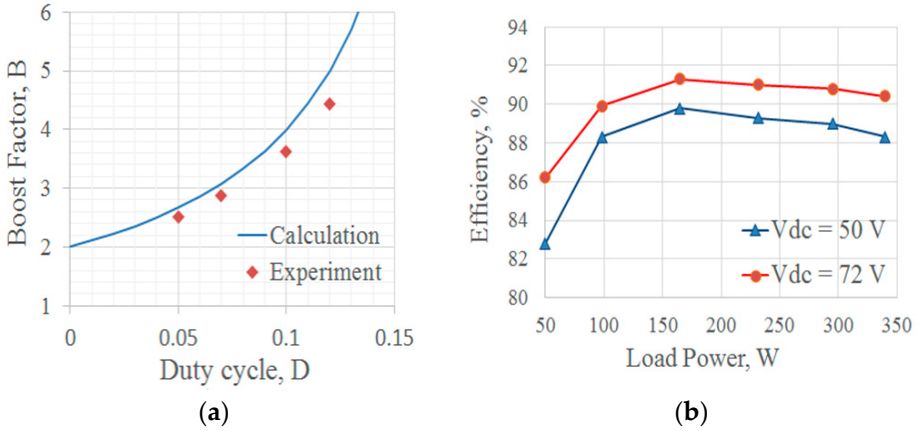


Figure 12. Measured results of (**a**) boost factor and (**b**) efficiency of the proposed inverter.

6. Discussions and Conclusion

Although ZS/qZSIs and qSBIs have a good performance with buck-boost voltage function, single-stage conversion, and ST immunity, their disadvantage is high voltage stress on capacitors, diodes, and switch. Using a small voltage rating of the devices leads to reduce the loss and cost of the power inverter system. Moreover, a small ST duty ratio or a high modulation index helps to enhance the output waveform quality of the inverter. In this paper, a new single-phase single-stage boost inverter based on the VMC structure was proposed. A new PWM control strategy was used for the proposed inverter to achieve a high voltage gain with a low input current ripple. Compared to the other active impedance source inverters, the proposed VMC-qSBI has a high voltage gain, low input current ripple, low voltage stress on the switch and diode, low ST current, and high modulation index. The extension was presented to improve the voltage gain of the proposed inverter by adding the VMCs. The operating modes, steady-state analysis, and design guideline were presented. A laboratory prototype was tested to verify the accuracy of the proposed VMC-qSBI. Simulation and experimental results were shown.

Because the proposed VMC-qSBI has high reliability with ST immunity, low voltage stress on devices, and high voltage gain inversion with multi-VMCs, it is suitable for renewable energy system applications such as photovoltaic and wind power.

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