

Article

# Design of Experiment (DOE) Analysis of System Level ESD Noise Coupling to High-Speed Memory Modules

Jawad Yousaf <sup>1</sup> , Muhammad Faisal <sup>1</sup>, Jinsung Youn <sup>2</sup> and Wansoo Nah <sup>1,\*</sup>

<sup>1</sup> Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea; jawad@skku.edu (J.Y.); mfaisal@skku.edu (M.F.)

<sup>2</sup> Hewlett Packard Enterprise, Palo Alto, CA 94304-1112, USA; jin-sung.youn@hpe.com

\* Correspondence: wsnah@skku.edu

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**Abstract:** This paper presents, for the first time, a comprehensive detailed design of experiment (DOE) based system level electrostatic discharge (ESD) coupling analysis of high-speed dynamic random access (DRAM) memory modules. The sensitive traces and planes on the high-speed DRAM modules (DDR3 and DDR4) against injected ESD noise are determined through full-wave numerical simulations of the memory modules using the developed 3D model of the ESD gun. The validity of the full-wave numerical setup is confirmed through measurements, prior to the DOE analysis. Besides, current distribution analysis of DRAMs, seven different DOE configurations based on the number of installed decoupling capacitors (decaps) and their values on memory modules, are analyzed. The findings of DOE analysis suggests that DDR4 is less susceptible (70–80 % less) to the coupled ESD noise compared to DDR3. In addition, the command address (CA) nets are most sensitive in both memory modules. The utilization of the maximum possible number of decaps covering low, medium and high frequency ranges, as well as separate power and ground layers in memory stack-up design, increase the robustness and immunity of memory modules for the transient ESD event. The suggested approach offers time-saving and financial advantages to high-speed memory community, with the robust design of the memory products at the design stage before the start of the production phase.

**Keywords:** Electrostatic Discharge (ESD); Dynamic Random Access Memory (DRAM); ESD gun; 3D model; numerical model; system level ESD

## 1. Introduction

The occurrence of transient electrostatic discharge (ESD) events results in the malfunctioning of the electronic devices due to the transfer of high amplitude current signals having a short rise time. ESD issues are becoming more critical due to the increasing speed of the microelectronic devices (e.g., DRAM memory modules) and stringent quality test passing criterion of the original equipment manufacturer (OEM) [1,2].

The direct or indirect electromagnetic (EM) coupling of the ESD noise to the sensitive module of the device under test (DUT), such as DRAM memory, would change the operational conditions of the complete product (such as a laptop). Consequentially, the product could be rejected from the quality and reliability testing [1,3,4]. The failure could be a soft or hard (permanent damage of DUT). The soft failure examples include: the incorrect reading or writing of the data to the hard disk (wrong instructions due to command/data bit change); abrupt turn off of the device; and/or the change in the operational condition of the device with a display of wrong output on DUT screen [1,5–8]. The

change of the ESD generator model could also affect the qualification of the DUT [3,9]. Furthermore, the lack of information about the ESD noise coupling paths makes things more difficult for the ESD qualification and reliability engineers, for the design of a possible solution.

To increase the robustness of the products against injected ESD noise, different experimental and full-wave numerical modeling techniques for system level ESD coupling analysis have been proposed in the literature. These include: failure analysis using susceptibility testing [5]; analysis of coupled ESD noise to DUT through time and frequency domain measurements [1,10–14]; and full-wave EM simulation of DUT and ESD source [2,6,15–18]. These reported techniques have limitations in terms of the requirement of the manufacturing of the DUT to perform susceptibility analysis [5], or the characterization of the coupled noise at victim positions for each different design configuration of the DUT [10–14,19].

The localized near field susceptibility scanning approach of [5] also has a limitation of inaccurate prediction of the root cause of failure for the high density ball-grid array integrated circuits (ICs), where the signal/data traces are routed on multiple inner layers. In addition, the size of the injection probes used in susceptibility analysis becomes quite large compared to the small size of such ICs [6,20]. The ESD analysis using full-wave EM simulation provides more insight into the ESD noise coupling paths across multiple layers unlike [5], and thus making it more appropriate for the fast and efficient analysis of ESD coupling to DUT, compared to only experimental techniques [1,5,6,10–14]. The existing studies related to ESD coupling analysis using full-wave numerical modeling, are either for a simple transmission line, circular loop and mobile phone-based DUTs [16–18,21] or lacks in the methodology for the systematic assessment of the sensitive traces for a realistic complete high-speed memory module.

In this paper, for the first time, we present a new DOE based full-wave EM simulation framework for the system level ESD noise coupling analysis of the realistic complete high-speed DRAM memory modules. The objective of the study is to identify the most sensitive traces on the memory modules. The study also analyzed the impact on the predicted sensitive traces when the number and values of installed decaps on memory modules are varied. Figure 1 shows the proposed DOE configurations based framework to identify the suitable design configuration of DUT for the reduction of soft-failure due to the coupled ESD noise. The validation of the designed 3D ESD gun model [19,22] for the full-wave EM simulations of memory modules is performed by comparing the injected current and induced voltage results for a microstrip line printed circuit board (PCB) in the complete IEC 61000-4-2 system level ESD setup environment [23]. After the validation of the made 3D EM numerical setup, microstrip line PCB is replaced with real models of the DDR3 and DDR4 memory modules for the current distribution analysis. Current distribution analysis provides an overview of the “hotspot” points where the maximum noise is coupled. The identified sensitive region using current distribution analysis contains different routed traces (command, address, clock, and data). To differentiate between the sensitivity of the different signals/data traces on memory modules against the zapped ESD noise, and to predict the best DUT design configuration for minimal induced ESD coupling, DOE analysis is performed in the following two parts:

- The sensitive traces on memory modules are identified by monitoring the induced voltages across different nets (by defining the voltage monitors (VM) across the net and ground plane of memory module) around various small outline dual in-line memory module (SODIMM) chips on memory modules
- The effects of the decaps values and number of decaps on induced voltages across identified sensitive traces are analyzed.

The major contribution and uniqueness of this study is the detailed extensive DOE based analysis of the two different realistic high-speed DRAM modules for coupled ESD noise in the complete system level ESD setup of IEC [23] using developed ESD gun model. To the best knowledge of the authors, no such study is reported in the literature for real, complete high-speed memory modules.

The rest of the paper is organized as follows: Section 2 describes the validation of the designed ESD numerical setup through ESD coupling analysis measurements and simulations. The current distribution analysis of DRAM modules (DDR3 and DDR4) is presented in Section 3. The details of the DOE experimentation for the identification of sensitive nets and appropriate design configuration for the reduction of coupled ESD noises are given in Sections 4 and 5, respectively. Section 6 concludes the findings of the study.

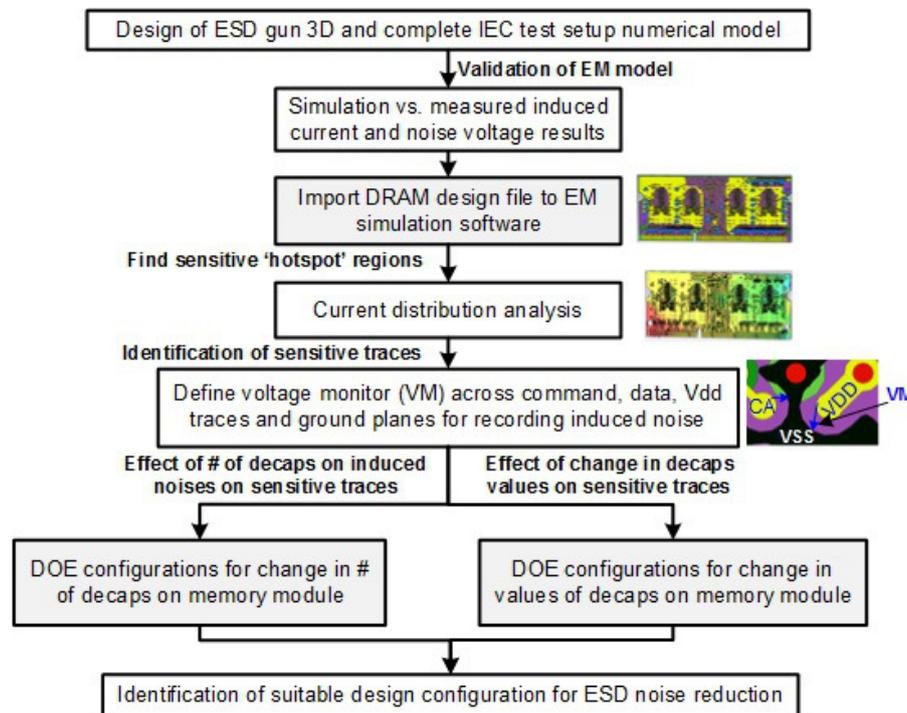
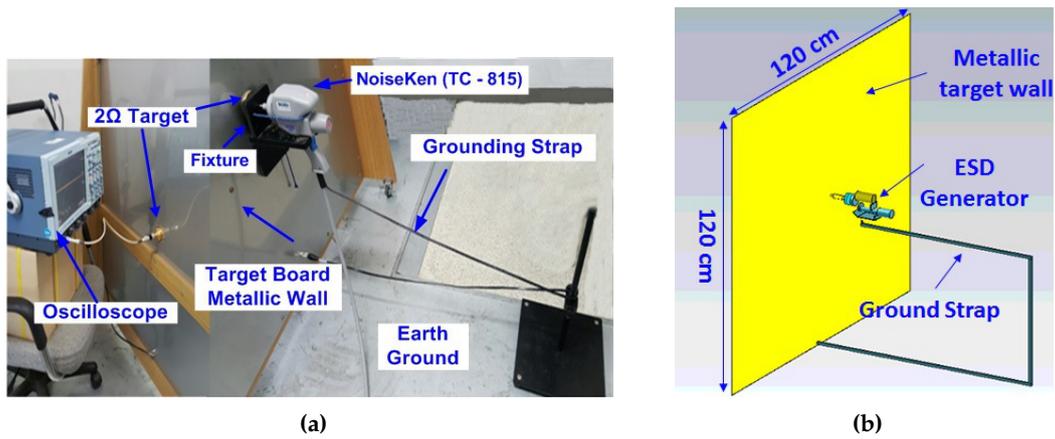


Figure 1. Proposed system level ESD coupling analysis framework based on DOE.

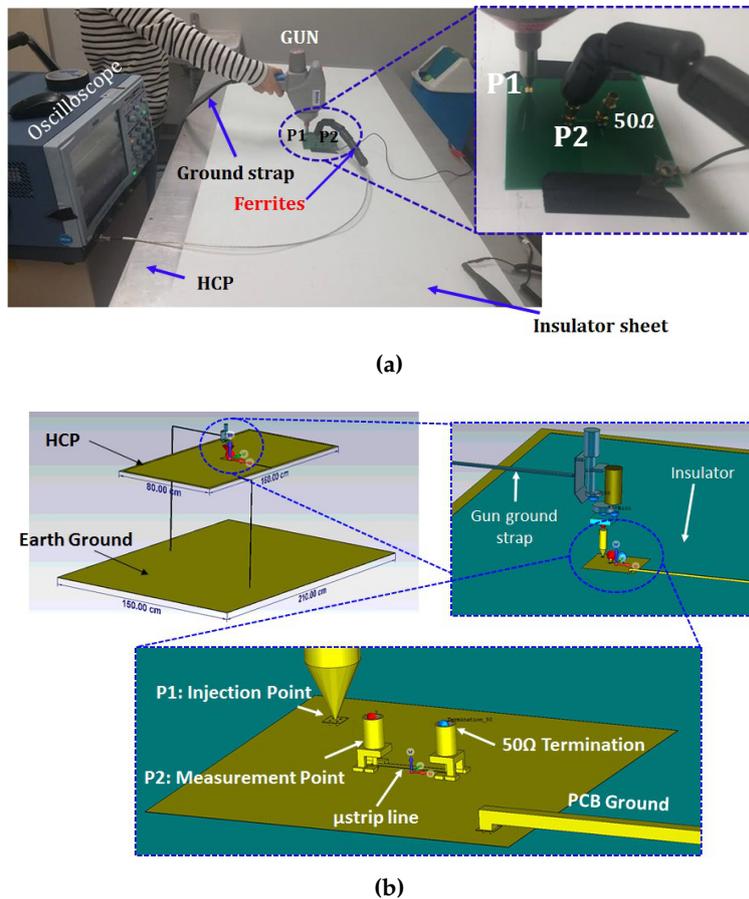
## 2. Validation of Estimation of Induced ESD Noise Using 3D EM Model

The validation of the developed numerical model of ESD gun model [19,22] is performed prior to the conduction of DOE experimentation on the full-wave realistic models of DRAM memory modules. The numerical model is used to generate the standard ESD reference waveform and to predict the induced coupling at the victim point on 20 mm  $\mu$ -strip line test PCB (DUT). The simulation results of numerical models are compared with measurement results for verification.

The measurement test setup for the calibration of the reference ESD waveform as per the requirements of [23] is shown in Figure 2a. The full-wave equivalent numerical model of Figure 2a is depicted in Figure 2b. Figure 3 shows the measurement setup and full-wave 3D model of the ESD gun and DUT for the induced ESD coupling analysis at the victim position ("P2") on DUT. The ESD noise is zapped at the ground plane ("P1") of DUT using Noiseken TC 815 gun while the coupled noise at the "P2" point is measured using high frequency oscilloscope as depicted in Figure 3a. The simulation setup in Figure 3b is almost an exact replica of the system level ESD measurement setup in Figure 3a, as per the requirements of [23]. The detailed description of measurement setup and numerical models of Figure 2 can be found in [19,22].



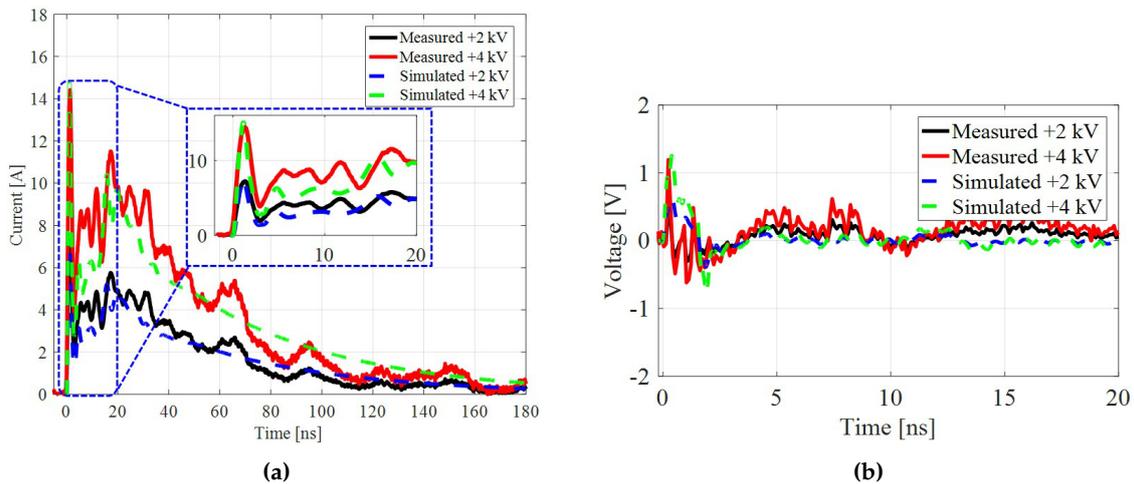
**Figure 2.** Reference ESD current waveform calibration setup: (a) IEC standard waveform measurement calibration setup; and (b) 3D model of calibration setup with developed Noiseken TC-815 ESD gun model in CST microwave studio (MWS).



**Figure 3.** ESD coupled noise analysis for  $\mu$ -strip line PCB: (a) measurement setup as per IEC 61000-4-2 requirements; and (b) full-wave EM model of  $\mu$ -strip line PCB for induced coupling analysis with developed ESD gun model.

The comparison of simulation and measured results of reference ESD waveforms is shown in Figure 4a for two input discharge voltage levels (+2 kV and +4 kV). The comparison illustrates that the developed 3D gun model accurately generates the reference ESD waveforms for different input discharge levels.

The comparison of the full-wave EM simulation results of Figure 3b with the measured results of Figure 3a is depicted in Figure 4b for +2 kV and +4 kV input discharge voltage levels. Figure 4b shows that the simulation and measured induced voltages waveforms have very good agreement for both discharge voltage levels. It confirms that the developed numerical model (Figure 3b) of complete measurement setup of system level ESD testing successfully predicts the induced voltages at victim position for different input ESD voltage levels and, thus, can be used as a reliable model for the ESD immunity testing of any DUT.



**Figure 4.** Measurement vs. simulation results: (a) comparison of measured and simulated ESD current waveforms; and (b) comparison of measured and full-wave EM simulation results of induced voltages for  $\mu$ -strip line test PCB.

### 3. Current Distribution Analysis Due to ESD Noise

#### 3.1. ESD Gun

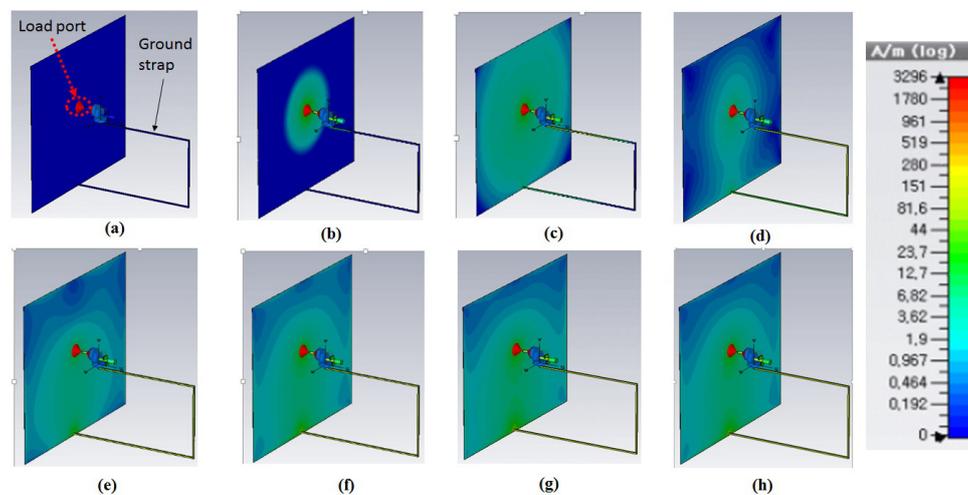
Firstly, the current distribution on the metallic ground wall with only ESD gun in the standard calibration setup of IEC 61000-4-2 [23] is analyzed in CST MWS. The analysis is performed for the developed Noiseken model in Figure 2b. To monitor the current distribution at different time steps, current field monitors are defined for 0–60 ns period with a coarse step size of 0.5 ns. The field monitors records the distributed current on the structure for each time step. The memory requirement increased drastically for the shorter time step.

Figure 5 shows the current distribution at different time intervals for the used full-wave Noiseken gun model in Figure 2b. Figure 6 presents the enlarged current distribution results for the ESD gun ground strap. For the initial time of 0–3 ns (see Figure 5a–c), high frequency components flow through the metallic ground plane target wall due to the offered low impedance path. Afterwards, the low frequency components started flowing through the ground strap, as can be observed in Figure 6e–h. It shows that ESD current peak value is dependent on metallic ground plane size and the structure, while the current values at higher time intervals, e.g., at 30 ns and 50 ns, are dependent on the ground strap of the gun.

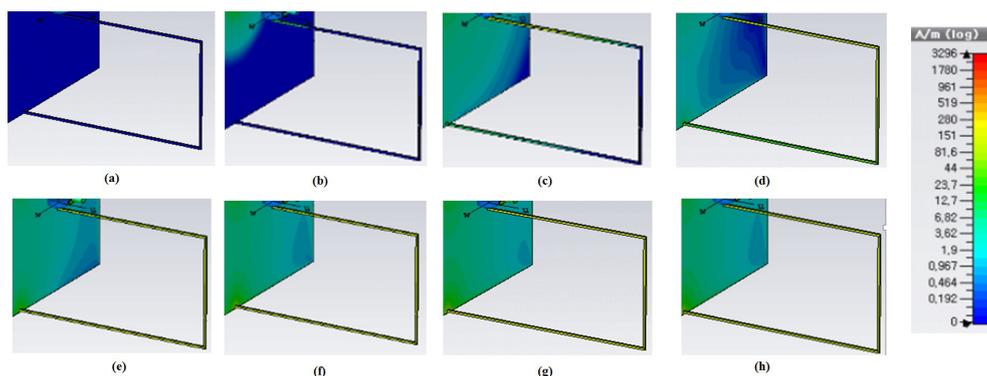
#### 3.2. DRAM Memory Modules

The current distribution analysis for the injecting ESD current is performed for two types of high-speed memory modules: DDR3 and DDR4. The accurate prediction of distributed current on DUT demands the accurate 3D modeling of DUT as a real model. The precise numerical modeling of complete memory module needs the exact information of module size, SODIMM chips positions and connections, routing configurations, layers stack-ups, lumped component values and their installation configurations on modules. For more accurate EM simulation of memory modules, the memory

modules design files are obtained from the open source available design files of Joint Electron Device Engineering Council (JEDEC) standard.



**Figure 5.** Current distribution for Noiseken gun model of Figure 2b for +4 kV voltage level: (a) 0 ns; (b) 1 ns; (c) 2.5 ns; (d) 4.5 ns; (e) 7 ns; (f) 20.5 ns; (g) 30 ns; and (h) 50 ns (the red part at the center of board as explained in a is of the load port not the color of current distribution).



**Figure 6.** Enlarged current distribution of ground strap from Figure 5: (a) 0 ns; (b) 1 ns; (c) 2.5 ns; (d) 4.5 ns; (e) 7 ns; (f) 20.5 ns; (g) 30 ns; and (h) 50 ns.

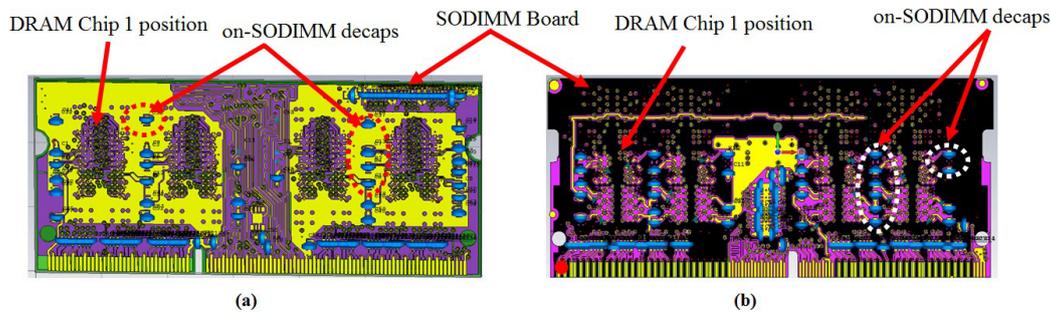
### 3.2.1. Design Files Importing

DDR3 and DDR4 design files are downloaded from [24,25], respectively. The details of the design files of both used DRAM modules are given in Table 1. Both DDR3 and DDR4 modules are of SODIMM type. For the analysis of the memory modules in CST MWS, “\*.brd file” from the downloaded folder of each memory modules is imported to the EM software. The files are imported in CST MWS by following this selection path: “Modeling → Import/export → 2D/EDA files → Cadence Allegro PCB/APD/SIP”. It is recommended to first import the “.brd file” design files in a separate model in CST MWS and then save it as CST file. This imported saved file is then added to the complete analysis setup file by using the “Sub-Project” option in the import tab.

Figure 7 shows the imported design file models of the DDR3 and DDR4. We note the positions of the DRAM chips and installed decoupling capacitors on the SODIMM boards of both memory modules in Figure 7. The installed decaps on the SODIMM boards of both memory modules are referred to as “on-SODIMM board decaps”, or “off-chip decaps” in this study. The conducted DOE analysis related to change in the number of decaps and their values presented in Section 5 is related to these on-SODIMM board decaps.

**Table 1.** Design file (DIMM) information of analyzed memory modules.

	DDR3	DDR4
Memory standard	JEDEC	JEDEC
DIMM version	204-pin Unbuffered SODIMMs	260-pin Unbuffered SODIMMs
Title	PC3-SODIMM_V210_RC_B4_20111220	PC4-SODIMM_V090_RC_A0_20131025
Raw card revision	B4	A0
Reference Specification	DDR3 Unbuffered SODIMM Reference Design Standard Rev. 2.1	DDR4 SO-DIMM Design Specification Annex-A0 Item 2228.08

**Figure 7.** Imported design file models in CST MWS: (a) DDR3; and (b) DDR4.

The stack-up details of both models are depicted in Figure 8. Figure 8 and Table 1 illustrate that the stack-up structure of DDR3 constitutes six conductor layers while there are eight layers in DDR4 design. DDR4 has two additional separate layers of VDD (VDD4) and ground plane (GND7) for the power and ground connections, as compared to DDR3 design.

Bill of materials details for both memory modules are depicted in Table 2. The lumped components (resistance and capacitance) details in Table 2 are for the on-SODIMM board components. Both memory module configurations are based on eight SODIMM chips installed on the SODIMM board, as illustrated in Figure 7. Four SODIMM chips are installed on the top side (see Figure 7) while the same number of SODIMM chips are on the backside of the board. There are in total 44 resistive and 71 capacitive lumped components installed on DDR3 module, as depicted in Table 2. On the other hand, DDR4 has a higher concentration of lumped components compared to DDR3: 57 resistive and 73 capacitive lumped components. Resistive lumped components are mostly installed at the primary and secondary sides of the data signals (DQ) and are used as termination resistors for command, address, control, and clock signals. The capacitive components are used as the decoupling capacitors (decaps) to reduce the noise levels. These decaps are installed across different power reference and ground planes such as VREFCA (reference voltage traces for command address (CA) signals)-VDD, VTT/VDD-VSS (GND), etc.

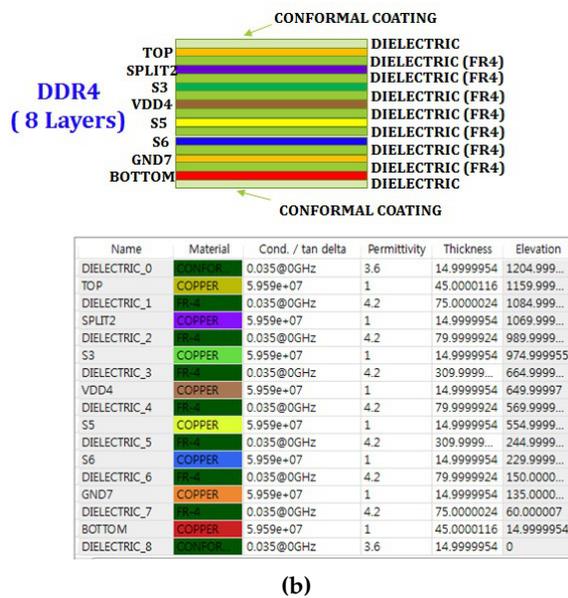
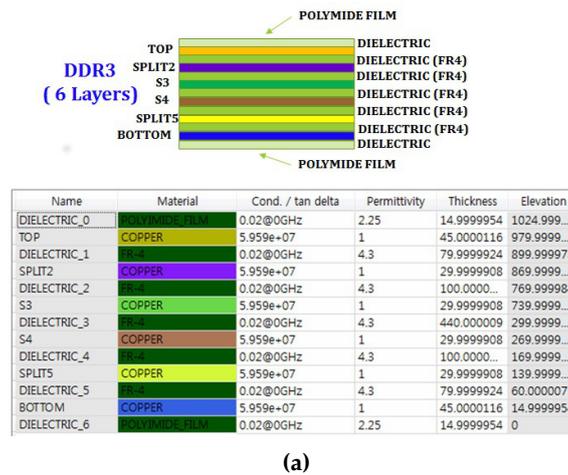


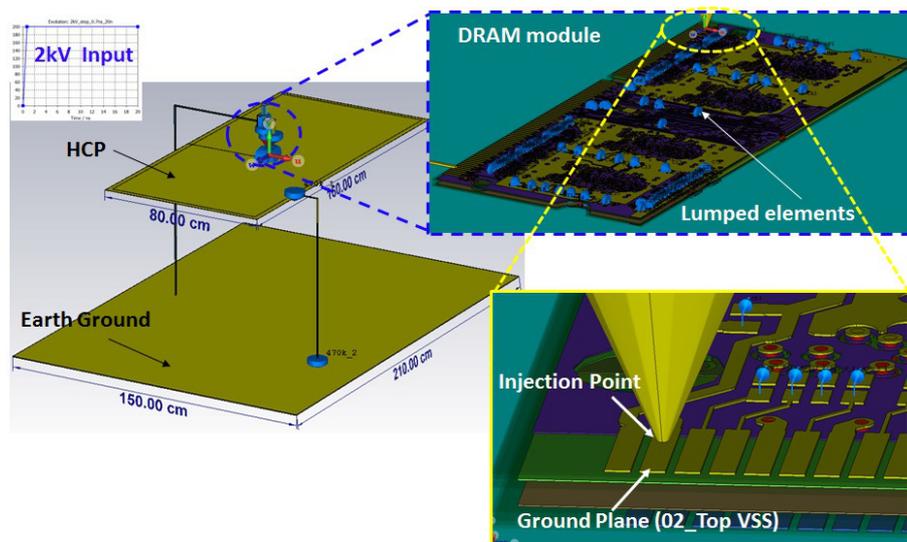
Figure 8. DDR3 vs. DDR4 stack-up: (a) DDR3; and (b) DDR4.

Table 2. Bill of materials (BOM) details of memory modules.

	DDR3	DDR4	
Configuration	1R × 8 SODIMM	1R × 8 SODIMM	
# of layers	6	8	
BOM		15 Ω × 37 ea	
		36 Ω × 2 ea	
	R	39 Ω × 7 ea	
		51 Ω × 1 ea	
		75 Ω × 1 ea	
		120 Ω × 1 ea	
		240 Ω × 8 ea	
	Total R	44	57
	C	1 μF × 5 ea	0.01 μF × 1 ea
		2.2 μF × 4 ea	0.1 μF × 9 ea
	100 nF × 52 ea	1 μF × 61 ea	
	220 nF × 9 ea	100 pF × 1 ea	
	3.3 pF × 1 ea	3.3 pF × 1 ea	
Total C	71	73	

### 3.2.2. Current Distribution Analysis

Figure 9 shows the simulation setup for the current distribution analysis of the memory module. The +2 kV input ESD signal is injected at the ground plane (02\_TOP VSS layer) of the DDR3 module. The dimensions of the horizontal coupling plane (HCP) and earth ground plane in the simulation setup are similar to the real-time system level ESD test setup of [23]. The surface current field monitors are defined for the time period of 0–20 ns (step size: 0.25 ns) for the recording of the distributed current levels on the memory module.



**Figure 9.** Simulation setup for the current distribution analysis of the DDR3 memory module (the dielectric layers of the DDR3 model shown in stack-up of Figure 8a are included in full-wave simulation but are hidden in the above depicted figure for the clarification of conductor layers and ESD injection point).

The selected instantaneous (0 ns, 1 ns, 2 ns, and 5 ns) current distribution results are shown in Figure 10. Note that the other current distributions in the complete memory modules (including all layers such as VDD plane, VSS (ground) plane, VREFCA traces, and CA signal traces) are not reported here for brevity. The current distribution data show that the surface current levels are at minimum level at 0 ns interval. The maximum coupling of the induced noise occurred between 0.75 ns and 1.25 ns. When the maximum current distribution is plotted in CST MWS, the software did not show the corresponding time-stamp value to that maximum values. The time of the maximum current distribution is estimated based on the observed current distribution levels between 0.75 and 1.25 ns and their comparison with the maximum current distribution plot. It can be observed in Figure 10 that the induced current noise coupling levels reduces at 5 ns for both complete module and the individual planes and traces.

Figure 10 also compares the current distribution for DDR3 and DDR4 modules and illustrates that the induced ESD current noise levels are almost 5–6 dB A/m lower in DDR4 (dotted elliptical regions) as compared to DDR3 module. The presence of separate ground and VDD plane in DDR4 (see Figure 8b) provides more shielding for the induced ESD current noise in DDR4. Consequently, it results in lower level of spreading current in DDR4 compared to DDR3 current profile. The current distribution profiles only provide insight into the coupling paths. Although current distribution for each layer can be obtained from full-wave EM simulation results, it is difficult to identify the sensitive traces that are being affected by the induced ESD noise only from the current distribution profiles. For the better estimation of sensitive routing nets on memory modules against the input discharge ESD voltages, information about the induced voltages across those nets is required, as explained in the next section.

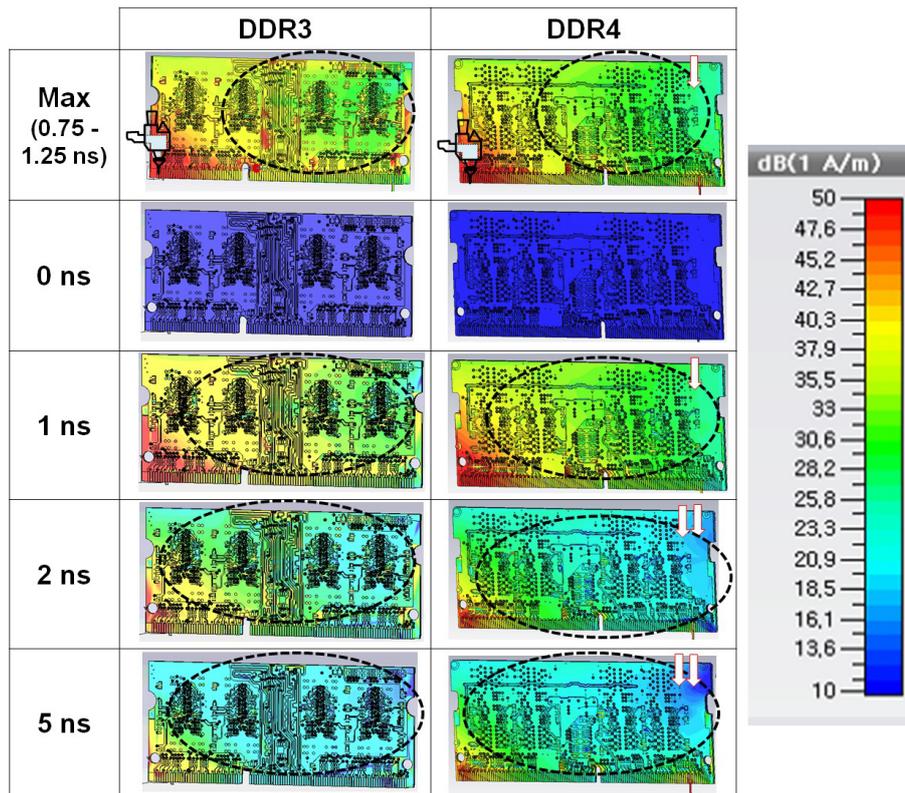


Figure 10. Comparison of current distribution for DDR3 and DDR4 for +2 kV voltage level.

#### 4. Identification of Sensitive Nets through DOE Analysis

To identify the sensitive nets among the VDD, CA and VREFCA nets of memory modules, induced voltages across these nets are measured by conducting the full-wave EM simulation of memory modules using the setup shown in Figure 9. The simulation settings remained the same as for the current distribution analysis in Section 3.2.2. For the monitoring of the coupled voltages across various nets, voltage monitors (VMs) are installed across those nets. Figure 11 shows the installed VMs across the top four SODIMM chips of the DDR3 and DDR4 memory modules, respectively. Three VMs are installed around each SODIMM chip: across VDD-VSS (ground), CA-VSS, and VREFCA-VSS nets. Thus, there are 12 total VMs on each memory module. The zapping point is denoted by the ESD gun in Figure 11 for each case.

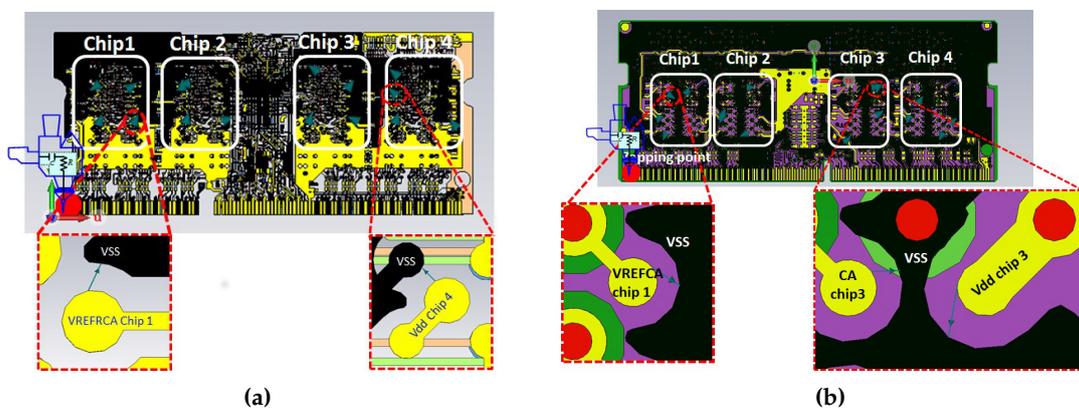
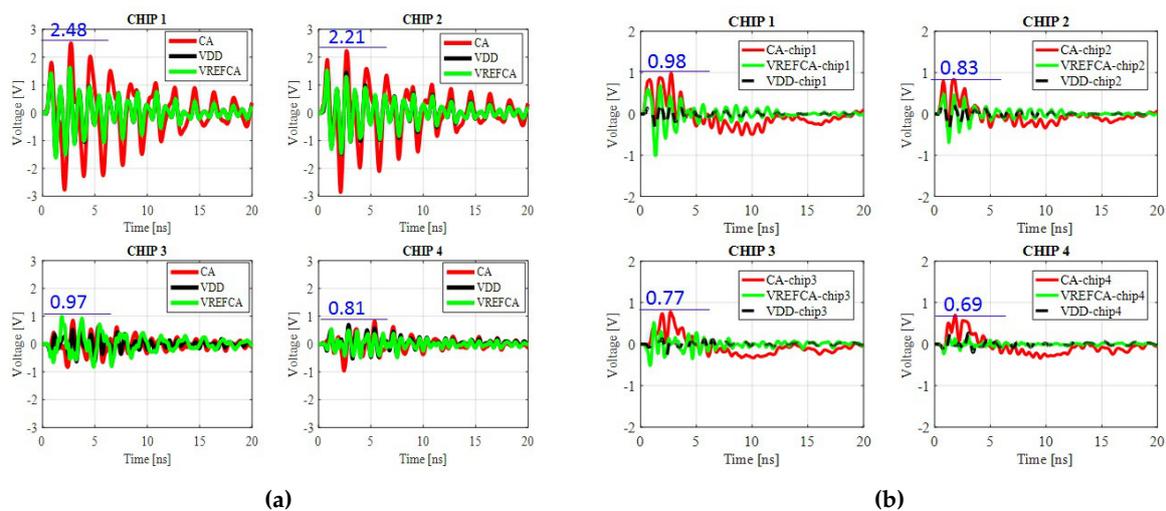


Figure 11. Installed voltage monitors (VMs) across difference trace of memory module for measuring induced ESD noise voltages: (a) DDR3; and (b) DDR4.

Figure 12 shows the induced voltages for the analyzed nets across the different chips of DDR3 and DDR4 modules. The maximum and peak to peak (VPP) voltage values for all nets around each SODIMM chip are depicted in Tables 3 and 4 for each memory module. Figure 12a and Table 3 demonstrate that CA net is the most sensitive for chip 1, chip 2, and chip 4, as the higher values of coupled ESD noise voltages are observed for this net. The maximum induced voltages levels across CA net for chip 1, chip 2, and chip 4 are 2.48 V, 2.21 V, and 0.81 V, respectively. On the other hand, the VDD nets are least sensitive to the injected noise. The recorded maximum voltage levels for VDD case are 1.60 V, 1.48 V, 0.61 V, and 0.68 V for chip 1, chip 2, chip 3 and chip 4, respectively. These voltage levels are lower than the induced voltages across CA and VREFCA nets.



**Figure 12.** Comparison of induced voltages with respect to net and chip positions for each memory module: (a) DDR3; and (b) DDR4.

**Table 3.** Induced voltages across all nets around each chip of DDR3 module (see waveform in Figure 12a) (bold depicts the sensitive net around each chip position).

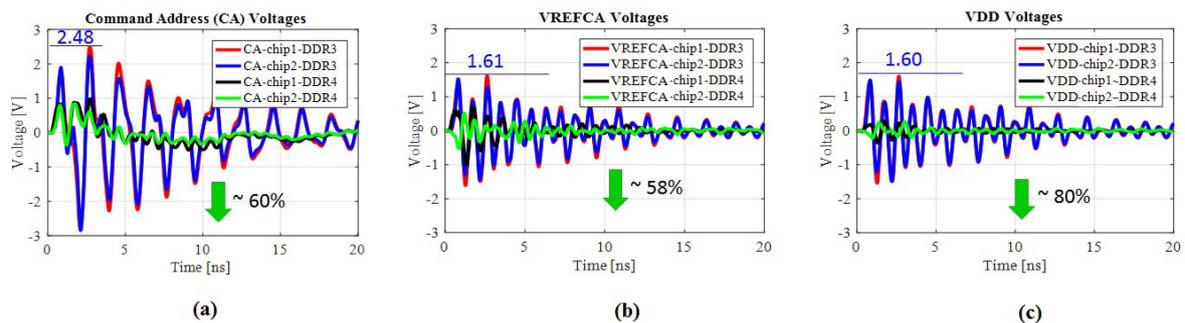
	Chip 1		Chip 2		Chip 3		Chip 4	
Trace	Max [V]	PP [V]						
CA	<b>2.48</b>	<b>5.25</b>	<b>2.21</b>	<b>5.06</b>	0.83	1.66	<b>0.81</b>	<b>1.77</b>
VREFCA	1.61	3.22	1.52	2.97	<b>0.97</b>	<b>1.78</b>	0.53	1.01
VDD	1.60	3.13	1.48	2.96	0.61	1.23	0.68	1.21

**Table 4.** Induced voltages across sensitive trace around each chip of DDR4 module (see waveform in Figure 12b) (bold depicts the sensitive net around each chip position).

	Chip 1		Chip 2		Chip 3		Chip 4	
Trace	Max [V]	PP [V]						
CA	<b>0.98</b>	<b>1.49</b>	<b>0.83</b>	<b>1.20</b>	<b>0.77</b>	<b>1.10</b>	<b>0.69</b>	<b>1.03</b>
VREFCA	0.68	1.69	0.68	1.69	0.51	1.03	0.17	0.40
VDD	0.29	0.65	0.47	1.17	0.14	0.41	0.26	0.48

A similar trend of high susceptibility of the CA net across all nets is noted from the DDR4 induced voltages results (see Figure 12b and Table 4). The maximum values of induced voltages across CA nets for different chips positions are 0.98 V (chip 1), 0.83 V (chip 2), 0.77 V (chip 3), and 0.69 V (chip 4). The observed induced voltage levels for VREFCA and VDD nets are much lower than those across CA nets.

Figure 13 depicts the comparison of the coupled ESD noises across various nets of DDR3 and DDR4 modules. To compare with the results in Figure 13, the two most sensitive nets from each category of nets of Figure 12 are taken. For example, for CA nets, “chip 1—CA” and “chip 2—CA” traces are the most sensitive for DDR3 and DDR4 modules (see Table 3 and Table 4, respectively). Therefore, the comparison of “chip 1—CA” and “chip 2—CA” nets is performed to compare the induced voltages results of DDR3 and DDR4 in Figure 13. Similarly, two most susceptible traces from VREFCA and VDD categories are selected for the comparison results of Figure 13. For VREFCA case, the most sensitive traces are related to chip 1 and chip 2 for both memory modules. Furthermore, “chip 1—VDD” and “chip 2—VDD” are regarded as the most susceptible traces in both memory modules for the VDD case.



**Figure 13.** Comparison of induced voltages for most sensitive traces of DDR3 and DDR4 nets across all SODIMM chip positions: (a) CA; (b) VREFCA; and (c) VDD.

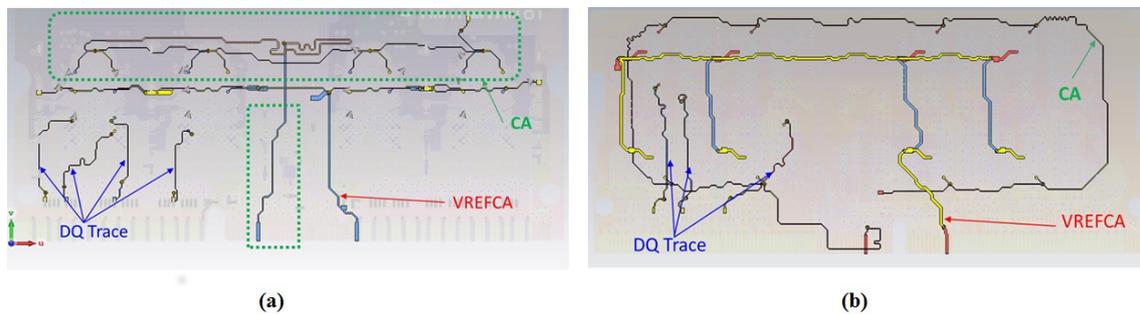
As shown in Figure 13 and Table 5, as expected, the coupled voltages for DDR4 module are around 60%, 58%, and 80% lower than the DDR3 module for CA, VREFCA, and VDD nets, respectively. The coupled voltage levels in DDR4 are lower than DDR3 due to the provided internal shielding by the separate ground plane in DDR4. The presence of additional separate ground (VDD) plane in DDR4 (see Figure 8b) limits the coupling noise as was also observed for the lower distributed current profile for DDR4 in Figure 10. Furthermore in DDR3, unlike DDR4, VDD plane configuration is routed along with other signal nets, which made it more sensitive to the coupled noise (80% higher induced voltage levels than those in DDR4). In addition to the two extra layers in DDR4, the installed decap values in DDR4 are also optimized (high concentration of 1  $\mu$ F decaps) to minimize the coupling noises, compared to installed decaps on DDR3, as illustrated in Table 6.

**Table 5.** Comparison of maximum induced voltages for most sensitive traces of DDR3 and DDR4 nets across all SODIMM chip positions (see waveforms in Figure 13).

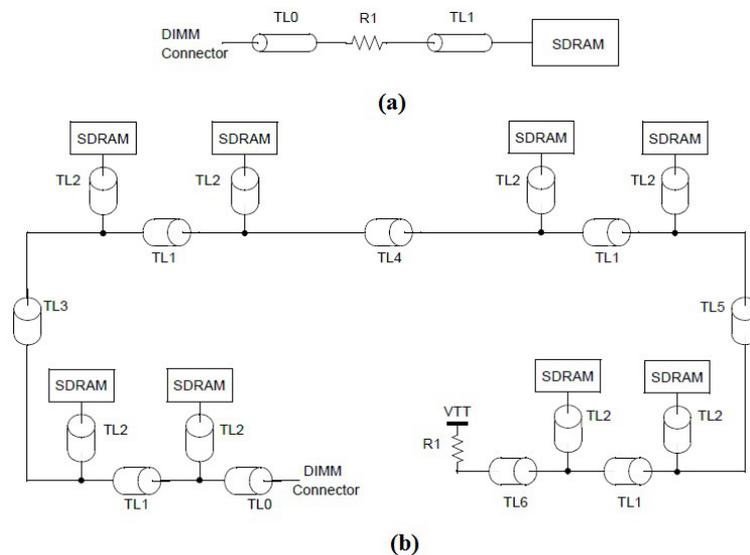
Trace	CA-Chip 1	CA-Chip 2	VREFCA-Chip 1	VREFCA-Chip 2	VDD-Chip 1	VDD-Chip 2
DDR3	2.48	2.21	1.61	1.52	1.60	1.48
DDR4	0.98	0.83	0.68	0.68	0.29	0.47
Reduction in DDR4 (%)	−60	−62	−58	−55	−82	−68

As shown in Figure 13, for both memory modules (DDR3 and DDR4), CA nets are the least immune to the coupled ESD noise. Figure 14 depicts the internal routing mechanism of analyzed nets on both memory modules. The illustration of the traces routing configuration is given in Figure 15. CA had higher induced voltages because the routing length of CA trace is almost 4–8 times longer than DQ nets [25], as elaborated in Figure 14. The CA nets have longer trace length because CA routing is across multiple layers with point-to-multiple-point (layers) connections, as illustrated in Figure 15b. In addition, CA nets have complex routing structure and capture higher routing portions compared to DQ signals which makes them more susceptible to noise than other traces. VREFCA nets are wider than CA nets but they are shorter than CA nets. Furthermore, VREFCA nets have relatively simple routing mechanisms compared to CA nets, which makes them less sensitive to the ESD noise than CA

nets across all chip positions. Overall, lower induced voltages are observed for VDD cases due to the plane structure of VDD as compared to CA and VREFCA traces.



**Figure 14.** Internal routing mechanism of the DQ, CA and VREFCA nets on memory modules: (a) DDR3; and (b) DDR4 (to save space, the traces routes have been overlapped).



**Figure 15.** Nets routing configurations of DDR4 module: (a) DQ nets (point to point); and (b) address nets (point to multi-points (layers)) [25].

### 5. Analysis of Effect of Decaps on Coupled Noise on Sensitive Nets through DOE Methodology

The role of the on/off-chip decaps is vital for the reductions of the power supply coupling noises in ICs [26,27]. Such decaps are also used to prevent the oxide breakdown [28], power-ground noises [29] and conducted noises [14] due to a transient ESD event.

In this section, based on DOE methodology, series of simulation experiments are presented that analyzed the effect on the coupled ESD noises on memory modules nets for two cases: (1) change in the number of decaps; and (2) change in decaps values. All DOE analyses are performed for the off-chip or on-SODIMM board decaps in Figure 7. Table 6 shows the installation configuration of all off-chip decaps on DDR3 and DDR4, respectively. As shown in Table 6, DDR4 module has a high concentration of 1  $\mu F$  decaps ( $61 \times 1 \mu F$  decaps), while 100 nF decaps are the leading decaps in DDR3 ( $50 \times 100 \text{ nF}$  decaps).

**Table 6.** On-SODIMM board decaps installation configurations: DDR3 vs. DDR4.

Connection Planes	Installed Decaps	
	DDR3	DDR4
VREFCA-VDD	100 nF × 9 ea	0.1 μF × 8 ea
VREFDQ-VSS	100 nF × 9 ea	-
VDD-VSS(GND)	100 nF × 18 ea	
	220 nF × 9 ea	1 μF × 31 ea
	1 μF × 5 ea	
VTT-VDD	2.2 μF × 4 ea	
	100 nF × 14 ea	1 μF × 14 ea
VPP-GND	-	1 μF × 16 ea

The effect of the decaps on coupled ESD noises is analyzed with the simulation configurations of Figure 11, for input ESD noise of +2 kV. However, for brevity herein, the analysis results are reported only for the most sensitive identified net across all chips positions of DDR3 and DDR4 modules.

5.1. Effect of Change of Number of Decaps

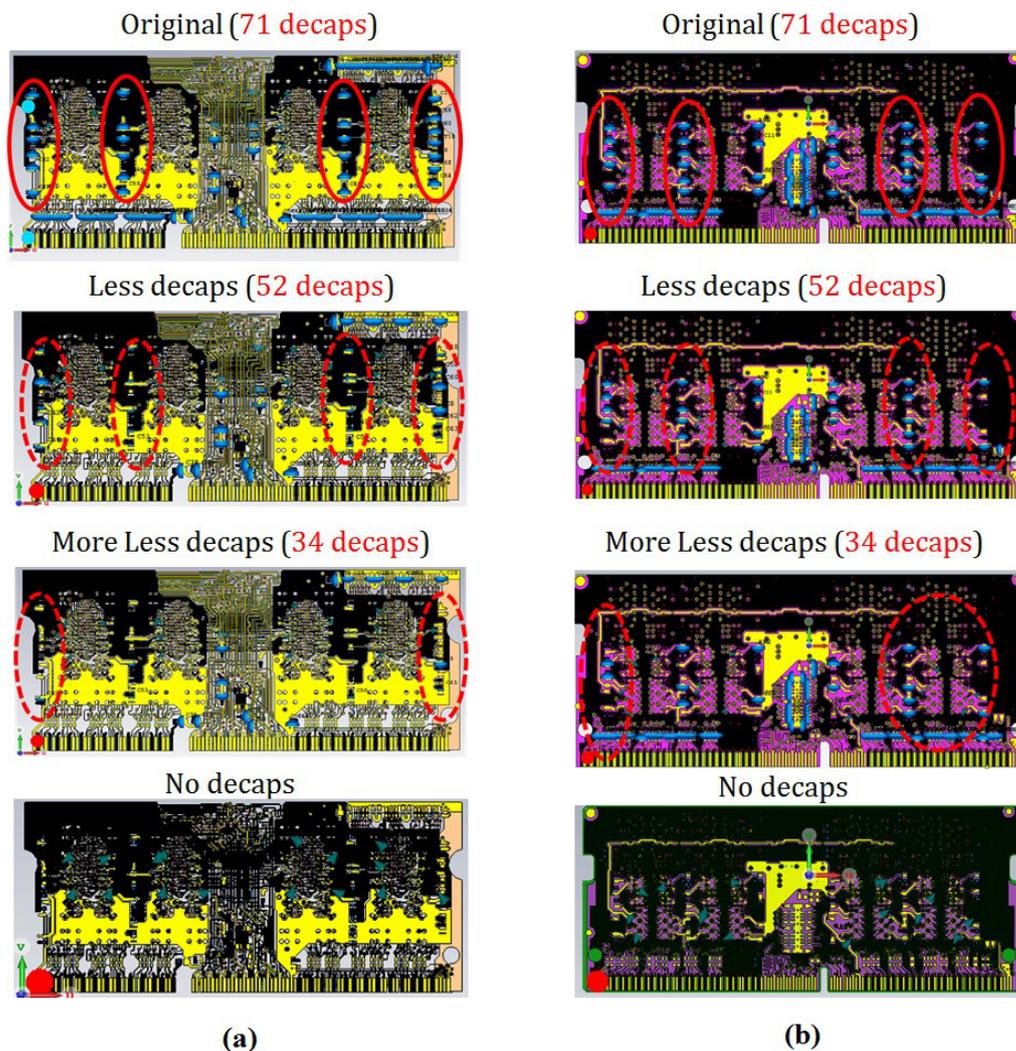
Table 7 illustrates the designed DOE simulations cases to evaluate the impact of the number of installed off-chip decaps on memory modules, on the coupled ESD noises. The analysis is performed for four cases of each module. Figure 16 depicts the cases in Table 7.

We change the passive decoupling capacitors that are mounted on the SODIMM board for the analysis of the cases in Table 7. For passive off-chip decaps, MLCC (multi-layer ceramic capacitor) is usually used for the memory modules as per their design files. For the on-chip (SODIMM chip) decaps, metal oxide semiconductor (MOS) and cell-type decaps are preferred [30]. However, the analysis of on-chip decaps is not in the scope of this study because the imported design files only contain information about the off-chip decap values and their installation positions.

As illustrated in Table 7, Case 1 is the original configuration in which no change in the already installed decaps on both memory modules is made. In Case 2, 19 decaps are removed from DDR3 while 21 are removed from DDR4 module to analyze the effect of fewerdecaps on induced noises. In Case 3, more decaps are removed, resulting in 34 installed decaps, for both DDR3 and DDR4 configurations. The decaps are removed from the positions around the SODIMM chips where the VMs are installed to monitor the induced noises, as illustrated in “dotted elliptical regions” in Figure 16. Case 4 depicts the worst case scenario and is simulated with no off-chip decap, as elaborated in “no decaps” pictures in Figure 16.

**Table 7.** ESD DOE simulation cases to analyze the change in number of decaps on coupled ESD noise (“#” shows the number of used decaps for each DOE case).

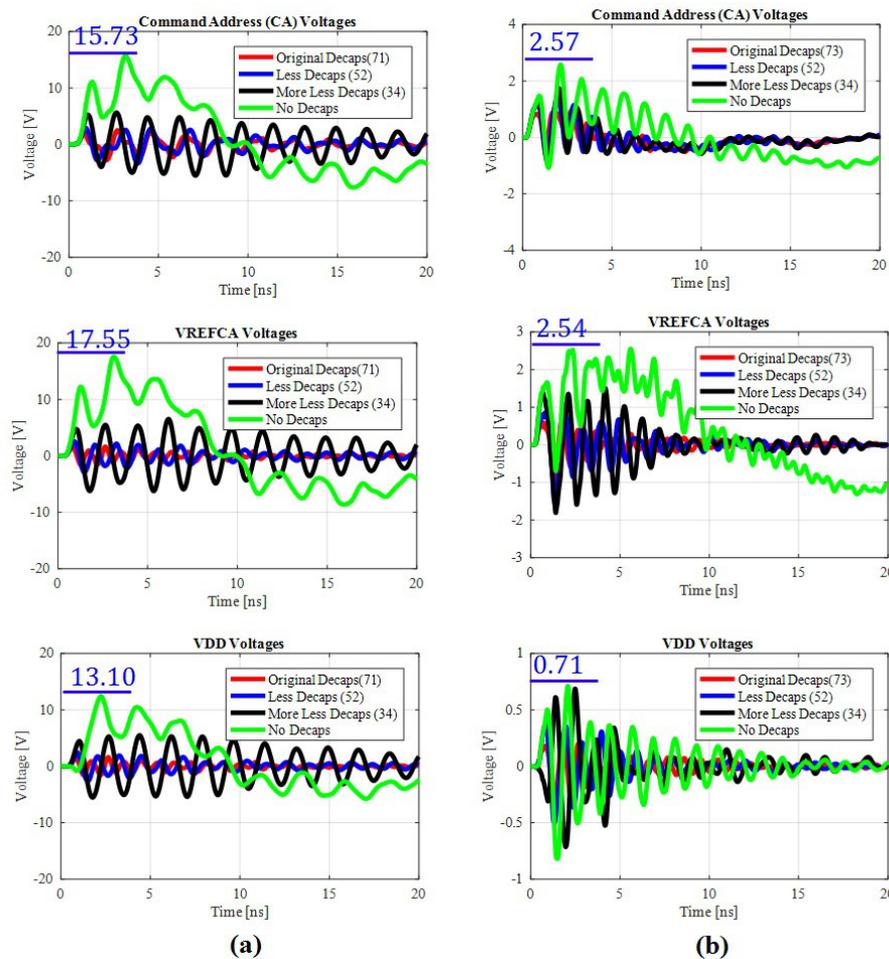
Case	1	2	3	4
<b>DUT</b>	<b>DDR3</b>			
Case Description	Original Decaps (71)	Less decaps (52)	More less decaps (34)	No decap
<b>DUT</b>	<b>DDR4</b>			
Case Description	Original Decaps (73)	Less decaps (52)	More less decaps (34)	No decap



**Figure 16.** DOE simulation cases to analyze the effect of number of decaps on induced ESD noises: (a) DDR3 module cases; and (b) DDR4 module cases.

The limitation of this analysis is that all DOE simulation configurations are analyzed for the ideal decap values for simplicity. The ideal decap values are taken because, when the JEDEC design files of the DRAM modules are imported in CST MWS, the lumped components values on the imported models were ideal with zero equivalent series resistance (ESR) and equivalent series inductance (ESL). The analysis could be performed with non-ideal decaps when accurate values of ESR and ESL of each decap are known.

Figure 17 shows the results of the DOE cases in Figure 16. Table 8 depicts the maximum and peak to peak (PP) voltages values of each waveform of Figure 17. It can be seen from the results in Figure 17 and Table 8 that, as expected, the highest values of induced voltage noises are observed for Case 4 (no decap) for all nets, in both modules. The induced voltage levels drop with the increase in the number of decaps, as can be confirmed from the results of Case 1 (original decaps configuration) in Figure 17 and Table 8. The maximum induced noise levels are 2.48 V, 1.61 V and 1.60 V for the CA, VREFCA, and VDD nets of DDR3, respectively, with 73 installed MLCC decaps. These values changed to 15.73 V, 17.55 V, and 13.10 V when all the decaps are removed (Case 4) from the memory module. This reflects the importance of the number of installed decaps on the module. These results imply that induced noise levels are inversely proportional to the number of installed decaps on memory modules.



**Figure 17.** DOE cases results to analyze the effect of number of decaps on induced ESD noises: (a) DDR3 module cases; and (b) DDR4 module cases.

**Table 8.** Comparison of coupled ESD noise voltages for various DOE cases in Figure 16 (waveform results in Figure 17).

Case #	1	2	3	4
<b>DDR3</b>				
Trace	Max [V]	PP [V]	Max [V]	PP [V]
CA	2.48	5.25	2.90	6.22
VREFCA	1.61	3.13	2.43	5.33
VDD	1.60	3.22	2.54	5.46
<b>DDR4</b>				
Trace	Max [V]	PP [V]	Max [V]	PP [V]
CA	0.98	1.49	1.45	2.17
VREFCA	0.68	1.69	1.07	2.70
VDD	0.29	0.65	0.37	0.84

As shown in Figure 17, the frequency of the induced noise signals decreases with the reduction in the number of decaps on the module. Furthermore, in Figure 17, the green color waveform (no decap case) is of low frequency compared with the other waveforms. The oscillation frequencies of voltage waveforms increase as we moved to the higher number of decap configurations. This shows that the decaps successfully filter the low frequency noises and results in lower voltage levels of the induced noises with original decaps configuration of Case 1, for both modules.

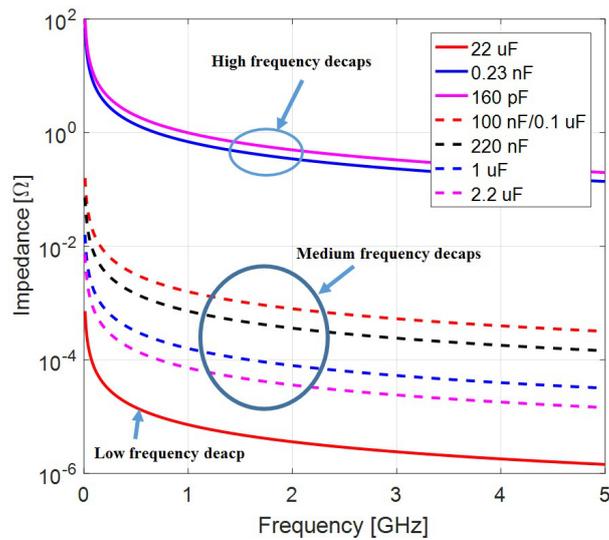
The comparison of induced voltage noises levels for DDR3 and DDR4 in Table 8 and Figure 17 illustrate that the coupled noise levels in DDR4 are 70–80% less than the observed voltage levels in DDR3. Even with no decap configuration (Case 4), the observed maximum noise voltage levels for CA, VREFCA, and VDD nets are 2.57 V, 2.54 V, and 0.71 V, respectively, for DDR4 module. The maximum voltage level of the most sensitive CA net (2.57 V) of DDR4 with no installed decap is similar to the coupled noise voltage of CA net (2.48 V) in DDR3 with all installed decaps. The maximum noise voltage level of VDD net (0.71 V) for Case 4 in DDR4 is 56% less than the recorded minimum VDD noise level of 1.61 V in DDR3 Case 1 configuration with all installed decaps. This suggests that, besides the number of installed decaps on memory modules, the role of the VDD and ground plane is also critical for the minimization of the coupled ESD noise. It is observed that the presence of isolated separate VDD and ground plane configuration in DDR4 significantly reduces the coupling noises from the ESD aggressor even for the worst case scenario of no installed decap on DDR4 module.

### 5.2. Effect of Change of Values of Decaps

The previous section presented an extensive analysis of the variations in the coupled ESD noise with the change in the number of installed decaps on memory modules. Next, variations in the induced ESD noise on highly sensitive CA, VREFCA, and VDD nets are analyzed by designing the DOE simulation configurations for the change in the values of the by-default installed decap values of Table 6, for both memory modules.

The determination of the changing decap values is based on the frequency of the coupled noise in the memory module traces. The oscillation frequency of the induced noise on CA nets is around 0.5 GHz and 1 GHz for DDR3 and DDR4 cases, respectively, as illustrated in Figure 17. The changing decap values needed to mitigate the corresponding frequency noises in the memory module nets.

The changing decap values on DRAM modules are 0.23 nF, 160 pF, and 22 μF. The comparison of the impedance results of already installed decaps, 100 nF, 220 nF, 1 μF, and 2.2 μF (see original configuration decap values in Table 6 for both DDR3 and DDR4), and that changed decap values is shown in Figure 18. All impedance results in Figure 18 are for the ideal conditions of decaps. The dotted waveforms in Figure 18 are for the already installed decaps on both modules, which actually belonged to the medium frequency region. The values of replaced decaps (0.23 nF, 160 pF, and 22 μF) are chosen intuitively to reduce both low and high frequency coupled ESD noises in various nets of memory modules. Figure 18 illustrates that 22 μF decap could be used for the mitigation of low frequency noises. The impedance results of 0.23 nF and 160 pF decaps reflect that their installation would filter out the high frequency noise component. For brevity in the discussion below, 22 μF decaps are referred to as low frequency (LF) decaps, while 160 pF and 0.23 nF decaps are referred to as high frequency (HF) decaps. The type of the changing decaps is the same i.e. MLCC decaps, as in the original configurations.



**Figure 18.** Comparison of impedance results of already installed (100 nF, 220 nF, 1  $\mu$ F and 2.2  $\mu$ F) ideal decaps and the changed decaps (0.23 nF, 160 pF, and 22  $\mu$ F) for DOE analysis.

The change in decaps values is done according to the DOE cases of Table 9. For each DRAM module, three different DOE configuration cases (Cases 5–7) are analyzed. The change of decap values in each DOE case is with respect to Case 1 (original configuration) of each module. In Case 5, high frequency decaps (160 pF) concentration on DRAM modules is increased while the number of low frequency decaps (22  $\mu$ F) is increased in Case 6. The purpose of designing Cases 5 and 6 is to analyze the impact of the presence of high concentration of high and low frequency mitigation decaps on memory modules on the induced noise. Case 7 is designed to have mixed low, medium and high frequency decaps on modules. Similar to the analysis presented in Section 5.1, all DOE configurations for the evaluation of the effect of the change in decap values are analyzed for ideal MLCC decap values. The change in decap values changed the impedance resonance profile of the module and eventually have an impact on the filtration of the induced ESD noise. The role of the ESR and ESL of decaps could be included when the exact values are known.

**Table 9.** DOE cases for the analysis of coupled ESD noise with the change in values of installed decaps on memory modules (NC: no change).

Connection Planes	VRREFCA-VDD	VREFDQ-VSS	VDD-VSS (GND)	VTT-VDD	VPP-GND	Total # of Changed Values Decaps
<b>DUT</b>			<b>DDR3</b>			
Case 1 (Original configuration)	100 nF × 9	100 nF × 9	100 nF × 18 220 nF × 9 1 μF × 5 2.2 μF × 4	100 nF × 14	-	
Case 5 (# of changed values decaps)	100 nF → 0.23 nF (9)	100 nF → 160 pF (9)	100 nF → 160 pF (13) 220 nF → 160 pF (6) 1 μF → 160 pF (5)	NC	-	42
Case 6 (# of changed values decaps)	100 nF → 22 μF (9)	100 nF → 22 μF (9)	100 nF → 22 μF (13) 220 nF → 22 μF (6) 1 μF → 22 μF (5)	NC	-	42
Case 7 (# of changed values decaps)	100 nF → 0.23 nF (5)	100 nF → 160 pF (5)	100 nF → 160 pF (12)	NC	-	22
<b>DUT</b>			<b>DDR4</b>			
Case 1 (Original configuration)	0.1 μF × 8	-	1 μF × 31	1 μF × 14	1 μF × 16	-
Case 5 (# of changed values decaps)	0.1 μF → 160 pF (8)	-	1 μF → 160 pF (31)	NC	NC	39
Case 6 (# of changed values decaps)	0.1 μF → 22 μF (8)	-	1 μF → 22 μF (31)	NC	NC	39
Case 7 (# of changed values decaps)	0.1 μF → 160 pF (4)	-	1 μF → 160 pF (14)	NC	NC	18

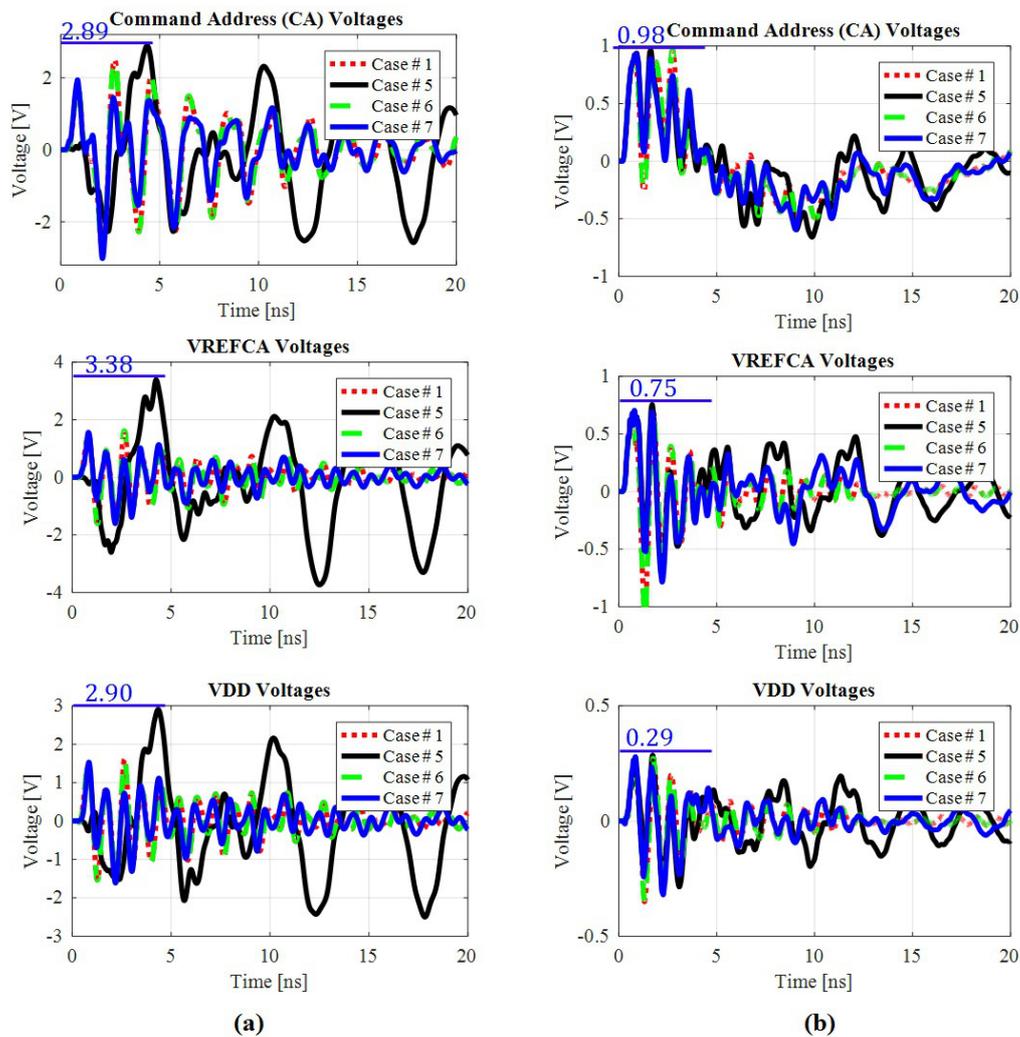
For DDR3 DUT, in Case 5, all decaps of VREFCA-VDD and VREFDQ-VSS planes are changed to 0.23 nF and 160 pF HF decaps, respectively. In addition, for VDD-VSS plane, 13 out of 18 100 nF, 6 out of 9 200 nF, and all 1  $\mu$ F decaps are replaced with HF 160 pF decaps. The total number of changed decaps in Case 5 is 42. The purpose of changing these decap values to 160 pF is to analyze the effect of the presence of a large number of HF decaps on the coupling noise on DDR3 nets. In Case 6, all 42 changed values decaps in the last case (Case 5) are replaced with LF 22  $\mu$ F decaps to investigate the impact of a large number of low frequency decaps on induced ESD noise on traces. In the last DOE case (Case 7), five out of nine 100 nF decaps installed across each VREFCA-VDD and VREFDQ-VSS planes are replaced with 0.23 nF and 160 pF HF decaps, respectively. The 12 100 nF decaps connected between VSS and VDD planes are changed to 160 pF decaps, making the total number of changed decaps for this case to 22. Out of 71 total decaps on DDR3 module, 22 decaps values are changed to HF decaps, which makes this case a mixed frequency decaps analysis case.

Similarly, for DDR4 module, in Case 5, all 0.1  $\mu$ F decaps of VREFCA-VDD plane and 1  $\mu$ F decaps of VDD-VSS plane are replaced with HF decaps of 160 pF. The last changed 39 decaps of 160 pF were changed to 22  $\mu$ F in Case 6 to make it low frequency DOE analysis configuration. Lastly, 18 capacitors installed across VREFCA-VDD and VDD-VSS planes are changed to 160 pF decaps in Case 7.

Figure 19 depicts the comparison of the results of the DOE analysis cases of Table 9 for DDR3 and DDR4 memory modules. Table 10 shows the maximum and peak to peak voltage values of each trace of Figure 19. In Table 10, the results of only Cases 5–7 are compared with the original configuration of Case 1, because, we want to analyze the impact of the change in decap values on the coupled ESD noises. The effect of the change in the number of decaps on induced noise is already discussed in Table 8. As shown in Figure 19, the change in decaps values brought significant variations in the noise voltage levels and their associated oscillation frequencies for both modules.

**Table 10.** Comparison of coupled ESD noise voltages for various DOE cases in Figure 19 (waveform results in Figure 19) (bold: minimum value; underline: maximum value).

Case	1		5		6		7		
<b>DUT</b>		<b>DDR3</b>							
Trace	Max [V]	PP [V]	Max [V]	PP [V]	Max [V]	PP [V]	Max [V]	PP [V]	
CA	2.48	5.25	<u>2.89</u>	5.47	2.48	5.25	<b>1.94</b>	4.96	
VREFCA	1.60	3.13	<u>3.38</u>	7.12	1.61	3.22	<b>1.56</b>	3.16	
VDD	1.61	3.22	<u>2.90</u>	5.40	1.60	3.13	<b>1.53</b>	3.14	
<b>DUT</b>		<b>DDR4</b>							
CA	<u>0.98</u>	1.49	0.96	1.61	0.96	1.46	<b>0.93</b>	1.52	
VREFCA	<u>0.68</u>	1.69	0.75	1.41	0.68	1.69	0.70	1.48	
VDD	<u>0.29</u>	0.65	0.28	0.57	0.27	0.62	<b>0.27</b>	0.59	



**Figure 19.** Comparison of DOE cases results to analyze the effect of change in decaps values on induced ESD noises: (a) DDR3 module cases; and (b) DDR4 module cases.

Figure 19a shows the results for the DOE configurations of DDR3. For all three nets in DDR3, maximum noise voltages are recorded for Case 5 with low frequency oscillations of the noise signals (solid black lines). The reason is that, as we replaced many (42) decap values to HF decap (160 pF) in this case, the high frequency noise that is present in the original configuration (Case 1) is filtered out. It increases the noise level of the coupled low frequency noise components in Case 5. The reverse happens for Case 6, in which 42 decap values are changed to LF (22 μF) decaps. Consequentially, it removes the low frequency noise, which is observed in Case 6. The net waveform results of this DOE case (Case 6) look similar to the original configuration results. The presence of the mixed frequency (low, medium and high) decaps in DOE Case 7 results in the filtration of both low and high frequency noises. Thus, it reduces the overall maximum and peak to peak noise levels, as can be noted from the blue curve results in Figure 19a and bold numerical values in Table 10 for all nets. In Table 10, the bold numerical values represent the minimum level of the recorded noise level while the maximum observed noise levels are underlined.

The comparison of the results for the different DOE configurations of DDR4 in Figure 19b depicts a similar behavior to that observed for DDR3 cases. As in DDR3, minimum noise levels are observed for the case where memory modules involve mixed frequency decaps, i.e., Case 7 (see blue traces in Figure 19b and bold values in Table 10 for DDR4 DUT). The variations in noise voltages are not as significant for various DOE configurations of DDR4 as those observed for DDR3 module. This reflects

the contribution of the two extra (VDD and ground) layers in DDR4 to control the overall level of coupling noises irrespective of the change in the decap values. The extra shielding offered by the isolated ground plane reduced the coupling noise. In addition, the power traces are routed through isolated VDD plane in DDR4, which minimizes the mutual interactions of the power trace with the CA and VREFCA nets. The mutual combination of both VDD and ground plane brought a comprehensive reduction in the induced noise levels for the DDR4 module. This reflects that the introduction of the separate planes for ground and power traces in the memory stack-up could make the device less prone towards the coupling ESD noises.

### 5.3. Analysis Summary

The findings of the DOE analysis suggests that CA trace is the most sensitive for all chips in both DDR3 and DDR4 modules. Almost 70–80% less noise voltage levels are recorded in DDR4 as compared to DDR3 owing to the internal stack-up structure of DDR4. Induced voltage level increases with the reduced number of decaps while the frequency of induced signal decreases. The mixed frequency (low, medium, and high) decaps are important to reduce ESD induced noise for CA and VREFCA nets. For VDD nets in DDR4, reduction of plane impedance is required as the change of decaps number and values did not significantly impact the induced voltage levels for VDD nets.

## 6. Conclusions

In this study, an extensive analysis of the ESD coupling noises on various nets (CA, VREFCA, and VDD) of two high-speed memory modules (DDR3 and DDR4) is performed. The analysis is conducted for seven different design of experiment (DOE) analysis configurations based on the change in the number of installed decaps and their values for each module. The distributed ESD noise current levels on DDR4 are almost 5 dB lower than DDR3 while 70–80% reduction in the coupling ESD noise voltage levels is observed in DDR4 DRAM, compared to DDR3 module. It is found that power routing through a separate ground plane and provision of an isolated ground plane in memory module played a significant role in the reduction of the coupling ESD current and voltages noises. In addition, the high possible number of decaps with decap values covering low, medium and high frequency bands proved to be the optimal configuration to reduce the maximum coupling noises along with separate VDD and ground plane stack-up configuration. Possible future work could involve the analysis of the impact on coupled ESD noise by including the effect of on-chip decaps and/or using of non-ideal characteristics of the decaps in DOE analysis.

The proposed analysis procedure based on DOE analysis and findings of this study could be very useful for the memory community designers. The memory designers could perform the ESD coupling noise analysis of the designed products using suggested full-wave EM simulation method, prior to the final manufacturing of the product to make the more robust design.

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**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

DOE	Design of experiment
ESD	Electrostatic discharge
3D	Three-dimensional
HCP	Horizontal coupling plane
DRAM	Dynamic random access memory
JEDEC	Joint electron device engineering council
SODIMM	Small outline dual in-line memory module
Decap	Decoupling capacitor
MWS	Microwave studio
CA	Command address
DQ	Data signal
GND	Ground
VREFCA	Reference voltage for command address
OEM	Original equipment manufacturer
MLCC	Multi-layer ceramic capacitor
MOS	Metal oxide semiconductor
EM	Electromagnetic
DUT	Device under test
IC	Integrated circuit
PCB	Printed circuit board
VM	Voltage monitor
$\mu$ -strip	Microstrip
PP	Peak to peak
MAX	Maximum
ESR	Equivalent series resistance
ESL	Equivalent series inductance
LF	Low frequency
HF	High frequency

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