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A Low-Voltage Multi-Band ZigBee Transceiver

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Abstract: This paper presents a low-voltage ZigBee transceiver covering a unique frequency band of 780/868/915/2400 MHz in 180 nm CMOS technology. The design consists of a receiver with a wideband variable-gain front end and a complex band-pass filter (CBPF) based on poles construction, a transmitter employing the two-point direct-modulation structure, a Σ-Δ fractional-N frequency synthesizer with two VCOs and some auxiliary circuits. The measured results show that under 1 V supply voltage, the receiver reaches –93.8 dBm and –102 dBm sensitivity for 2.4 GHz and sub-GHz band, respectively, and dissipates only 1.42 mW power. The frequency synthesizer achieves –106.8 dBc/Hz and –116.7 dBc/Hz phase noise at 1 MHz frequency offset along with 4.2 mW and 3.5 mW power consumption for 2.4 GHz and sub-GHz band, respectively. The transmitter features 2.67 dBm and 12.65 dBm maximum output power at the expense of 21.2 mW and 69.5 mW power for 2.4 GHz and sub-GHz band, respectively.

Keywords: ZigBee; low-voltage; transceiver; multi-band; CMOS

1. Introduction

Wireless sensor network (WSN) is one of the research hotspots in the current information field with a wide application prospect. How to minimize the power consumption is an important issue when designing the sensor network nodes and other wireless communication systems as well. Compared with baseband circuits, RF circuits account for most of the system power consumption, while each performance index of an RF transceiver has a certain tradeoff with power consumption [1]. Thus, how to reduce the power consumption while ensuring the RF performance has become one of the research hotspots and difficulties [2]. Generally, the RF transceiver is comprised of the low noise amplifier (LNA), mixer, band-pass filter, IF amplifier, power amplifier (PA), frequency synthesizer, and several other circuit modules. Several methods have been proposed to improve the traditional transceiver structure by integrating multiple functions in one module or reusing bias current in multiple modules [3–7]. For each module in the transceiver, the traditional design optimization theory is mainly aimed at the improvement of circuit performance while less consideration is given to power saving [8–12]. In order to minimize the power consumption of the WSN system fundamentally, attention should be paid both to the system architecture and to the circuit modules.

Currently, the research and design of a low-power ZigBee transceiver are mainly focused on 2.4 GHz frequency band [13–15]. Few studies concentrated in sub-GHz frequency band transceiver are reported [16,17]. A reconfigurable sliding-IF transceiver covering 400 MHz and 2.4 GHz bands was proposed in 2013 [18]. No research of a transceiver covering full ZigBee band has been reported. This paper presents a ZigBee transceiver covering 780/868/915/2400 MHz frequency bands, focusing on both low-power and performance improvements. Specific design methods and optimization

strategies are presented, including the implementation method of two VCOs in the two-point delta-sigma modulation frequency synthesizer for wideband operation, the graphical solution for parameter determination in the receiver front end to achieve the compromise between conversion gain, noise figure, input matching, and power consumption, and the pole structure-based design method for power saving and circuit simplification in a complex band-pass filter (CBPF). The paper is organized as follows. System architecture and consideration of the ZigBee transceiver are described in Section 2. Low-voltage and low-power RF transmitter/receiver circuit designs are demonstrated in Section 3 and 4, respectively. Section 5 presents the experimental results of the implemented transceiver, and Section 6 concludes this work.

2. ZigBee Transceiver Architecture

2.1. Transceiver Architecture

Figure 1 shows the block diagram of the proposed low-voltage multi-band ZigBee transceiver. The receiver employs low-IF structure for its high integration level, low cost, and reasonable dc offset and 1/f noise. The transmitter employs the direct digital modulation structure to produce constant envelope signals containing phase information only by controlling the frequency synthesizer directly, such that the hardware overhead and power consumption can be minimized.

The receiver, consisting of a front end, a CBPF, a limiter, and a 1-bit ADC, adopts a fully differential structure to weaken the effect of bond wires. The IEEE 802.15.4 standard specifies the data rate utilizing a direct sequence spread spectrum (DSSS) and O-QPSK modulation, of which the signal amplitude contains no useful information. Therefore, the output signal of CBPF can be handled directly by the limiter for digital signal converting.

The transmitter is comprised of a two-point modulation fractional-N PLL, as shown in Figure 2, and a PA. The digital baseband signal is injected to control the frequency dividing ratio of the divider and the tuning voltage of the VCO simultaneously to maintain the dynamic locking of the loop, which ensures the stability of the carrier frequency of the transmitter and avoids frequency shift [19].

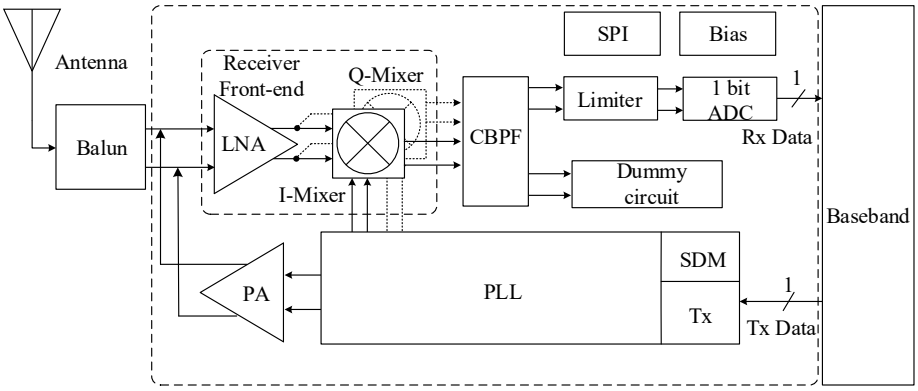


Figure 1. Block diagram of the proposed low-voltage multi-band ZigBee transceiver.

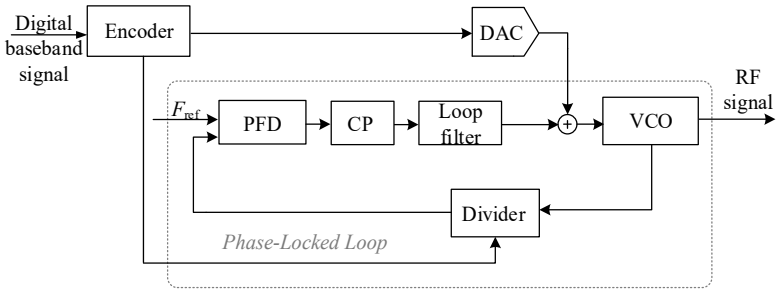


Figure 2. Block diagram of the two-point modulation PLL.

2.2. System Consideration

WSN has a total of 31 channels on a global scale according to IEEE 802.15.4 protocol [20], and the center frequency (f_C), modulation mode, and chip rate (F_{chip}) of baseband signals are shown in Table 1. The frequency synthesizer should provide the frequency of $f_C - f_{IF}$ (f_{IF} = 2 MHz) and $f_C \pm F_{chip}/4$ in receiving and transmitting mode, respectively. In all, the output frequency range of the frequency synthesizer ought to be 778–925 MHz and 2403–2481 MHz with the frequency resolution of 100 kHz.

To ensure that the down-converted product of the jamming signal in the receiver would not affect the signal-to-noise ratio (SNR), the following relationship should be satisfied [21]

$$L < P_{\text{Sig}} - P_{\text{Int}} - SNR_{\min} - 10\log(BW) \quad (1)$$

where P_{Int} is the power of the interference signal, P_{Sig} is the power of the useful signal, and L is the phase noise of the LO signal. The required $SNR_{\min}$ was 0.5 dB [22] and the channel bandwidth BW was 2 MHz. In IEEE 802.15.4 protocol, P_{Int} is likely to be 20 dB and 30 dB greater than P_{Sig} at 1 MHz and 3 MHz frequency offset, respectively, which resulted in the requirement of phase noise lower than –83.5 dBc/Hz and –93.5 dBc/Hz, respectively.

In order to generate quadrature LO signals for the mixer in the receiver, a divide-by-2 frequency divider was adopted, which required that the oscillation frequency of the VCO should be double that of the output frequency of the frequency synthesizer. Thus, two individual VCOs were employed in the design, including VCO_H for high frequency band and VCO_L for low frequency band. Accordingly, two dual-modulus prescalers were employed to make sure that each one can work near the resonant frequency of the corresponding VCO, so that the amplitude requirement could be easily satisfied. In addition, the use of gated power technology can guarantee that when working in a high frequency band, the associated circuit for a low frequency band was dormant, and vice versa. The block diagram of the frequency synthesizer is presented in Figure 3. The reference frequency was 16 MHz.

Three gain levels (low, mid, and high), corresponding to three input signal ranges (–35 to approximately –20 dBm, –60 to approximately –35 dBm, and –85 to approximately –60 dBm), were set by adjusting the gain of the front end or the filter to enlarge the SFDR of the receiver. Accordingly, with 5 dB margins, the NF in mid and high gain mode should be lower than 45.5 dB and 20.5 dB according to the following relationship [21]

$$NF = 174\text{dBm/Hz} + P_{\text{sen}} - SNR_{\min} - 10\log(BW) \quad (2)$$

where P_{sen} is the RF receiver sensitivity.

With large input signals, the input IP_3 (IIP_3) was generally required to be 10 dB larger than IP1dB (>–20 dBm), that is –10 dBm. With small input signals, considering the influence of interference signals, the following relationship shall be satisfied [22]

$$\text{IIP}_3 > \frac{\left(3P_{\text{Int}} - P_{\text{Sig}} + SNR_{\min} + \text{margins}\right)}{2}. \quad (3)$$

With 5 dB margins, an interfering power of −52 dBm [22], and a minimum signal power of −82 dBm (3 dB above minimum sensitivity level), the expected IIP_3 was −34.25 dBm. The summary of indexes (NF and IIP_3) for the receiver at three gain levels is shown in Table 2.

Table 1. Center frequency, modulation mode, and chip rate of baseband signals for a wireless sensor network (WSN).

Frequency band (MHz)	Modulation mode	Chip rate F_{chip} (Mchip/s)	Center frequency f_C (MHz)
780	O-QPSK	1	780 + 2k, k = 0, …, 3
868	O-QPSK	0.4	868.3

915	O-QPSK	1	906 + 2*k*, *k* = 0, …, 9
2400	O-QPSK	2	2405 + 5*k*, *k* = 0, …, 15

Table 2. Summary of indexes (NF and IIP_3) for the receiver at three gain levels.

Index	Input signal ranges (dBm)	NF (dB)	IIP_3 (dBm)
Low gain level	−35~-20	--	>−10
Mid gain level	−60~-35	<45.5	--
High gain level	−85~-60	<20.5	>−34.25

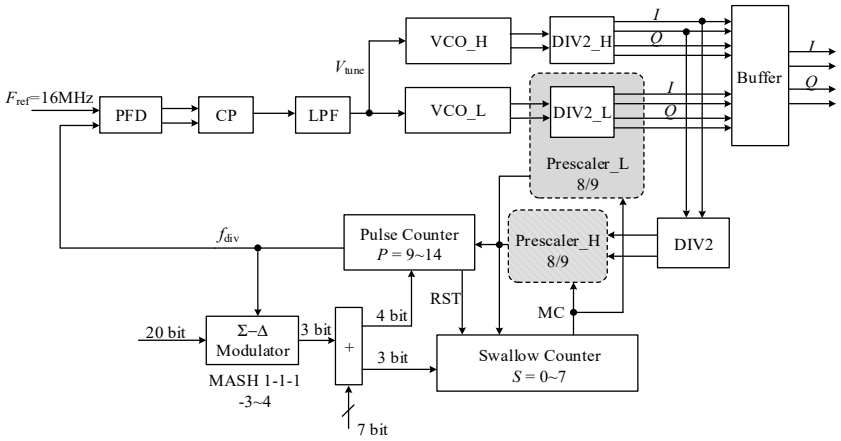


Figure 3. Block diagram of the frequency synthesizer for the WSN transceiver.

3. Transmitter Design

3.1. Implementation of Two-Point Modulation Frequency Synthesizer

The semi-cos-formed O-QPSK signal is known to be constant, of which the circular frequency ω_M can be expressed as

$$\omega_M = \omega_C + (-1)^m \cdot \frac{\pi}{2\tau} \tag{4}$$

where ω_C is the circular frequency of the carrier, and τ is the inverse of F_{chip}. Assuming b_k as the symbol of baseband signal, then

$$m = \begin{cases} not\left(b_k \text{ xor } b_{k-1}\right) & k=1,3,5,\cdots \\ b_k \text{ xor } b_{k-1} & k=2,4,6,\cdots \end{cases} \tag{5}$$

The frequency of the modulated signal can be calculated as

$$f_M = f_C + (-1)^m \cdot \frac{F_{chip}}{4} \tag{6}$$

Taking the high-frequency loop of the frequency synthesizer as an example, the block diagram of the two-point modulation system is depicted in Figure 4. When the enable signal *EN* is 1, the encoder computed the input baseband signal and generated the control signal *m*. Then, module G_{LP} switched the control word of the frequency divider ratio between +Δ*f Div Word* and −Δ*f Div Word* to achieve the frequency deviation of ± F_{chip}/4. Meanwhile, module G_{HP} switched the tuning voltage M_{tune} between m_{tune0} and m_{tune1}. The m_{tune0} and m_{tune1} were the output of the 8-bit DAC controlled by +Δ*f*

Mtune Word and −Δ*f Mtune Word*. It should be noted that the output tuning voltage of G_{HP} (M_{tune}) and output tuning voltage of CP (V_{tune}) were superimposed relationships, in which V_{tune} determined the carrier frequency f_C, and M_{tune} was used to control the frequency deviation. To avoid extra noise, M_{tune} and V_{tune} controlled two parallel variable capacitors of the VCO_H resonator, respectively. The control words +Δ*f Div Word*, −Δ*f Div Word*, +Δ*f Mtune Word*, and −Δ*f Mtune Word* were configured through in-chip integrated SPI.

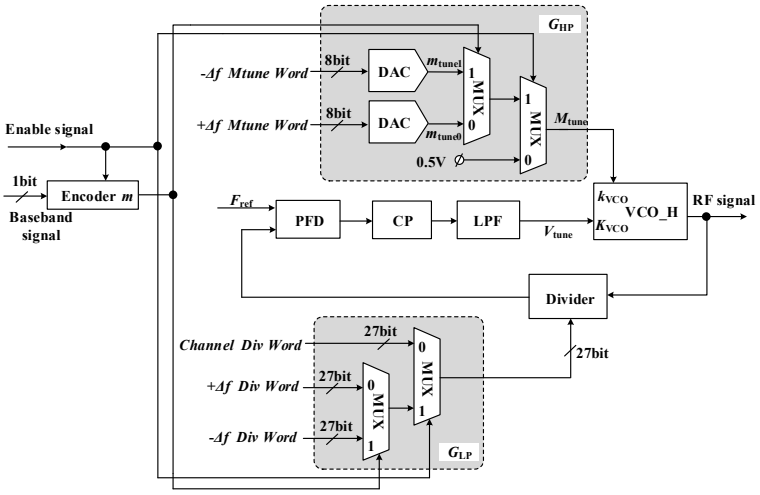


Figure 4. Block diagram of the two-point modulation system.

3.2. VCO

In order for VCO to have a wide frequency tuning range with relatively small tuning gain, a switched capacitor array for coarse frequency tuning was imposed on the basis of original variable capacitors. For VCO_H, a 3-bit switched capacitor array was utilized to achieve 8 levels of frequency coarse adjustment with 300 MHz/V tuning gain for each tuning curve. In order to guarantee equal open-loop transfer functions for high- and low-frequency loops in the frequency synthesizer to unify the parameters of the two loops and simplify the design of other modules like LPF, the tuning gain and divider ratio of the two loops should satisfy the following relationship

$$\frac{K_{VCO\_H}}{M_{\_H}} = \frac{K_{VCO\_L}}{M_{\_L}} \tag{7}$$

where K_{VCO_H} and K_{VCO_L} were the tuning gain of VCO_H and VCO_L, $M_{\_H}$ was the total divider ratio of high frequency loop, which was 300–310, and $M_{\_L}$ was the total divider ratio of the low frequency loop, which was 97–116. It was found that $M_{\_H}$ was approximately three times of $M_{\_L}$, which led to $K_{VCO\_L} = K_{VCO\_H}/3$ = 100 MHz/V. Thus, for VCO_L, a 4-bit switched capacitor array was employed to achieve 16 levels of frequency coarse adjustment with 100 MHz/V tuning gain for each tuning curve.

The schematic of VCO_H is shown in Figure 5(a). A CMOS complementary cross-coupling structure was chosen for its larger equivalent negative trans-conductance under the same bias current compared with NMOS cross-coupling structure, so that the starting condition for oscillation can be satisfied under smaller current and the power consumption can be reduced in consequence. The oscillation frequency was controlled by $SW_{0\text{-}2}$, V_{tune}, and M_{tune}. The current of VCO_H was controlled through the 4-bit switched resistors at the power and grounding end. In order to solve the voltage margin problem under low supply voltage, forward bias technology was employed in this design. Figure 6(a) presents the variation curves of threshold voltage V_{TH} and body-source leakage current i_{BS} of the NMOS transistor (W=20μm, L = 0.18μm) against V_{BS} under the bias condition of V_{GS} = 0.6 V and V_{DS} = 0.5 V. As can be seen from the figure, with the increase of V_{BS}, V_{TH} gradually decreased. When V_{BS} > 0.6 V, V_{TH} decreased slowly, while i_{BS} increased sharply, which is what should be avoided in the design. Thus, V_{BS} was finally set as 0.5 V, and the V_{TH} of the transistor was about 0.4

V, which made the complementary cross-coupling structure work normally under the supply voltage of 1 V. R_{B1}–R_{B4} are current-limiting resistors for reducing the substrate leakage current caused by the using of forward bias technology.

The variable capacitor unit utilized accumulation MOS tube, which has a larger tuning range and smaller parasitic resistance and the capacitance is monotonous against control voltage. The schematic of the conventional variable capacitor unit is shown in Figure 5(b), and the *C-V* characteristic curves are shown in Figure 6(b). As can be seen from Figure 6(b), the voltage-controlled characteristic of the conventional variable capacitor was not fully utilized. To improve the performance, blocking capacitor C_B and resistor R_B were employed to add a bias voltage V_{bias} to the gate of the MOS tube, as presented in Figure 5(c), so that the *C-V* characteristic curve can shift with V_{bias} and the variable capacitance can be fully exploited, as shown in Figure 6. The schematic of the switching capacitor array is demonstrated in Figure 5(d).

An automatic frequency calibration (AFC) module was utilized to automatically select an appropriate tuning curve for VCO to make sure that the frequency synthesizer could work in the expected frequency range. The basic principle of the AFC is to measure the output frequency of the VCO under different control words using a counting method and to find a set of control words which is closest to corresponding to the frequency that needs to be locked. The block diagram of AFC is presented in Figure 7(a) and the work flow chart is demonstrated in Figure 7(b). The function of the 32 divider in AFC is to reduce the output frequency of the VCO, so that the frequency divided signal could be processed directly by the digital circuits. The accuracy of AFC should be less than half of the frequency difference between the center points of two adjacent tuning curves. There were 8 tuning curves in VCO_H, and the frequency difference between the two adjacent curves was 150 MHz. Therefore, the frequency accuracy of AFC needed to be less than 75MHz.

When the tuning voltage V_{tune} was 0.5 V, the measured results of the AFC function of VCO_H under different channel codes *Channel* [3:0] are shown in Table 3. It can be seen from the table that the AFC functioned correctly, and the maximum frequency deviation after locking was 32MHz, which met the index requirement.

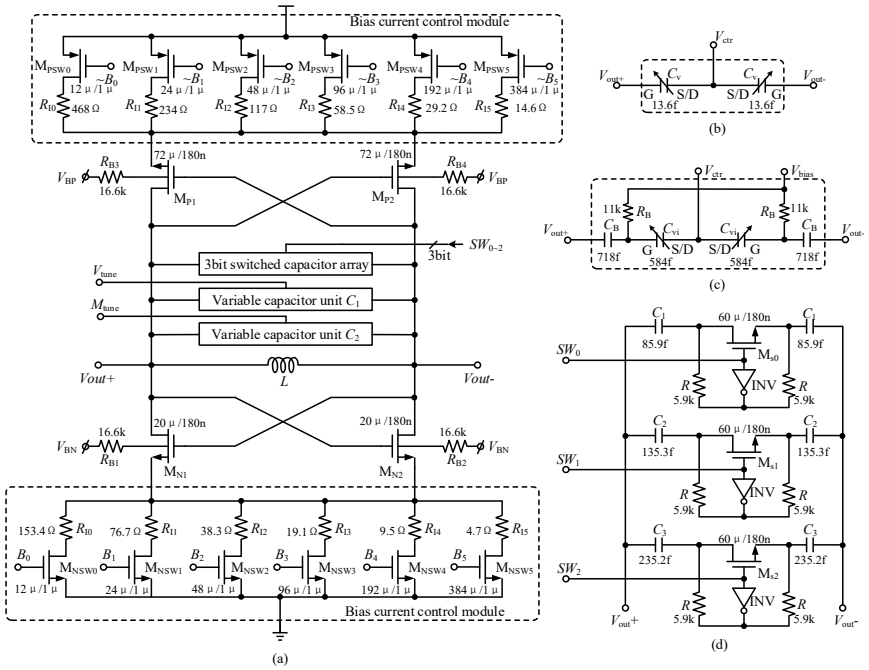


Figure 5. Schematic of (**a**) VCO_H, (**b**) conventional variable capacitor unit, (**c**) improved variable capacitor unit, and (**d**) switching capacitor array.

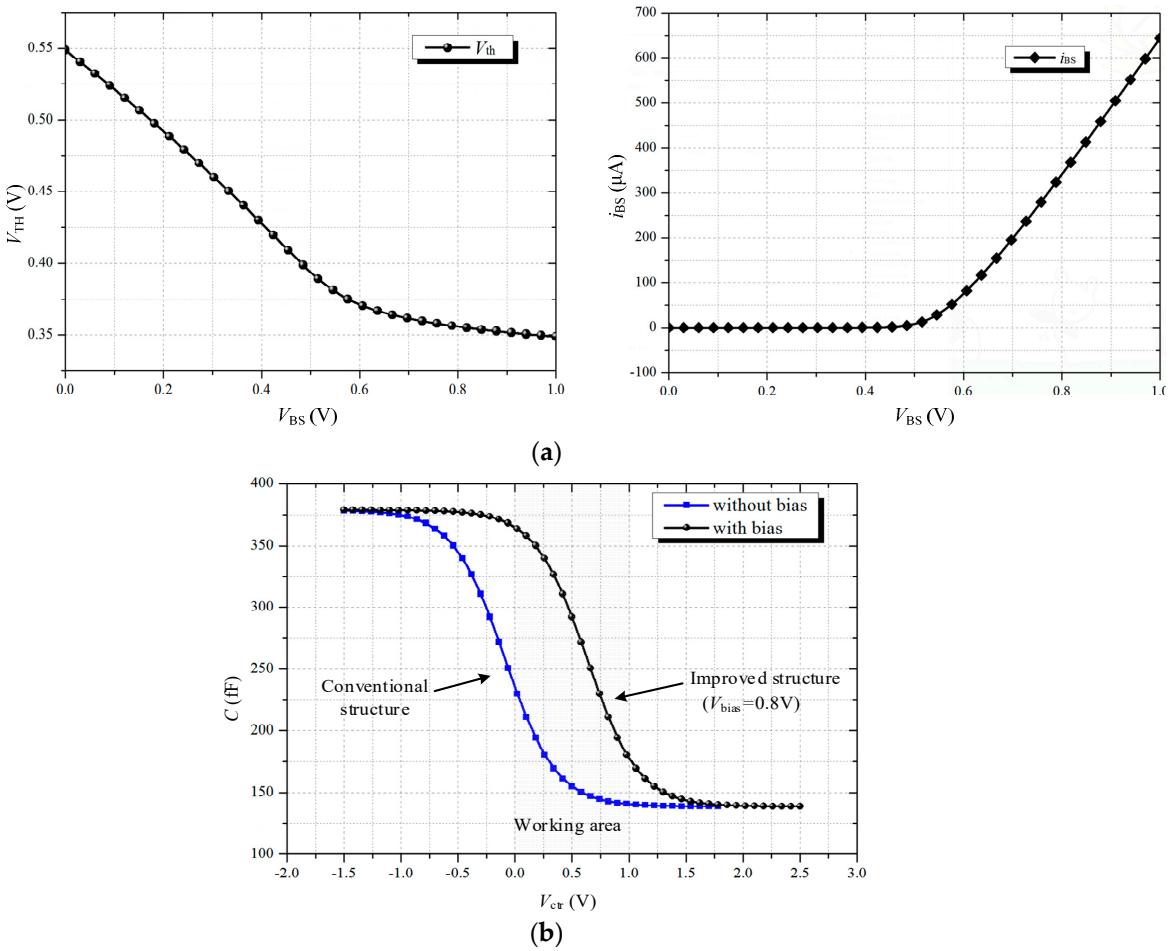


Figure 6. (**a**) The variation curves of V_{TH} and i_{BS} against V_{BS}, (**b**) C-V characteristic curves of the variable capacitor unit.

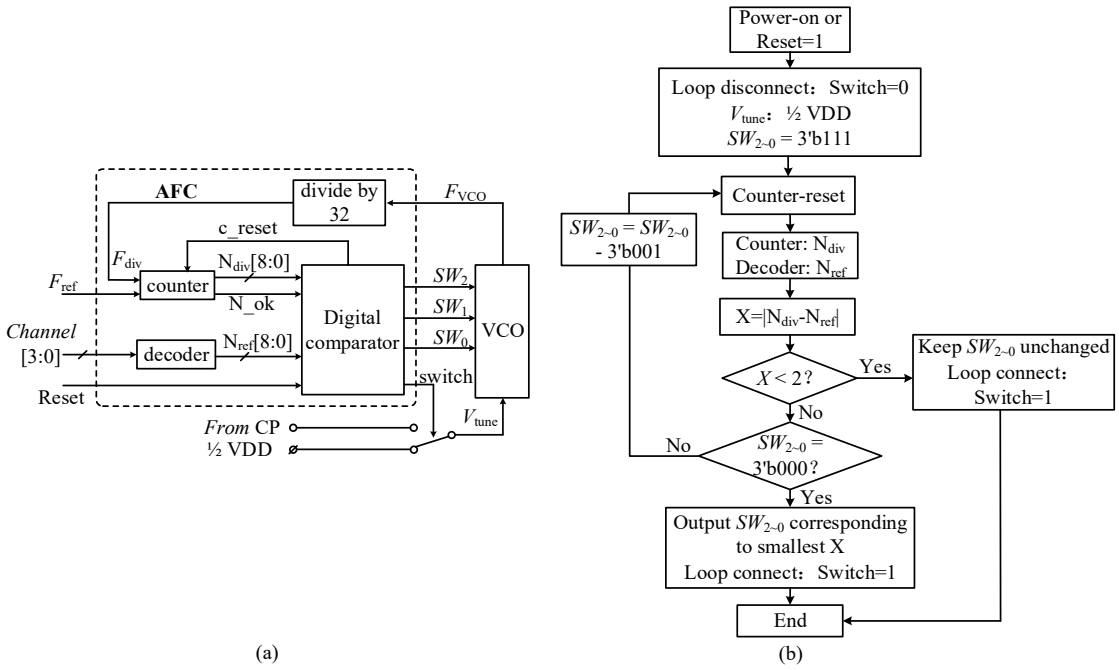


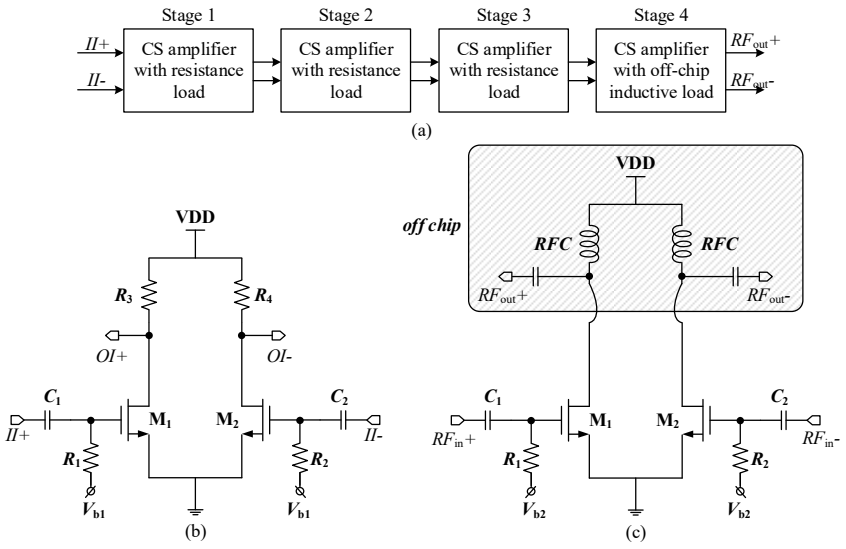
Figure 7. (**a**) Block diagram, (**b**) work flow chart of the AFC.

Table 3. Measured results of the AFC function of VCO_H under different channel codes *Channel* [3:0] with 0.5 V V_{tune}.

Channel [3:0]	Locked $SW_{2\text{-}0}$	Output frequency divided by 2/MHz	Channel center frequency/MHz	Frequency deviation/MHz
4′b0000	3′b101	2413	2405	8
4′b0001	3′b101	2413	2410	3
4′b0010	3′b101	2413	2415	2
4′b0011	3′b101	2413	2420	7
4′b0100	3′b101	2413	2425	12
4′b0101	3′b101	2413	2430	17
4′b0110	3′b101	2413	2435	22
4′b0111	3′b101	2413	2440	27
4′b1000	3′b101	2413	2445	32
4′b1001	3′b100	2481	2450	31
4′b1010	3′b100	2481	2455	26
4′b1011	3′b100	2481	2460	21
4′b1100	3′b100	2481	2465	16
4′b1101	3′b100	2481	2470	11
4′b1110	3′b100	2481	2475	6
4′b1111	3′b100	2481	2480	1

3.3. PA

PA is composed of four stages differential common-source (CS) amplifiers. The first three stages adopt resistance load and the last stage adopts off-chip Bias-T as inductive load. The block diagram, circuit structure, and component parameters of PA are shown in Figure 8.



	M1/M2(W/L) (μm/μm)	C1/C2 (fF)	R1/R2 (kΩ)	R3/R4 (Ω)
Stage1	24/0.18	114.6	21.7	671.7
Stage2	24/0.18	114.6	21.7	671.7
Stage3	48/0.18	114.6	21.7	265.3
Stage4	576/0.18	951.6	21.7	--

Figure 8. Schematic of a power amplifier (PA) (**a**) block diagram, (**b**) structure of common-source (CS) amplifier with resistance load, (**c**) structure of CS amplifier with off-chip inductive load.

4. Receiver Design

4.1. Receiver Front End

Figure 9 demonstrates the schematic of the receiver front end employing current reuse and active g_m-boosting technologies for power saving and gain enhancement, respectively. M_{SW} is a gain-control switch controlled by signal D_0. When D_0 is low, M_{SW} is in cut-off state, which has little effect on the circuit. When D_0 is high, M_{SW} is in conduction state and can be equivalent to a small resistor, which is in parallel with the resistance load R_{LOAD} in the circuit. Thus, it can reduce the gain of the receiver front end.

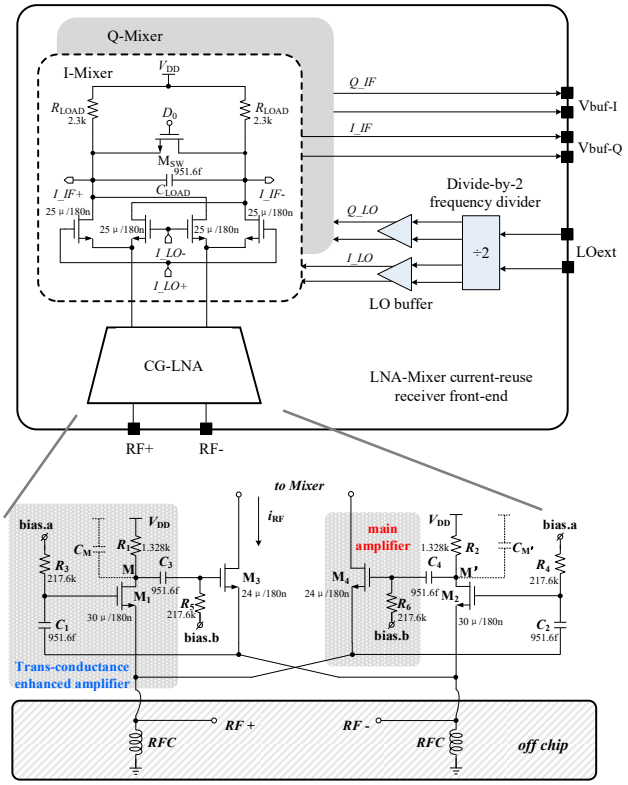


Figure 9. Schematic of the receiver front end.

The conversion gain (G_V) and input admittance ($Y_{IN\text{-}D}(j\omega)$) of the differential LNA-mixer current-reuse receiver front end can be respectively derived as

$$\begin{aligned} G_V &= \frac{1}{\pi} G_M R_{LOAD} = \frac{1}{\pi}(1+A_{boost}) g_{m3} R_{LOAD} \\ &= \frac{1}{\pi}\left(1+2g_{m1}\frac{R_1}{\sqrt{1+(2\pi f R_1 C_M)^2}}\right) g_{m3} R_{LOAD} \\ &= \frac{1}{\pi}\left(1+2g_{m1}R_{EQ}\right) g_{m3} R_{LOAD} \end{aligned} \tag{8}$$

$$\begin{aligned} Y_{IN\text{-}D}(j\omega) &= \frac{g_{m3}}{2}\left[1+A_{boost}(j\omega)\right]+g_{m1}+j\omega C_{in} \\ &= g_{m1}+\frac{g_{m3}}{2}+\frac{g_{m1}g_{m3}R_1}{1+(C_M R_1 \omega)^2}+j\omega\left(C_{in}-\frac{g_{m1}g_{m3}R_1^2 C_M}{1+(C_M R_1 \omega)^2}\right) \end{aligned} \tag{9}$$

where G_M is the equivalent trans-conductance of the common-gate LNA (CG-LNA), A_{boost} and R_{EQ} are, respectively, the voltage gain and the equivalent load impedance of the trans-conductance

enhanced amplifier, $g_{m1(3)}$ is the trans-conductance of $M_{1(3)}$, C_M is the equivalent load capacitance of nodal point M, and C_{in} is the parasitic capacitance of ESD and pads. R_{EQ} varies with R_1 and operating frequency f, as shown in Figure 10(a). To make a compromise between the conversion gain and the frequency bandwidth of the front end, $R_1 = 1$ kΩ was finally selected. On this basis, the blue curves in Figure 10(b) show the values of G_V against g_{m1} and g_{m3}. The shaded area in Figure 10(b) present the available g_{m1} and g_{m3} for Y_{IN-D} curve corresponding to the frequency range of 780–2400 MHz to fall within the circle $S_{11} < -10$ dB in the smith chart.

The CG-LNA using active g_m-boosting technology can provide enough gain to suppress the noise of the mixer [23], thus the main analysis and optimization of the NF were for trans-conductance circuit CG-LNA. The NF of CG-LNA (F_{CG_LNA}) can be written as

$$\begin{aligned} F_{CG\_LNA} &= F_{M3} + F_{M1} + F_{R1} \\ &= 1 + \frac{2\gamma}{\alpha g_{m3} R_S \left(1 + 2 g_{m1} R_1\right)^2} + \frac{\gamma}{2\alpha g_{m1} R_S} + \frac{1}{2 g_{m1}^2 R_1 R_S} \end{aligned} \tag{10}$$

where R_S is the source impedance, γ is the thermal noise coefficient of MOS transistors, and α is the ratio of g_m (trans-conductance) to g_{d0} (zero-bias drain conductance). Parameters γ and α are dependent on process and bias [24], and for BSIM v4.5 MOS transistor model, the value of γ/α can empirically be estimated as 2.5 [25]. The red curves in Figure 10(b) show the values of F_{CG_LNA} against g_{m1} and g_{m3}.

The parameter $\eta = g_m/I_D$ determines the trans-conductance that can be provided by unit bias current, which directly affects the power consumption of the circuit, and η is only determined by overdrive voltage V_{GS}-V_{TH} [26]. V_{GS} also affects the linearity of the circuit. Thus, a compromise between η and linearity was required to select the appropriate bias voltage V_{GS} for the front end. The current I_D can be approximately expressed as

$$I_D = c_1 V_{GS} + c_2 V_{GS}^2 + c_3 V_{GS}^3 \tag{11}$$

where c_i is the i_{th} harmonic coefficient of the current I_D, and c_1 is transistor trans-conductance g_m, c_3 is the main source of trans-conductance distortion. For NMOS transistors with gate length of 0.18 μm, the variation curve of g_m/I_D and $6c_3$ against V_{GS} is shown in Figure 11. It can be seen that the curve $6c_3$ against V_{GS} has a zero crossing when $V_{GS} = 0.6$ V, where the linearity of the trans-conductance circuit got the maximal value and g_m/I_D = 12.5 mS/mA, within reasonable limits. With limited power consumption, if V_{GS} is continually reduced in order to obtain a higher trans-conductance value, the value of c_3 will deviate from the zero point, resulting in a worse linearity, which is not worth the loss in the design of front end with a very critical linearity index. Thus, the value of η is finally determined as 12.5mS/mA in this design.

Eventually, the value of g_{m1} and g_{m3} were evaluated as 5mS and 2mS. As shown in Figure 10(b), the design point falls in the center of the shaded region, indicating a good input matching feature, an acceptable noise feature ($F_{CG-LNA} = 4$~5), enough conversion gain ($G_V > 25$ dB), and a restricted power consumption ($I_{D-total} = 2(g_{m1}+g_{m3})/\eta$).

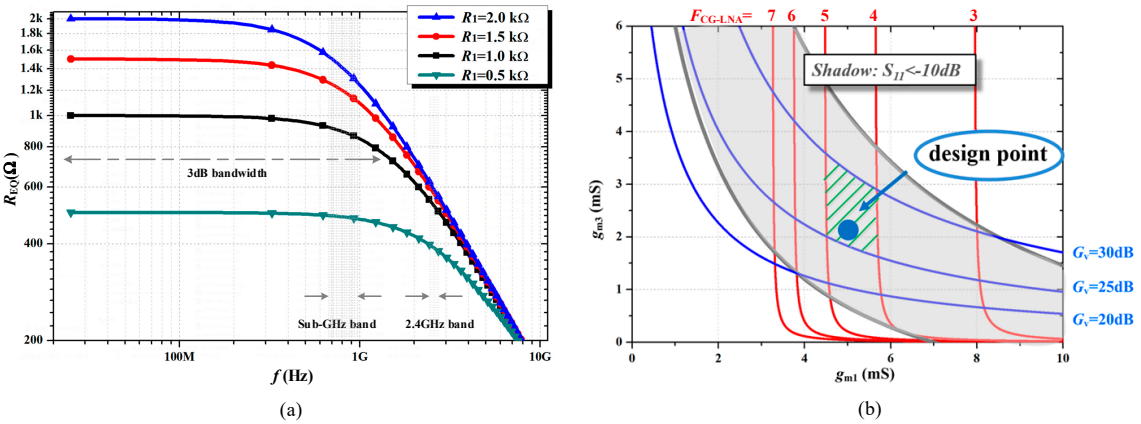


Figure 10. (**a**) Equivalent load impedance R_{EQ} against R_1 and f, (**b**) conversion gain G_V, NF F_{CG_LNA}, and input matching S_{11} against g_{m1} and g_{m3}.

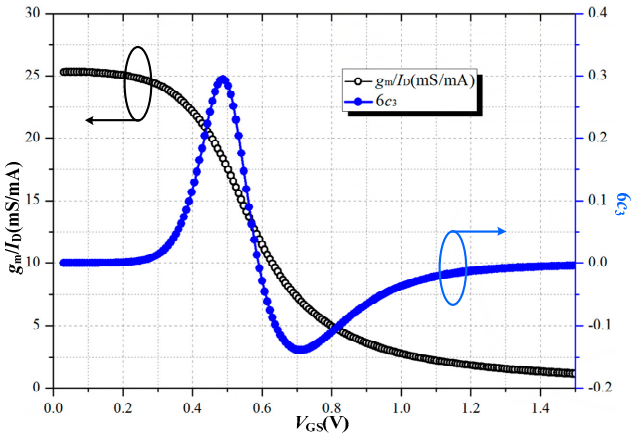


Figure 11. The variation curve of g_m/I_D and $6c_3$ against V_{GS}.

4.2. Complex Band-Pass Filter

The four-order CBPF employs G_m-C structure implemented based on the technique of poles construction to simplify the circuit and to reduce the power consumption to the utmost extent. The CBPF totally consumed 8 complex pole units, and the schematic of the unit circuit is shown in Figure 12. M_T and variable-resistance R constitute the trans-conductance unit (with the equivalent trans-conductance of G_m), M_Q, M_R, and C form the load unit, and M_S represents the frequency shifting unit which reused the current with trans-conductance unit. Gain control was achieved by changing the feedback resistance R, which was in parallel constituted by a fixed resistor R_F and a switch M_{SWF} controlled by signal D_1. It worked in a similar way to the gain control part of the receiver front end.

Assuming that $V_{in} = V_{I+} - V_{I-}$, $V_{out} = V_{OI+} - V_{OI-}$, $j \cdot V_{in} = V_{Q+} - V_{Q-}$, and $j \cdot V_{out} = V_{OQ+} - V_{OQ-}$, the transfer function of the complex pole unit can be written as

$$\frac{V_{out}}{V_{in}} = \frac{-G_m}{2sC + \left(g_{mQ} - g_{mR} - j \cdot g_{mS}\right)} \tag{12}$$

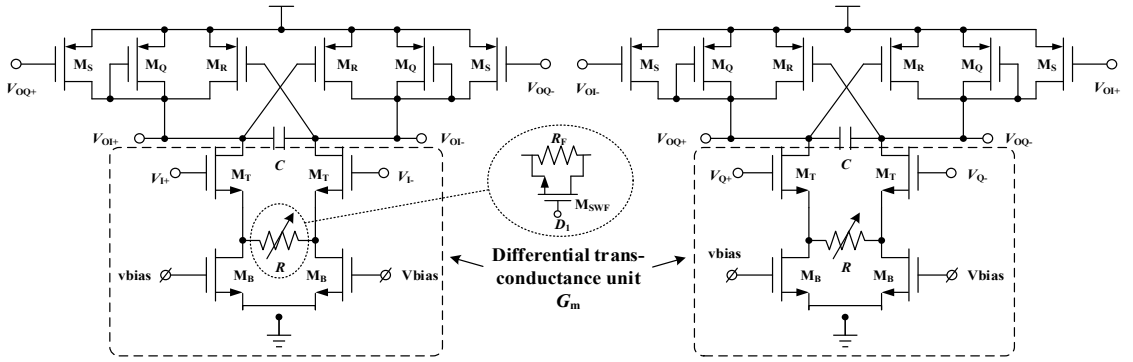
with one complex pole

$$P_{-3dB} = \frac{-g_{mQ} + g_{mR}}{2C} + j \cdot \frac{g_{mS}}{2C} \tag{13}$$

where g_{mS}, g_{mQ}, and g_{mR} are the trans-conductance of M_S, M_Q, and M_R. By choosing suitable parameters, four complex poles were constructed separately and then cascaded to finally compose the four-order CBPF with 2MHz bandwidth. The component parameters of each pole unit are listed in the table in Figure 12.

4.3. Modulator

Thanks to O-QPSK modulation, a simple limiting amplifier with a 1-bit ADC was employed as the modulator to amplify and shape IF signals output by CBPF to square wave signals which can be processed directly as digital signals in following digital modules. The limiting amplifier adopting a fully differential architecture utilized negative feedback structure for DC-offset cancellation, and the overall circuit block diagram, including four stages voltage amplifiers, A_1–A_4, and trans-conductance amplifiers, G_{m1} and G_{mF}, is shown in Figure 13. The small signal gain of the limiting amplifier was 54 dB. The schematic of the voltage amplifier is shown in Figure 14(a), and G_{m1}, G_{mF}, and R_D can be combined and achieved by the circuit structure shown in Figure 14(b). The block diagram of 1-bit ADC and the schematic of the internal comparator are presented in Figure 15.



	M_B(W/L) (μm/μm)	M_T(W/L) (μm/μm)	C (fF)	M_R(W/L) (μm/μm)	M_Q(W/L) (μm/μm)	M_S(W/L) (μm/μm)	R_F (kΩ)	M_{SW}(W/L) (μm/μm)
unit1	45/2	4/2	321.6	9/1.5	11/1.5	16/1.5	22.1	33/0.3
unit2	20/2	4/2	750.8	0.5/1.5	4/1.5	4/1.5	22.1	33/0.3
unit3	20/2	4/2	220	6/1	11/1	11/1	22.1	33/0.3
unit4	30/2	8/2	508	1.5/1	8.5/1	8/1	22.1	33/0.3

Figure 12. Schematic of the complex pole unit and component parameters of each unit used in complex band-pass filter (CBPF).

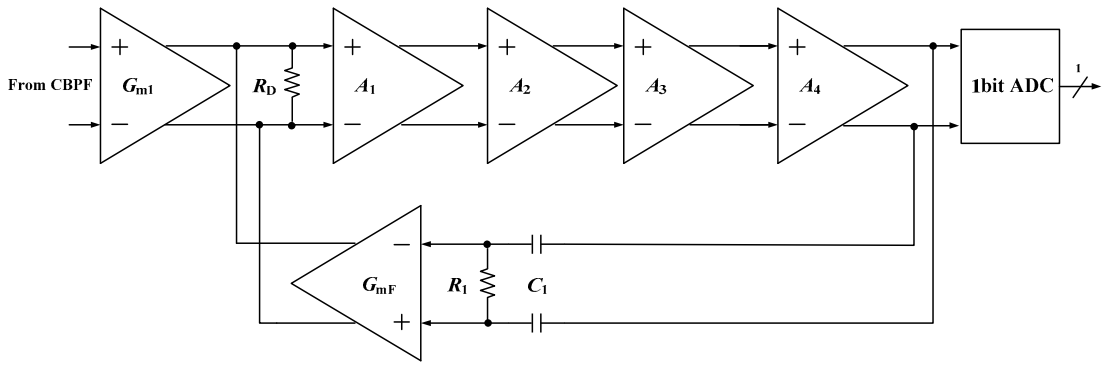


Figure 13. The overall circuit block diagram of the limiting amplifier.

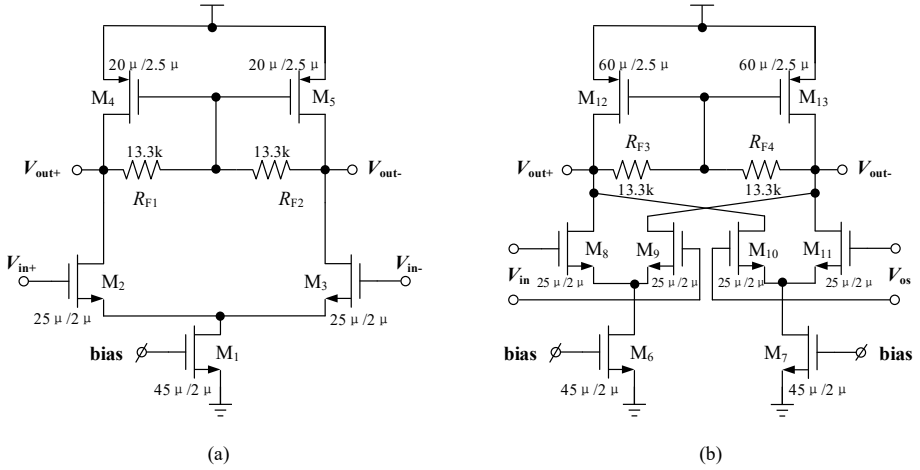


Figure 14. The schematic of (**a**) the voltage amplifier, (**b**) G_{m1}, G_{mF} and R_D.

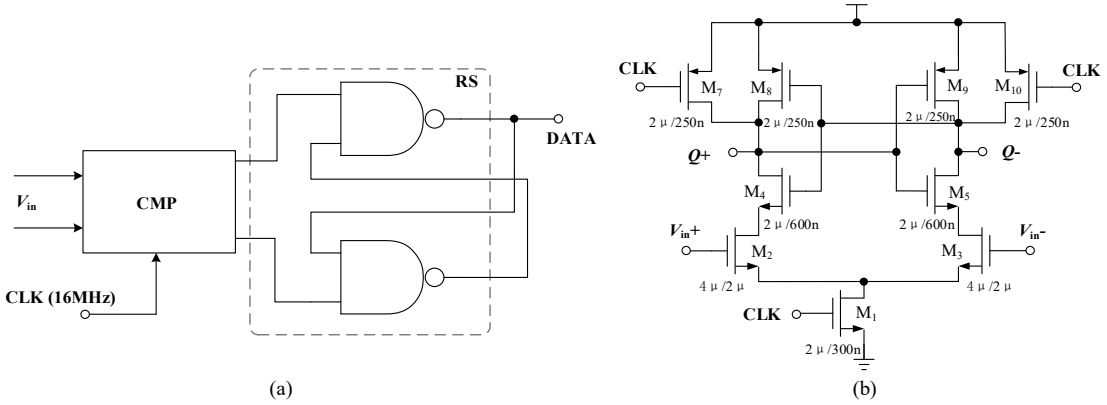
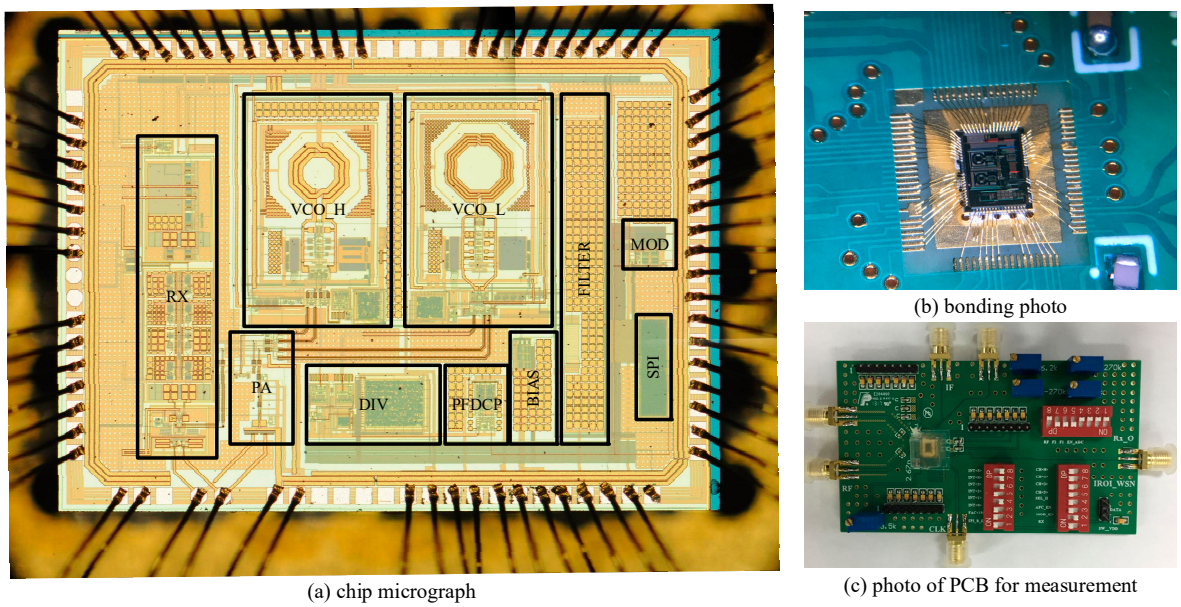


Figure 15. (**a**) The block diagram of the 1-bit ADC, (**b**) the schematic of the internal comparator.

5. Measurement Results

The die photograph of the proposed multi-band ZigBee transceiver fabricated in TSMC 0.18 μm CMOS process is presented in Figure 16. The chip size was 6.04 mm^2, including ESD and pads. The transceiver was measured under 1 V supply voltage.

The schematic diagrams of receiving and transmitting tests are shown in Figure 17. The gain, linearity, and noise test of the receiving link only included the receiver front end and CBPF in the link, as the modulator worked in a nonlinear state. Since the minimum test frequency of the psophometer N8975A in the laboratory was 10 MHz, the noise at IF frequency 2 MHz could not be measured. Thus, the gain test method [27] was adopted in NF measurement through the spectrum analyzer. In linearity (IIP_3) measurement, a dual-tone signal with a frequency interval of 10 MHz was fed to the RF port. The RX gain of the transceiver was controlled by D_0 and D_1. When D_0 and D_1 were both low, the receiver worked in high gain mode. When D_0 was low and D_1 was high, the receiver worked in mid gain mode. When D_0 and D_1 were both high, the receiver worked in low gain mode.



(a) chip micrograph

(b) bonding photo

(c) photo of PCB for measurement

Figure 16. Chip micrograph of the full-band ZigBee transceiver: (**a**) Chip micrograph, **(b)** bonding photo, (**c**) photo of PCB for measurement.

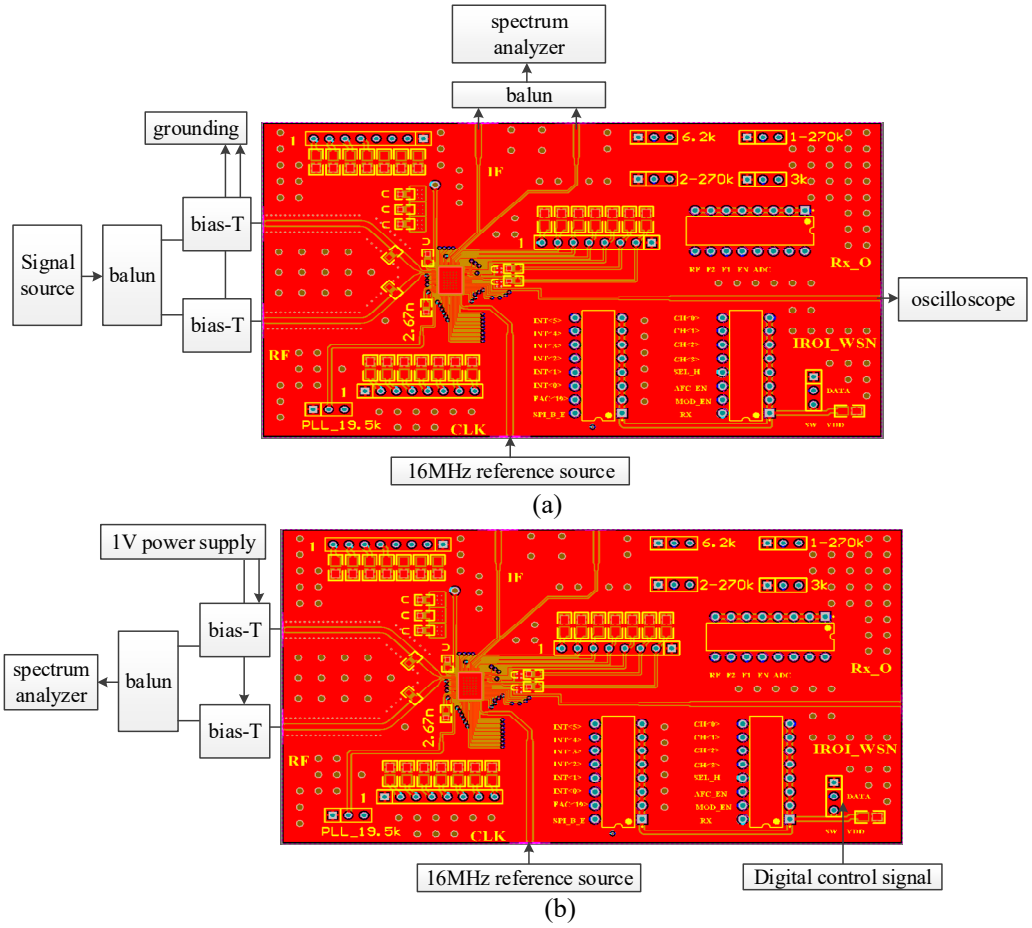


Figure 17. (**a**) Schematic diagram of receiving test, (**b**) schematic diagram of transmitting test.

5.1. RX Transmission

In receiving mode, the current consumption of this work was only 1.42 mA without PLL. The measured RX conversion gain and NF in three gain modes against multi-band are shown in Figure 18. As can be seen from the picture, different characteristics existed between 2.4 GHz and sub-GHz frequency band, but the internal characteristics of sub-GHz frequency band were similar. Thus, the RX and TX measurement results at 780 MHz frequency band are given in the paper as the representative of sub-GHz frequency band characteristics. In high gain mode, the receiver showed 38.4 dB and 45.9 dB in-band gain at 2.4 GHz and 780 MHz band and the corresponding NF was 16.7 dB and 8.4 dB. The measured RX intermediate-frequency response test curve in high gain mode at 2.4 GHz band is presented in Figure 19(a), from which the alternate channel rejection, adjacent channel rejection, and image rejection can be read to be 55 dB, 29.3 dB, and 23.1 dB. The receiver showed a good input-matching ($S_{11} < -10$ dB) from 500 MHz to 2.5 GHz, as shown in Figure 19(b). Figure 20 shows the measured RX out-of-band IIP_3 at 2.4 GHz and 780 MHz band in three gain modes, which were 2.4 dBm and −2.5 dBm, respectively, in low gain mode. Furthermore, it followed that the sensitivity and SFDR of the receiver could be estimated to be −93.8 dBm, 64 dB, and −102 dBm, 66.2 dB at 2.4 GHz and sub-GHz band, respectively. In three gain modes, the measured RX conversion gain, NF and IIP_3 are summarized in Table 4.

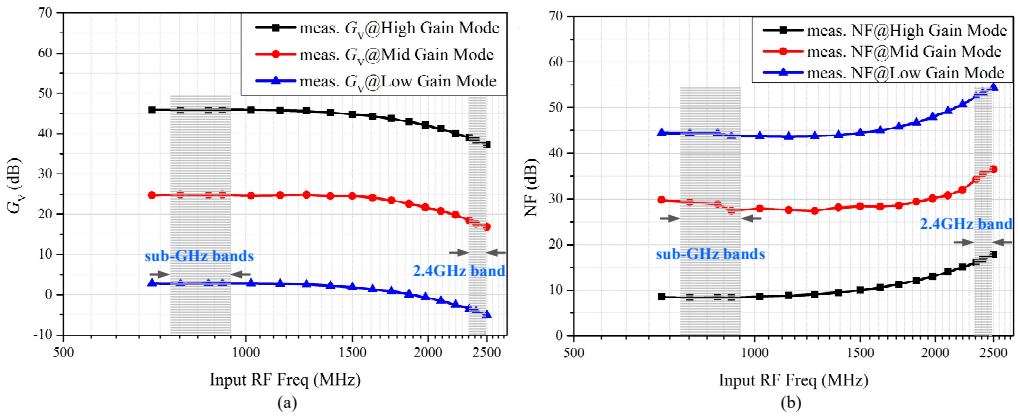


Figure 18. Measured RX (**a**) conversion gain, (**b**) NF in three gain modes against multi-band.

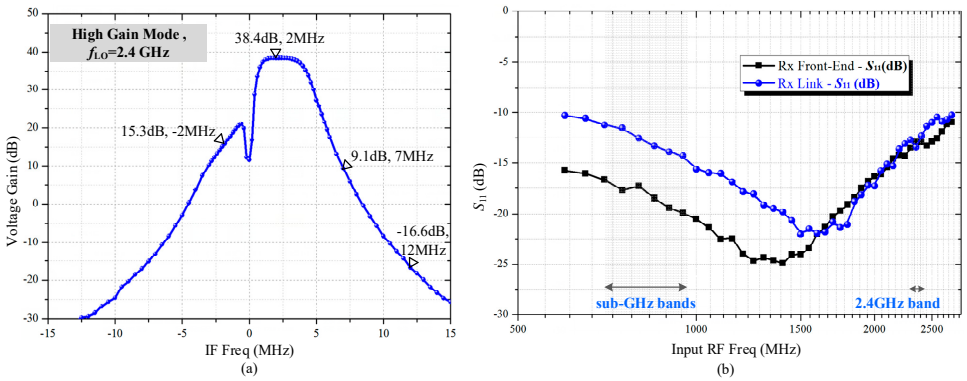


Figure 19. (**a**) Measured RX intermediate-frequency response test curve in high gain mode at 2.4 GHz band, (**b**) measured RX input matching.

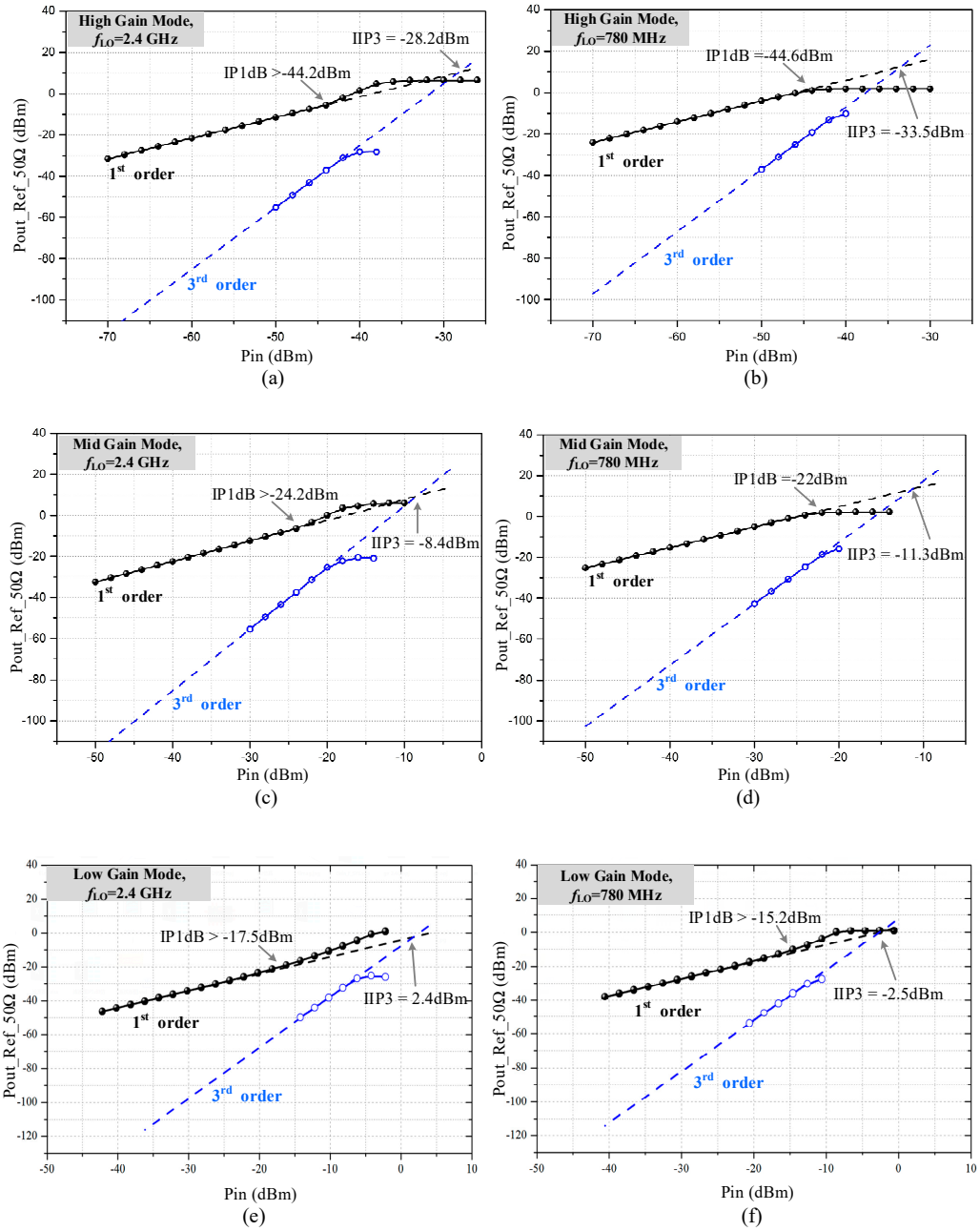


Figure 20. Measured RX out-of-band IIP_3 at 2.4 GHz and 780 MHz band in three gain modes: (**a**) High gain mode, f_{LO} = 2.4 GHz; (**b**) high gain mode, f_{LO} = 780 MHz; (**c**) mid gain mode, f_{LO} = 2.4 GHz; (**d**) mid gain mode, f_{LO} = 780 MHz; (**e**) low gain mode, f_{LO} = 2.4 GHz; (**f**) low gain mode, f_{LO} = 780 MHz.

Table 4. Measured RX conversion gain, NF, and IIP_3.

Frequency band (MHz)	Gain mode	Conversion Gain (dB)	NF (dB)	IIP_3 (dBm)
780	High	45.9	8.4	-33.5
	Mid	24.8	29.3	-11.3
	Low	2.7	44.4	-2.5
868	High	45.9	8.5	---
	Mid	24.7	28.9	---
	Low	2.8	44.5	---
915	High	46.0	8.4	---
	Mid	24.8	27.4	---
	Low	2.8	43.8	---
2400	High	38.4	16.7	-28.2
	Mid	17.6	35.6	-8.4
	Low	-4.1	53.3	2.4

5.2. Frequency Synthesizer

The measured phase noise at PA output is presented in Figure 20(a). The worst phase noise at sub-GHz frequency band was −116.7 dBc/Hz and −129.2 dBc/Hz at 1-MHz and 3-MHz frequency offset, and the phase noise at 2480 MHz was −106.8 dBc/Hz and −122.6 dBc/Hz at 1-MHz and 3-MHz frequency offset, satisfying the phase noise requirement of the system. The measured synthesizer current consumption for sub-GHz and 2.4 GHz band were 3.5 mA and 4.2 mA, respectively.

5.3. TX Transmission

Figure 21(b) shows the TX carrier spectrum at 2.4 GHz and sub-GHz band. Taking 5 dB loss of the cable and balun at RF port into consideration, the output power measured at 780/868/924/2480 MHz band were 12.65 dBm, 12.37 dBm, 12.16 dBm, and 2.67 dBm, respectively. The TX output power and current consumption, including the PA, the frequency synthesizer, and the modulator which is used to change the dividing ratio of the divider and the tuning word of the VCO, for different channel frequency are shown in Table 5. Figure 22 shows the measured TX carrier spectrum at 784 MHz with the reference spur of –53 dB and the TX carrier spectrum at 2.4 GHz with the reference spur of –51 dB.

Table 5. Measured TX output power and current consumption.

Channel frequency (MHz)	Output power (dBm)	Current consumption (mA)			
		PA	Frequency synthesizer	Modulator	Total
780	12.65	65	3.5	1	69.5
868	12.37	65	3.5	1	69.5
924	12.16	65	3.5	1	69.5
2480	2.67	16	4.2	1	21.2

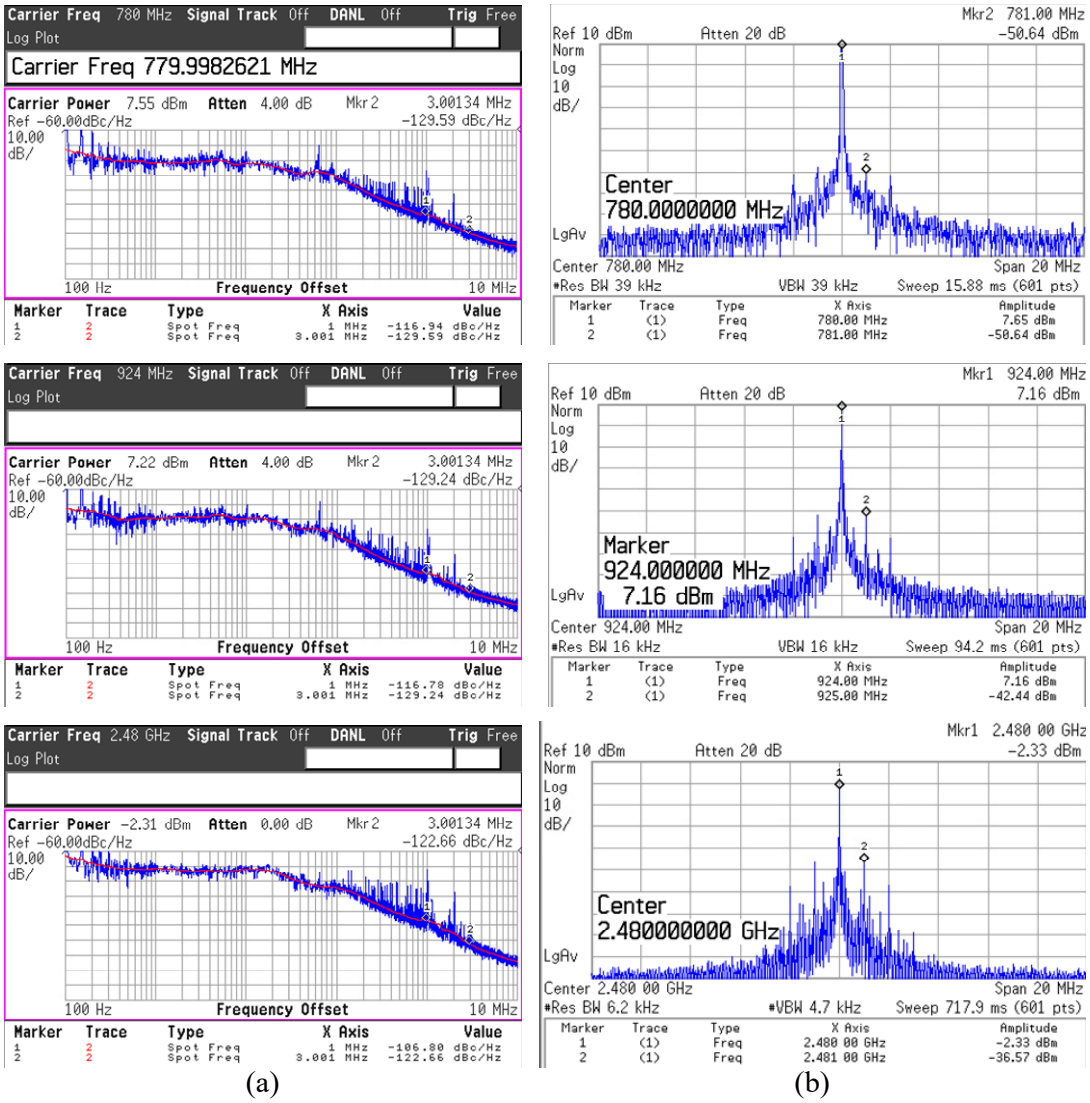


Figure 21. (**a**) Measured phase noise, (**b**) measured TX carrier spectrum at 2.4 GHz and sub-GHz band.

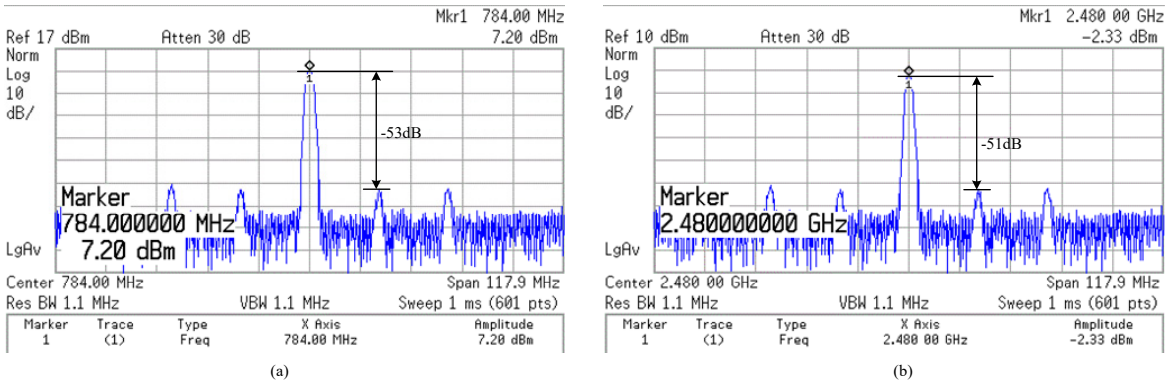


Figure 22. Measured TX carrier spectrum (**a**) at 784 MHz with the reference spur of –53 dB, (**b**) at 2.4 GHz with the reference spur of –51 dB.

5.4. Performance Summary and Comparison

Performance summary and comparison of the proposed transceiver with previously reported transceivers and available systems in the market are listed in Table 6. It can be seen that the proposed transceiver had comparable performance with previously reported or market-available transceivers

working alone at 2.4 GHz or sub-GHz band, but it could cover the whole frequency band and consume less power.

Table 6. Performance summary and comparison.

	This work		[14]	[15]	[16]	[28]	[29]	[30]	Unit
RF frequency range	700–1000	2400–2500	2405–2480	2405–2480	433–960	2405–2480	2400–2483.5	862–928	MHz
TX output power	12.65	2.67	5	9	--	0	3	10	dBm
Phase Noise									
@1MHz offset	-116.7	-106.8	-107	-111.5	--	--	-135[f]	-126	dBc/Hz
@3MHz offset	-129.2	-122.6		--	-117.4[d]		-145[g]	-131	
RX Conversion Gain	45.9[a]	38.4[a]	102.5	--	50	--	--	--	dB
	24.7[b]	17.6[b]							
	2.7[c]	-4.1[c]							
RX Sensitivity	-102	-93.8	-101	-97	--	-94	-95	-100	dBm
	8.5[a]	16.7[a]							
RX NF	29.3[b]	35.6[b]	6.2	7.5	8.1	8	--	--	dB
	44.5[c]	53.3[c]							
	-33.5[a]	-28.2[a]							
RX IIP_3	-11.3[b]	-8.4[b]	-11	--	-20.5	--	-13.6	-12.2	dBm
	-2.5[c]	2.4[c]							
Channel Rejection									
Image	23.1		--	-	--	--	--	36	dB
Adjacent (±5 MHz)	29.3			30.9		30		38	
Alternate (±10 MHz)	55			52		40		--	
Current Consumption									
RX mode	4.92	5.62	14.3	15.4	2.3	19	19	12.8	mA
TX mode	69.5	21.2	16.7	28.4	--	23	21.5	24.1	
Supply voltage	1		1.8	1.2	0.5	3.3	3.6	3	V
Technology	180		180	90	65	--	--	--	nm
Die Size	6.04		7.84	3.24	0.2	496.6[e]	25[h]	25[h]	mm^2

[a]in high gain mode, [b]in mid gain mode, [c]in low gain mode, [d]VCO phase noise @3.5 MHz, [e]surface mountable, [f]10 MHz frequency offset, [g]≥50 MHz frequency offset, [h]32-lead LFCSP package.

6. Conclusions

This paper has demonstrated a low-voltage multi-band ZigBee transceiver employing various techniques for power saving and performance enhancement. Specific design methods and optimization strategies were proposed in the design of receiver front end, filter, and frequency synthesizer. Two VCOs were employed for wideband operation. Different gain modes were utilized to adapt to different input signal amplitudes to expand the RX dynamic range. Measurement results indicated that the proposed transceiver is comparable to or even better than previously reported single/dual band transceivers in the following aspects: Receiver sensitivity, IIP_3, synthesizer phase noise, and power dissipation, while providing a particular frequency coverage of 780/868/915 MHz and 2.4 GHz, which means that the WSN nodes can be equipped with superb compatibility and flexibility.

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Conflicts of Interest: The authors declare no conflict of interest.

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