Article

A Complementary Recycling Operational Transconductance Amplifier with Data-Driven Enhancement of Transconductance [†]

Xiang Li , Bo Hou , Chung Ju, Qi Wei * , Bin Zhou * and Rong Zhang *

Department of Precision Instruments, Tsinghua University, Beijing 100084, China; li-x07@mails.tsinghua.edu.cn (X.L.); houb15@mails.tsinghua.edu.cn (B.H.); jcg17@mails.tsinghua.edu.cn (C.J.)

* Correspondence: weiqi@tsinghua.edu.cn (Q.W.); zhoub@mail.tsinghua.edu.cn (B.Z.); rongzh@mail.tsinghua.edu.cn (R.Z.); Tel.: +86-10-6279-5692 (Q.W. & B.Z. & R.Z.)

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Abstract: An improved operational transconductance amplifier (OTA) is presented in this work. The fully differential OTA adopts the current recycling technique and complementary NMOS and PMOS input branches to enhance the total transconductance. Moreover, in order to achieve higher current efficiency, a data-driven biasing circuit was developed to dynamically adjust the power consumption of the amplifier. Two comparators were added to detect the voltage difference at the input nodes, and when the differential input is large enough to activate either comparator, extra biasing current is activated and poured into the amplifier to enhance its slew rate and gain-bandwidth product (GBW). The threshold voltage of the complementary recycling folded cascode (CRFC)-based comparator is configured to suppress overshoot. Complementary common-mode feedback (CMFB) topology with local CMFB structure is built to acquire high common-mode gain. The OTA was fabricated in SMIC 0.18- μm CMOS technology. The experimental result based on a capacitive feedback loop shows that the data-driven operation improves the average slew rate of the amplifier from 10.2 V/ μs to 55.5 V/ μs while the power only increases by 150%. The OTA has good potential to satisfy the fast settling demands for capacitive sensing circuits.

Keywords: complementary recycling folded cascode (CRFC); switched capacitor circuit; OTA; data-driven

1. Introduction

Operational transconductance amplifiers (OTAs) are widely used in capacitive sensor interface and switched capacitor circuits [1–5]. Enhancement of gain-bandwidth product (GBW), slew rate (SR) and current efficiency (CE) of OTA is required in application areas for large capacitive load, expeditious and accurate signal transition, and small power consumption. The folded cascode (FC) has been a fundamental amplifier structure to acquire high DC gain and relatively large signal swing [6,7], which is shown in Figure 1. However, it usually costs much biasing current since the cascode transistors are in separate current paths from the input transistors. Based on the current recycling technique by Assaad and Silva-Martinez [8,9], several approaches have been reported to enhance the transconductance and speed of OTA [10–13]. Although these techniques are beneficial for achieving higher and higher CE, the static biasing current remains a fixed power consumption contributor in a conventional class-A amplifiers. Considering the behaviour of a switched capacitor circuit for example, it generally consists of sampling stage and holding stage when triggered by a clock edge. To guarantee fast settling

in sampling stage, the amplifier requires much biasing current to achieve high SR [14], but in the holding stage, it becomes unnecessary to maintain high SR and power consumption.

In this article, we demonstrate a data-driven complementary recycling folded cascode (CRFC) OTA for applications such as sensing and driving interfaces. The CRFC amplifier topology was developed to augment the GBW and make more efficient use of the current than the conventional recycling folded cascode (RFC) amplifier. Moreover, we established a data-driven scheme with a comparator-controlled extra current source branch added to the biasing circuit of the OTA. The data-driven current branch is activated and the extra current is poured into the biasing circuit to enhance the SR and GBW of the OTA and improve its speed when the input differential signal exceeds the comparator's threshold voltage.

The article is organised as follows. In Section 2, the conventional FC and RFC architectures are analysed. In Section 3 the structure of the proposed CRFC amplifier is then described, and to improve its dynamic current efficiency, the data-driven scheme is introduced. The OTA was fabricated in SMIC 0.18 μm technology. The simulated and experimental results are discussed in Section 4. Section 5 provides the conclusions.

Figure 1. Conventional folded cascode operational transconductance amplifiers (OTA).

2. Folded Cascode OTA and Recycling Technique

The conventional folded cascode (FC) OTA is shown in Figure 1. Two identical transistors $MP1$ and $MP2$ form differential input pair, and the cascode transistors $MN3$ and $MN4$ are in separate current paths, which are "folded" to the drain nodes of $MN1$ and $MN2$. The total current consumption is $4I_b$, and the equivalent transconductance of the amplifier is

$$G_{m,FC} = g_{mP1}. \quad (1)$$

Under large signal input assumption, the SR of the FC amplifier can be expressed as

$$SR_{FC} = \frac{2I_b}{C_L}. \quad (2)$$

The FC is regarded as one of the most significant amplifier architectures for its high gain and relatively large signal swing [15]. However, as the cascode transistors consume biasing current independently, they suffer the disadvantage of power inefficiency. To enhance the transconductance of the FC, Assaad and Silva-Martinez [8,9] introduced the recycling technique and realised the recycling folded cascode (RFC) amplifier shown in Figure 2. The input transistors are split in half, and the transistors $MN1$ and $MN2$ in Figure 1 are modified to current mirrors which have a ratio of 3:1.

The total current of the RFC is $4I_b$, equal to the FC. The small signal currents are amplified by the current mirrors to get enhanced transconductance, which can be derived as

$$G_{m,RFC} = (1 + 3)g_{mP1a} = 4g_{mP1a}, \quad (3)$$

where $2g_{mP1a} = g_{mP1}$. And the SR of RFC is

$$SR_{RFC} = \frac{6I_b}{C_L}. \quad (4)$$

Figure 2. The recycling folded cascode (RFC) OTA.

Compared with Equations (1) and (2), it can be seen that the RFC has an enhanced transconductance by a factor of 2 and a slewrate larger by a factor of 3 than the FC under equal biasing current conditions.

3. Proposed Data-Driven CRFC OTA

3.1. CRFC Amplifier Circuit

We introduced a CRFC [16] architecture as the main part of the amplifier, shown in Figure 3. This structure was developed from the idea of recycling current of a folded cascode [8,9]. As opposed to the PMOS-input-only RFC amplifier in Figure 2, an NMOS-input branch formed by transistors $MN1a$, $MN1b$, $MN2a$ and $MN2b$ is added parallel to the PMOS-input one. The cascode transistors of each branch ($MN9$ and $MN10$ for the PMOS input, $MP9$ and $MP10$ for the NMOS input) share the same current path, and the total current flowing through the folded cascode transistors is $2I_b$. The biasing current of either input drivers, i.e., the drain current of $MP0$ or $MN0$, is also equal to $2I_b$, so the total static current of the CRFC amplifier is $6I_b$. The transconductance of the amplifier can be written as

$$G_{m,CRFC} = 4g_{mP1a} + 4g_{mN1a}, \quad (5)$$

and the slew rate of the full-differential output can also be derived as

$$SR_{CRFC} = \frac{12I_b}{C_L}. \quad (6)$$

Figure 3. The complementary recycling folded cascode (CRFC) OTA [16].

Since for a transistor in strong inversion region, whether P-type or N-type, g_m/I_D is only relevant to $V_{GS} - V_T$, we can reasonably assume the PMOS and NMOS input transistors have the equal transconductance. It can be found that the transconductance and the slew rate of the CRFC amplifier is twice that of the conventional RFC while the current consumption increases by a half. If we define two $FoMs$ (figures of merit) to characterise the amplifiers' performance as

$$FoM_1 = \frac{GBW \times C_L}{I}, \quad (7)$$

$$FoM_2 = \frac{SR \times C_L}{I}, \quad (8)$$

we can find $FoM_{1,CRFC} = 4FoM_{1,RFC}/3$ and $FoM_{2,CRFC} = 4FoM_{2,RFC}/3$, which indicates the current efficiency of the CRFC is improved by a factor of 1/3 compared with the RFC, with the same capacitive load. The symmetry of the circuit with complementary input differential pairs also provides larger input swing.

3.2. Data-Driven Biasing Scheme

The biasing circuit with data-driven scheme for the CRFC amplifier [16] is shown in Figure 4. The current mirrors formed by transistors $M1 \sim M24$ and the current source I_1 compose conventional biasing circuit. Under this biasing circumstance, the amplifier will operate at a fixed static current level. The transconductance and SR of the OTA are limited by Equations (5) and (6), which means that higher speed can only be achieved by increasing the aspect ratio of the transistors, and thus consuming more power. In order to explore a method to mitigate the conflict between performance and power dissipation, a data-driven control method is implemented to the biasing circuit.

A parallel current source I_2 with two NMOS switches $MS1$ and $MS2$ was added to the biasing circuit. The gate of each switch is connected to the output terminal of one comparator. The absolute difference of input signal of the OTA is also monitored by the comparators. If the differential input signal is large enough to drive either comparator to flip, for example, letting V_{INP} larger than V_{INN} , the output voltage of $COMP1$ will be pulled to V_{DD} and switch $MS1$ will be turned on. Then, current source I_2 will be activated in the biasing circuit and the total current of the amplifier is augmented, enhancing the transconductance and slew rate. When the input signal gets smaller than the comparators' threshold, both comparators are pulled down to zero voltage and shut off the switches. Only current source I_1 provides biasing, and the amplifier consumes relatively little power. However, stability and accuracy of the circuit are retained due to better phase margin at this static state. We take the switched capacitor circuit as an application example. At the sampling stage, the data-driven option is activated and the transition speed be improved, while at holding stage, the amplifier works at low-power state preserving high DC gain and accuracy. Through the dynamic biasing accommodation

method, a higher average current efficiency will be achieved. The data-driven biased amplifier was inspired by a common digital circuit [17]. The voltage difference between two differential input nodes is sampled to generate one-bit signal to control the analogue biasing condition. Still, it should be underlined that the proposed amplifier has two different biasing current levels. When designing the transistors' parameters, the operating points of static mode and data-driven mode should be considered simultaneously to retain good performance at both working states.

Figure 4. Biasing circuit with the data-driven scheme [16].

Figure 5 shows the comparator circuit used in the data-driven part. Latch-based structure is widely used in data converters [18]. However, extremely high comparator gain is not preferred in this design, since a very small input signal will trigger the data-driven operation, leading to large power consumption and signal distortion. The comparator based on the CRFC technique was chosen, modifying the full-differential topology to single-end output. The threshold of comparator should also be carefully designed to select an optimised shifting point between small-current and large-current states. We configured the threshold several millivolts over zero to reduce overshoot when switching from data-driven mode to static mode. We reduced the aspect ratio of transistor MC0 to pull up the drain voltage of MC18 and MC20 with zero differential input signal. When $V_{CN} - V_{CP} > V_{thres}$, the drain voltage of MC18 comes below the turning point of the inverter, causing the comparator output V_{COUT} set to 1. Through this configuration, the operating window of the data-driven scheme can be controlled to satisfy specific requirements.

Figure 5. Comparator circuit based on CRFC structure.

3.3. Common-Mode Feedback (CMFB) Realisation

The full-differential OTA requires a common-mode feedback circuit (CMFB) to settle the common-mode voltage of both output points. In order to avoid signal glitch and aliasing, we established a continuous-time CMFB architecture based on the idea in [19] for the CRFC amplifier, which is shown in Figure 6: a complementary CMFB circuit which has two separate branches to provide biasing for both NMOS and PMOS current sources in the CRFC amplifier (see Figure 3). Each branch in the proposed CMFB circuit applies a local CMFB structure which consists of two MOS transistors and two matched resistors in series, which, taking the V_{cmfbp} -output branch as an example, enlarges the transconductance by a factor of $g_{mP0}R$, where g_{mP0} is the transconductance of $MP0$ in the CRFC amplifier's main circuit. By using this CMFB module, a larger GBW can be achieved and the dynamic performance is improved.

Figure 6. Complementary common-mode feedback circuit (CMFB) circuit.

4. Simulation and Experimental Results

The amplifier was designed and fabricated in an SMIC 0.18- μm mixed-signal CMOS process, and the chip's micro-photograph is shown in Figure 7. The core part of the amplifier occupied $0.42 \times 0.32 \text{ mm}^2$. The DC supply voltage for the circuit was 5 V. Selection logic was added to choose whether the data-driven function turns on.

Figure 7. The chip's micro-photograph, showing the core part and surrounding I/O pads.

First, open loop AC response of the designed OTA at static mode and data-driven mode was simulated respectively, shown in Figure 8. At static mode, when the amplifier works at low current standard, the DC gain is 61.0 dB and the GBW is 17.5 MHz with a phase margin of 58.5° . In data-driven mode, the DC gain slightly decreases to 59.2 dB, but the GBW increases to 49.2 MHz with a phase margin of 57.0° . This can be explained by the theoretical model of a single transistor, for which, as current increases, transconductance gets higher while small-signal resistance gets smaller, leading to the degradation of DC gain.

Figure 8. AC response of proposed amplifier in static and data-driven modes.

A unity gain capacitive feedback circuit was set up as a test bench for characterising the amplifier's performance, as Figure 9 shows. The input and feedback capacitors were 5 pF, and there was 12 pF of capacitive load at each output terminal. Besides, Tektronix MDO3034 oscilloscope was used to detect the output signal, with 3.9 pF of the probe. The overall load was 18.4 pF approximately. A pair of differential square signals with a peak-to-peak voltage of 1 V and frequency of 800 kHz was applied to the input terminals, and transient waveform of the differential output was sampled by the oscilloscope, as Figure 10 shows. For the CRFC amplifier biased in static mode, the rising times were 403 and 379 ns with a total average current of 530 μ A, and the average calculated SR was 10.2 V/ μ s. Meanwhile, for the circuit with the data-driven scheme activated, decreased rising times of 79 and 65 ns were recorded and the average SR was 55.5 V/ μ s with an average current consumption of 1320 μ A. Note that the measured current included the main amplifier circuit, biasing current mirrors, common-mode feedback circuit and comparators (only in data-driven mode). It was found that in this test, the data-driven operational cost was about 150% extra current. The increased part of power dissipation came from the voltage-controlled current source and the comparators. However, an enhancement about 440% in speed was achieved, indicating that adopting the data-driven scheme improved the total current efficiency, even counting the added current consumption.

Figure 9. Test bench setup for characterising the amplifier's performance.

(a)

(b)

Figure 10. Transient response waveforms of the proposed OTA. (a) The CRFC amplifier in static mode with an average slew rate (SR) of 10.2 V/ μ s; and (b) the data-driven scheme enabled amplifier with an average SR of 55.5 V/ μ s.

The results of the proposed amplifier are summarised in Table 1 (compared with previous reported OTAs). Assaad et al. first reported the recycling current technology [8,9], based on which Yan et al. [10], Akbari [11] and Zhao et al. [13] did significant works to improve the performance of single-stage OTAs. Designed for applications such as capacitive sensor interfaces, DC supply voltage of 5 V was selected to guarantee driving capability and preserve accuracy [20]. Since the transistors operating at this supply level were relatively slower than low-voltage counterparts in general, the amplifier presented in this work had smaller $FoMs$. However, previous simulation results using low voltage transistors [16] indicated the architecture proposed could achieve very high $FoMs$. The comparison of the proposed amplifier between static mode and data-driven mode should be emphasised more; it indicated that the idea of dynamically adjusting the biasing current introduced in this work improved the current efficiency over conventional class-A amplifiers significantly, making a novel attempt at digital control in the field of OTAs. It should also be noted that the efficiency improvement was achieved at the cost of more area occupation, mainly taken by the comparators. And to avoid performance degradation when switching between static mode and data-driven mode, the transistors in the main amplifier circuit should be more carefully designed, which increases design difficulties.

Table 1. Performance comparison.

Parameter	[9]	[10]	[11]	[13]	This Work	
					Static	Data-Driven
DC supply (V)	1.8	1	1.2	1	5	5
Current (μ A)	400	800	483	40	530	1320
Capacitive load (pF)	5.6	10	5	30	18.4	18.4
GBW (MHz)	70.4	203.2	650	10.2	17.5	83
Phase margin ($^{\circ}$)	79.8	66.2	50	80.4	58.5	66.2
DC gain (dB)	59.7	54.5	59.1	80.3	70.2	61.0
Average SR (V/ μ s)	48.1	91.6	115.2	1.78	10.2	55.5
FoM ₁ (MHz·pF/mA)	985.6	2540	6279	7650	607.5	1157
FoM ₂ ((V/ μ s)pF/mA)	673.4	1145	1193	1335	354.1	773.6

5. Conclusions

In this paper, an improved operational transconductance amplifier with a data-driven transconductance enhancement method was presented. The complementary recycling architecture was adopted to achieve a better transconductance and power efficiency. The data-driven method adopted the digital control idea to accommodate the biasing current of amplifier dynamically, and to achieve both augmented slew rate and speed significantly when the amplifier deals with large input. Experimental results confirmed the performance improvement through the data-driven operation. It was an attempt to combine digital thought with a basic analogue circuit block, opening a path to acquiring high performance and low power usage simultaneously. This kind of amplifier has great potential for applications such as capacitive sensing and switched capacitor circuits.

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