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Effects of Back-Gate Bias on Subthreshold Swing of Tunnel Field-Effect Transistor

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Abstract: In this study, the effects of back-gate bias on the subthreshold swing (S) of a tunnel field-effect transistor (TFET) were discussed. The electrostatic characteristics of the back-gated TFET were obtained using technology computer-aided design (TCAD) simulation and were explained using the concepts of turn-on and inversion voltages. As a result, S decreased, when the back-gate voltage increased; this behavior is attributed to the resultant increase in inversion voltage. In addition, it was found that the on–off current ratio of the TFET increased with a decrease in S due to the back-gate voltage.

Keywords: tunnel field-effect transistor (TFET); band-to-band tunneling; back-gate bias effect

1. Introduction

A continuous scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) has enabled integrated circuit (IC) chips to be fabricated with more functionality and at a lower cost [1,2]. Currently, multi-gated (MG) FETs (e.g., FinFETs) have replaced conventional FETs, which face a physical limit on scaling owing to short-channel effects [3]. Moreover, FinFETs also have a theoretical limit on subthreshold swing (S), since they are based on Boltzmann statistics as well. Therefore, a decrease in power consumption through the maintenance of a high on–off current ratio (I_{on}/I_{off}) is a huge technical challenge for future complementary MOS (CMOS) technology.

A tunnel FET (TFET) has been regarded as one of the most promising candidates for the next-generation low-power devices, because it can achieve a subthreshold swing of 60 mV/decade at room temperature [4,5]. Most studies about TFETs have mainly focused on improving their performance in terms of I_{on}, S, etc. by changing their structures and materials of devices [6–9]. Moreover, most TFETs use silicon-on-insulator (SOI) structures; therefore, it is very important to understand how a back-gate bias (V_{bg}) affects the operation of TFETs. A few studies have reported that back-gate biases change the transfer characteristics of TFETs [8,10]. However, no in-depth analysis has yet been conducted on how a back-gate bias affects S specifically. Therefore, in this study, the subthreshold characteristics of a back-gated TFET are extensively analyzed by means of technology computer-aided design (TCAD) simulation. Through this simulation, it is shown, for different back-gate biases, the channel potential changes with gate bias, along with the mechanism behind this change. The results thus obtained were used to analyze the influence of back-gate bias on the transfer characteristics of the TFET, especially the subthreshold swing.

2. Simulation Conditions

The device structure studied in this work is shown in Figure 1. In order to improve current drivability with the help of pseudo-direct band-to-band tunneling (BTBT) model, a p-type source and a channel are made of Ge [9]. On the other hand, a Si drain is used for suppressing a leakage current due to the ambipolar behavior (I_{amb}) and the Shockley–Read–Hall (SRH) recombination observed in TFETs. As well as the top-gate oxide of a 1 nm thick SiO_2 layer, the back-gate electrode is also separated from the Ge channel, using the same thickness of SiO_2 to prevent the substrate leakage current, through the forward-biased source to the substrate junction; in this case, the substrate is negatively biased. The work functions for both the top and back gates are 4.05 eV. The other device design parameters are summarized in Table 1. In order to rigorously examine the BTBT behavior, a dynamic nonlocal BTBT model was used for TCAD simulation after calibration [11,12]. In addition, both indirect and direct BTBTs were considered in this simulation [7,9,11].

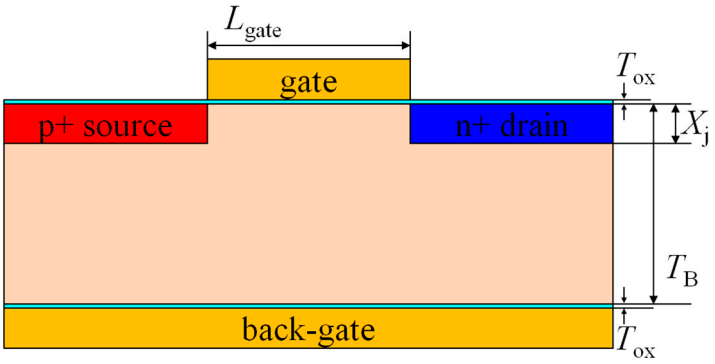

Figure 1. Schematic diagram of a back-gated tunnel field-effect transistor (TFET).

Table 1. Device parameters used in technology computer-aided design (TCAD) simulation.

Parameter	Description	Unit	Value
L_{gate}	gate length	nm	50
T_{ox}	equivalent oxide thicknesses of top- and back-gate oxides	nm	1
X_j	junction depth	nm	10
T_B	body thickness	nm	50
N_S	source doping concentration	/cm^3	10^{20}
N_D	drain doping concentration	/cm^3	10^{20}
N_B	body doping concentration	/cm^3	10^{17}

3. Results and Discussions

Figure 2 shows drain current (I_d) as a function of top-gate voltage (V_{tg}) for different values of V_{bg}. Different drain voltages (V_{ds}) of 0.05 V and 0.5 V were applied as shown in Figure 2a,b, respectively. Two noteworthy phenomena were discussed below.

First, a comparison of Figure 2a,b clarified that a higher V_{ds} contributed to a lower minimum S. Furthermore, it was also observed that, as V_{ds} increased, the channel inversion voltage (V_{inv}) increased. V_{inv} is defined as the value of V_{tg} required for the formation of an inversion layer [9]. It was observed that, similar to those of MOSFETs, the surface potential of the TFET rarely changed after an occurrence of channel inversion ($V_{tg} \geq V_{inv}$). However, it was observed that the V_{inv} of the TFET was unaffected by the gate-to-source voltage (V_{gs}), but it was determined by the gate-to-drain voltage (V_{gd}) instead. Moreover, an increase in V_{ds} also increased V_{inv}, while the change in turn-on voltage (V_{on}) was negligible during the first occurrence of the BTBT. Due to this, the gate-to-channel coupling for high

V_{ds} was stronger than that for low V_{ds}, which further resulted in a smaller S compared with that for low V_{ds}.

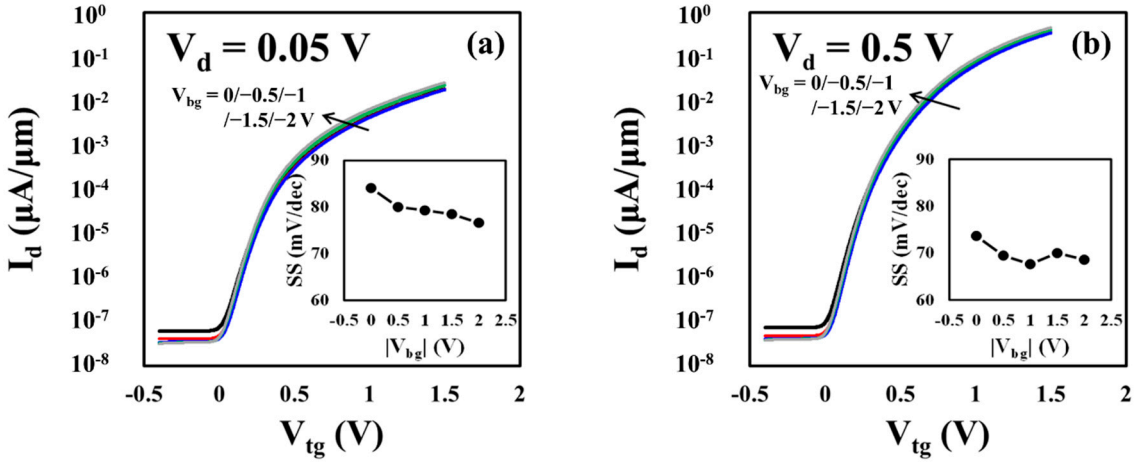

Figure 2. Transfer characteristics, where V_{bg} is changed from 0 to −2.0 V with a −0.5 V step at different V_{ds} values: (**a**) 0.05 V and (**b**) 0.5 V. The insets are the extracted minimum S as a function of V_{bg}.

Second, the insets of both Figure 2a,b indicate that S was improved as the amount of V_{bg} increased. As shown, if the amount of V_{bg} was increased up to 2 V, S was decreased from 84 to 77 mV/dec for V_{ds} = 0.05 V and from 74 to 68 mV/dec for V_{ds} = 0.5 V. In addition, Figure 3a,b depict the change in ratio (I_{on}/I_{off}) of the on-state current (I_{on}) and the off-state current (I_{off}) with increasing amount of V_{bg}. The I_{on} and I_{off} are defined as I_d at V_{tg} = 1.0 V and V_{tg} = 0 V, respectively. As mentioned earlier, due to the improved S by increasing the amount of V_{bg}, the I_{on}/I_{off} increased by 144% and 126% for V_{ds} of 0.05 and 0.5 V, respectively.

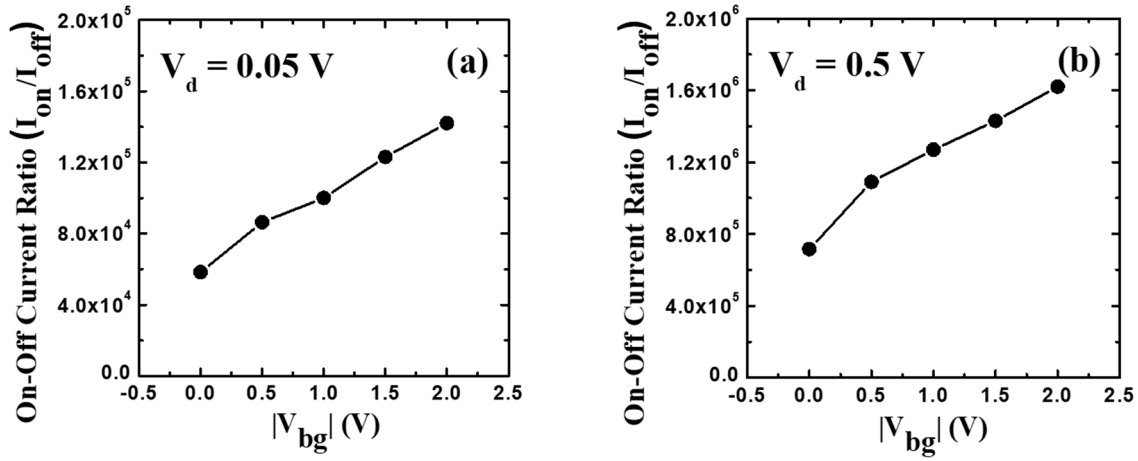

Figure 3. The change in the ratio of the on-state current (I_{on}) and the off-state current (I_{off}), where V_{bg} is changed from 0 to −2.0 V with a −0.5 V step, at different V_{ds} values: (**a**) 0.05 V and (**b**) 0.5 V.

In order to analyze these phenomena, the change in surface potential ($\Delta\varphi_s$) of the back-gated TFET as a function of V_{tg} was examined, as shown in Figure 4. $\Delta\varphi_s$ was extracted as the change in surface potential with respect to V_{tg} sweep starting from −0.4 V. As shown, for small values of V_{tg}, the surface potential was linearly proportional to it. However, as V_{tg} further increased, the surface potential became saturated. This behavior is attributed to the formation of an inversion layer, which decouples the V_{tg} with the surface potential [13]. Owing to the screening of the V_{tg} by the inversion charges at the channel, the surface potential could not be increased any further. As a result, the BTBT barrier width (i.e., BTBT probability) was almost fixed, and I_d became slightly saturated, which resulted in a distinct

degradation of S with the increase in V_{tg}, as shown in Figure 2. An interesting phenomenon observed in Figure 4 is that the saturation point of the surface potential was pulled back when V_{bg} was applied. The channel potential was well-controlled by V_{tg} before the saturation region, which explained the improvement in S with a larger $|V_{bg}|$.

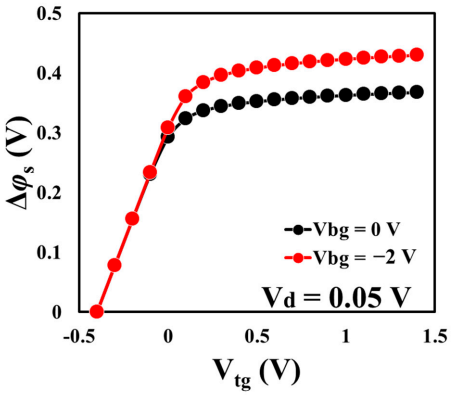

Figure 4. The change in surface potential as a function of V_{tg}, when V_{bg} is biased by 0 and −2 V. At a higher V_{tg}, an increase in amount of V_{bg} causes the formation of an inversion layer, which results in the occurrence of the saturation of the surface potential.

In order to confirm the dependence of S on V_{bg} more quantitatively, the values of V_{inv} were extracted from the gate capacitance (C_g) and V_{tg} relationship for different values of V_{bg}, as shown in Figure 5a, and were further compared with V_{on}, as shown in Figure 5b. By referring to [14], the values of V_{inv} were extracted from the first extremums of the second derivative of the C_g–V_{tg} curves. The extraction method is a concept of extracting the V_{th} of an MOESFET similar to the maximum transconductance ($g_{m,max}$) method; and the extraction equation was written as below:

$$\frac{dg_m}{dV_{tg}} = \frac{d^2I_d}{dV_{tg}{}^2} \propto \frac{d^2C_g}{dV_{tg}{}^2}. \quad (1)$$

As a result, the larger extremum points were obtained, when higher values of $|V_{bg}|$ were applied, which meant the higher V_{tg} was required for the channel inversion. Because the better gate controllability was secured before the formation of the inversion layer, the higher value of V_{inv} means that the region of steeper transfer characteristics was expanded. The top-gate controllability improvement by the back-gate bias can be explained with the energy band diagrams of a single-gate device and a double-gate device, as shown in Figure 5c.

Considering the definitions of V_{inv} and V_{on}, the mechanism of the change in S with respect to the amount of V_{bg} can be understood by comparing the values of V_{inv} and V_{on}. As clearly observed from Figures 2a and 5b, V_{on} did not vary for different values of V_{bg}, and the transistor was turned on for the same value of V_{tg} (−0.04 V). Since the energy level of the Γ valley of Ge for direct tunneling is 0.14 eV higher than that of the L valley, where indirect tunneling occurred, it is necessary to change the surface potential, even after the turn-on point of the transistor V_{on}, in order to improve S using direct tunneling. In the absence of V_{bg}, V_{inv} was found to be lower than V_{on}, as shown in Figure 5b. This meant that, in this case, it was hard for direct tunneling to take place, because of the already formed inversion layer, which screened the electric field. In contrast, when a negative V_{bg} was applied, V_{inv} became larger, while V_{on} remained the same, as shown in Figure 5b. Therefore, the direct tunneling between the source and the channel became dominant after the turn-on point of the transistor. Moreover, S was kept at a low level, until the coupling between the V_{tg} and the surface potential became weaker due to the formation of the inversion layer. As a result, the voltage window between V_{on} and V_{inv} was found to be the determining factor for the subthreshold characteristics of TFETs. Furthermore, this is the reason why a lower S can be obtained in back-gated TFETs compared to that in conventional TFETs.

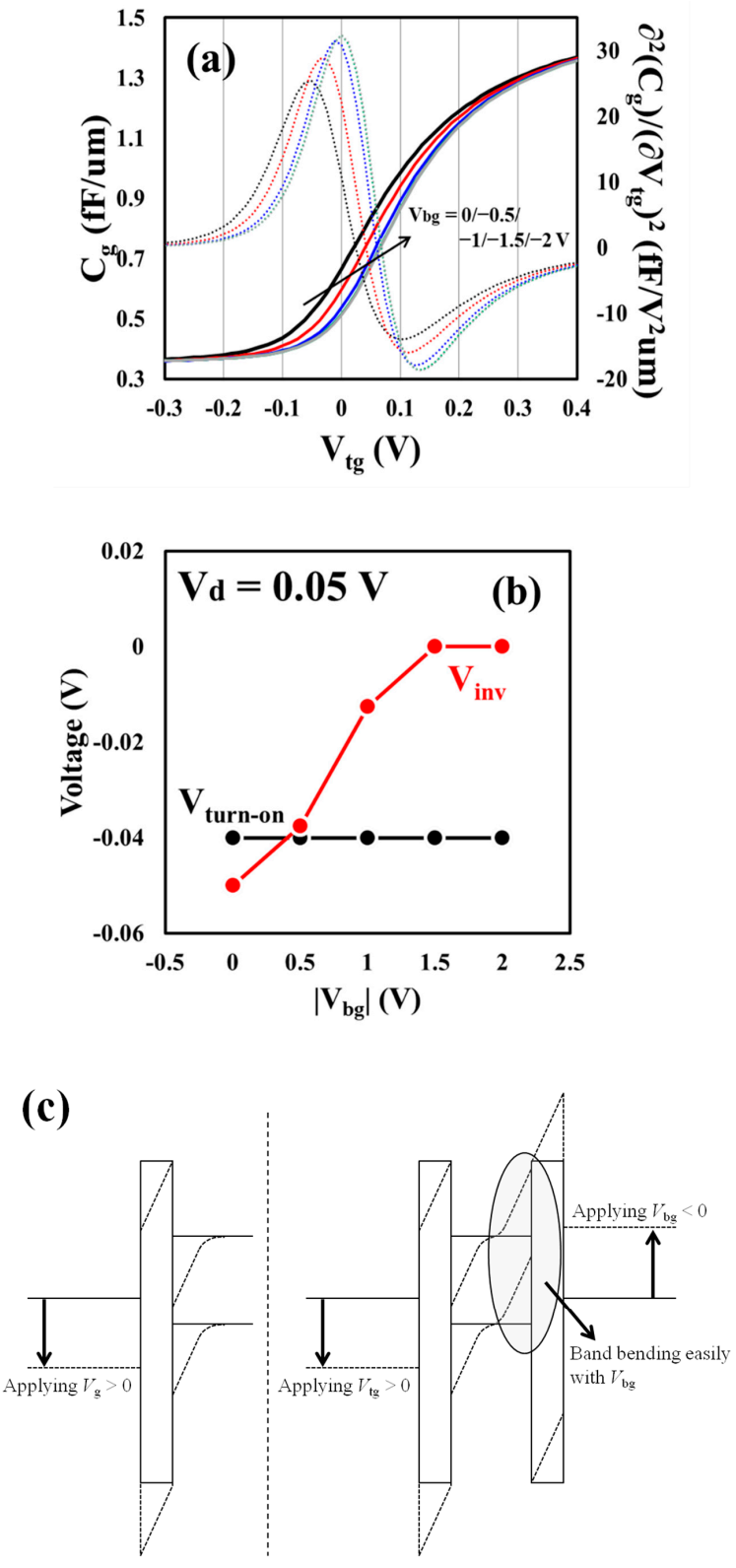

Figure 5. (**a**) Extraction of V_{inv} from the C_g–V_{tg} relationship and its second derivative charts, when the V_{bg} is increased. V_{bg} slows down the inversion point. (**b**) V_{on} and V_{inv} as a function of V_{bg}. V_{inv} increases, as the amount of V_{bg} increases, while V_{on} is kept constant. (**c**) Energy band diagrams of a single-gate device and a double-gate device. The left diagram represents the energy band diagram of the single-gate device, and the right one represents that of the double-gate device. The negative back-gate bias of the double-gate device helps invoke band bending easily.

4. Conclusions

In this study, using the TCAD simulation, it was confirmed that the subthreshold characteristics of a TFET can be improved by introducing a back-gate bias, compared to those of conventional TFETs. The impact of V_{bg} on S was discussed using the concepts of V_{on} and V_{inv}. A V_{bg} value of −2 V can help reduce S of the TFET with L_{gate} = 50 nm. For V_{ds} = 0.05 V, an improvement in S by −7 mV/dec was achieved. In addition, the minimum S value of 68 mV/dec was obtained at V_{ds} = 0.5 V for V_{bg} = −2 V. Moreover, an improvement in transfer characteristics, which was caused by the back-gate voltage, was confirmed by an increase of 126% in on–off current ratio at V_{ds} = 0.5 V for V_{bg} = −2 V. Considering the applications of TFETs as a low-power device, the back-gated TFET structure can be one of the strategies for achieving better performance.

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Conflicts of Interest: The authors declare no conflicts of interest.

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