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Improved Synchronized Space Vector PWM Strategy for Three-Level Inverter at Low Modulation Index

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Abstract: Aimed at reducing the switching loss and common-mode voltage amplitude of high-power medium-voltage three-level inverter under low modulation index conditions, an improved synchronous space vector PWM strategy is proposed in this paper. The switching times in each fundamental period are reduced by the re-division of small regions and the full use of the redundant switching state. The sum of switching algebra is introduced as an evaluation index and the switching state with the minimum value of the sum of switching algebra are adopted. Then, the common mode voltage amplitude is reduced. The theoretical analysis and experimental results show that the improved modulation strategy proposed in this paper can effectively reduce the switching loss and common-mode voltage amplitude of the inverter under the condition of the low modulation index. Moreover, the neutral-point voltage ripple is also reduced simultaneously.

Keywords: switching loss; common mode voltage; synchronization modulation; space vector modulation

1. Introduction

Compared with the traditional two-level converter, the multi-level converter has numerous advantages, such as reduced total harmonic distortion (THD), low dv/dt, and high inversion efficiency. It is widely used in wind power generation, ship propulsion, locomotive traction, and other applications [1–3]. When applied to the above medium-voltage high power motor system, the switching loss becomes the major component of system losses. Taking the traction drive motor system as an example, due to the poor working environment, the cooling condition is poor. Therefore, due to the limitation of heat dissipation, the switching frequency of the inverter is relatively low, usually no more than 1 kHz [4]. In addition, due to the limitation of characteristics of the inverter, common mode voltage will inevitably be generated in the system. When applied to the medium-voltage high power motor system, high common mode voltage will produce large common mode current on the motor shaft, and it may even lead to the breakdown of the insulation layer and affect the service life of the motor [5]. To sum up, how to reduce the switching loss and amplitude of common mode voltage is a problem that must be considered in the high power motor system.

At present, domestic and overseas scholars have carried out extensive and in-depth research on the problems of high switching loss [6–10] and high common mode voltage [11–15] of multilevel inverters, and have made a series of achievements. In terms of switching loss reduction, in Reference [6], a closed-loop control strategy based on carrier modulation is proposed, in which the clamping region is inserted in every half fundamental period to reduce switching loss. In Reference [7], the method of reducing switching loss by inserting the clamping region is adopted from Reference [6],

but on this basis, the PI (Proportional-Integral) controller is used to solve the problem of the neutral point potential shift. Under the condition of ensuring the neutral point potential balance, the clamping region is symmetrically distributed in the fundamental period, and the low-order harmonics of the inverter output are reduced. In Reference [8], the various performances of the inverter including switching loss and neutral point voltage are analyzed, the calculation complexity of the duty cycle is simplified, and the simplified model of switching loss is constructed. Through the re-distribution of redundant small vectors, the switching loss is restrained, while the neutral point voltage wave is reduced at that moment. In Reference [9], a "0-clamp" discontinuous modulation strategy is proposed. Based on the calculation method of the average error current vector, the space vector sector in the full modulation system is partitioned. The optimal clamping mode and region boundary of the output waveform quality are determined to reduce the switching loss on the basis of satisfying the high output performance of the inverter. In Reference [10], the discontinuous modulation method is also used to set the discontinuous range of phase voltage according to the load power factor, so as to realize the suppression of switching loss of the inverter under the condition of the variable load power factor.

In terms of common mode voltage suppression, in Reference [11], a method to reduce the frequency of common mode current by reducing the number of common mode voltage changes is proposed. When the switching sequence is arranged, the change times of common mode voltage can be reduced by reducing the commutation times. Compared with the traditional continuous and discontinuous modulation strategy of the three-level inverter, the THD of output current is higher because of the non-nearest three vector synthesis method. While the frequency of the common mode current is reduced, the amplitude is not suppressed. With the decrease of the modulation index, the common mode voltage will gradually increase, and the amplitude of the common mode current will also increase. In order to suppress the common mode voltage, a modulation strategy of eliminating the common mode voltage by using the method of three zero common mode voltage vector synthesis is proposed in Reference [12]. In order to facilitate the analysis of the switch state, the multi-level inverter is equivalent to the two-level inverter in the reference. Based on the modeling of the switching loss, the lowest switching mode can be selected. But due to the degree of freedom used in the switching state setting of the strategy, the THD of the output current and voltage of the inverter is greatly increased compared to the traditional strategy. In Reference [13], considering the shortcomings of the three zero common mode voltage vector in the output waveform quality of the inverter, a modulation strategy for improving the output waveform quality is proposed based on the degree of freedom set for the switching state, but the principle of the three zero common mode voltage vector must be satisfied. Additionally, the design and selection rules of the optimal switch sequence are obtained through the analysis of the current ripple. Based on the analysis of Reference [13], Reference [14] proposes a double zero vector synthesis sequence method, which can reduce the output current ripple while ensuring the zero common mode voltage amplitude of the inverter. In Reference [15], a method of reducing switching loss by adjusting the position of the zero vector in the sampling period is proposed, and the basic vector synthesis switching sequence with small common mode voltage amplitude is selected. However, the calculation process of this method is complex, and the strategy is essentially a continuous modulation strategy, the switching loss can be further reduced. However, it must be noted that References [12–15] all adopt the synthesis method of the non-nearest three vector, the ripple, and THD value of output waveform of the inverter will go up, especially in the low modulation index.

The improved modulation strategy of the above reference can only be applied to the asynchronous modulation mode with a high carrier ratio. When the carrier ratio decreased, due to the limitation of switching frequency of the inverter, the common mode voltage amplitude can still be reduced, but the quality of output waveform will be seriously reduced. When the switching frequency is further reduced, a synchronous modulation strategy is needed to ensure the synchronization and symmetry of the output phase voltage waveform of the inverter [16–20]. In Reference [18], the synchronous space vector modulation is introduced into the three-level inverter for the first time, and the modulation strategy under the condition of different parity of the reference

vector number is designed. In Reference [19], a multi-mode synchronous SVPWM (Space Vector Pulse Width Modulation) strategy with low switching frequency is proposed. By designing the switching sequence, the output waveform quality of the inverter is improved in the full modulation system. In Reference [20], four kinds of synchronous discontinuous space vector modulation strategies are proposed. Through four different phase voltage clamping methods, the output waveform quality of the converter is guaranteed and the switching loss is reduced. However, there are some problems in the strategy, such as large switching loss and high amplitude of common mode voltage, which need to be improved.

This paper presents a synchronous space vector modulation strategy that can reduce the switching loss and common mode voltage amplitude simultaneously at low switching frequency. Aiming at the switching loss and common mode voltage amplitude suppression, a new switching sequence design method is proposed based on the traditional switching sequence design rules. By using the redundant switching state of the three-level inverter space voltage vector, an improved modulation strategy is formed to achieve the simultaneous suppression of the switching loss and common mode voltage amplitude under the low-modulation index of NPC (Neutral Point Clamped) three-level inverter.

2. Space Vector Modulation of Three-Level Inverter

2.1. NPC Three-Level Inverter

The topology of NPC three-level inverter is shown in Figure 1.

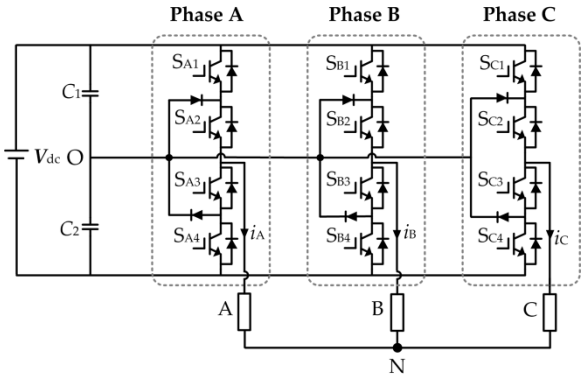

Figure 1. Topology of NPC three-level inverter.

Each phase leg has three switching states: P, O, and N. The definition is shown in Table 1. S_{x1}–S_{x4} represents the on-off state of four switches in X ∈ (A, B, C) phase, 1 represents on, and 0 represents off. There is a total of $3^3 = 27$ switching state combinations for three-level inverters, which corresponds to 19 basic voltage vectors in the space vector diagram. As shown in Figure 2, θ is the angle between the reference vector $\boldsymbol{V}_{ref}$ and α axis.

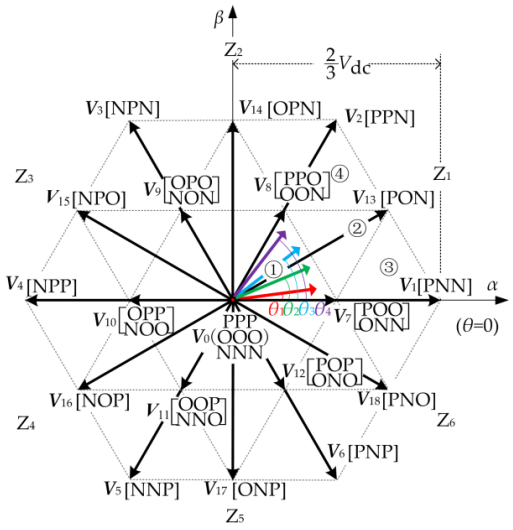

Figure 2. Space vector diagram of the three-level inverter.

Table 1. Contrast table of switching function and output level of the three-level inverter.

S_{x1}	S_{x2}	S_{x3}	S_{x4}	Level	Station
1	1	0	0	$V_{dc/2}$	P
0	1	1	0	0	O
0	0	1	1	$-V_{dc/2}$	N

Basic voltage vectors can be divided into four categories (one zero vector, six small vectors, six medium vectors, and six large vectors) according to their magnitudes. Each small vector corresponds to two switching state combinations and the zero vector corresponds to three switching state combinations. The whole space vector diagram can be divided into six sectors Z_1–Z_6 and each sector can be further divided into four small regions, as shown in Figure 2. In conventional synchronous space vector modulation strategies, the reference vector $\boldsymbol{V}_{ref}$ is synthesized by the nearest three basic vectors.

Modulation index m is defined as:

$$m = \frac{\sqrt{3}V_{ref}}{V_{dc}} \quad (1),$$

where V_{ref} is the amplitude of the reference vector. Taking $\boldsymbol{V}_{ref}$ in region ① of sector Z_1 as an example, $\boldsymbol{V}_{ref}$ is synthesized by the basic vector $\boldsymbol{V}_7$, $\boldsymbol{V}_8$, and $\boldsymbol{V}_0$. The dwell time of each basic vector can be calculated according to the principle of volt-second balance.

$$\begin{cases} \boldsymbol{V}_{ref}T_s = \boldsymbol{V}_7T_1 + \boldsymbol{V}_8T_2 + \boldsymbol{V}_0T_0 \\ T_s = T_1 + T_2 + T_0 \end{cases} \quad (2),$$

where T_s is the sampling period, T_1, T_2, and T_0 are the dwell times of basic vectors $\boldsymbol{V}_7$, $\boldsymbol{V}_8$, and $\boldsymbol{V}_0$, respectively.

2.2. Traditional Synchronized Discontinuous Space Vector Modulation Strategy

In synchronous space vector modulation strategies, reference vectors need to be evenly distributed in the space vector diagram. If the number of reference vectors N is odd, there will be a reference vector located at the center of each sector and the other reference vectors will be symmetrically distributed on both sides of the sector's center. While N is even, reference vectors shall not be located at the center of each sector [18]. Taking N = 4 and N = 5 as examples, distributions of reference vectors in sector Z_I are shown in Figure 3.

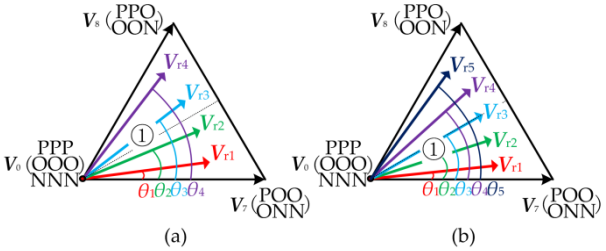

Figure 3. Distribution of reference vectors (**a**) $N = 4$ (**b**) $N = 5$.

When the inverter is operated under low carrier ratio conditions, in order to reduce the sub-harmonics, third harmonics and even harmonics, the output voltage needs to meet the synchronization conditions:

$$\begin{cases} v_{AO}(\theta \pm 2\pi) = v_{AO}(\theta) \\ v_{BO}(\theta \pm 2\pi) = v_{BO}(\theta) \\ v_{CO}(\theta \pm 2\pi) = v_{CO}(\theta) \end{cases} \quad (3).$$

Three-phase symmetry conditions:

$$v_{AO}(\theta) = v_{BO}\left(\theta + \frac{2}{3}\pi\right) = v_{CO}\left(\theta - \frac{2}{3}\pi\right) \quad (4).$$

Half-wave symmetry conditions:

$$\begin{cases} v_{AO}(\theta \pm \pi) = -v_{AO}(\theta) \\ v_{BO}(\theta \pm \pi) = -v_{BO}(\theta) \\ v_{CO}(\theta \pm \pi) = -v_{CO}(\theta) \end{cases} \quad (5).$$

Constrained by the above synchronization and symmetry conditions, the design principles of the switching sequence can be obtained as follows [19]:

Principle 1: There will be at most two switching of any arbitrary phase leg in each sampling period.

Principle 2: At most two-phase leg has switching in each sampling period.

Principle 3: At the intersection of two sample periods, the switching between P and N is not allowed in any arbitrary phase leg.

Principle 4: The terminal state of the current sampling period is the starting state of the next sampling period.

According to the above four principles, the traditional modulation strategy can be designed. Taking $N = 4$ as an example, when the modulation index $m \leq 0.5043$, the switching sequence of SDPWM$_{I}$~SDPWM$_{IV}$ in sector Z$_{I}$ is shown in Table 2 [20].

Table 2. Four SDPWM switching sequences with a low modulation index at $N = 4$.

	SDPWM$_{I}$	**SDPWM$_{II}$**	**SDPWM$_{III}$**	**SDPWM$_{IV}$**
V_{r1}	POO → PPO→ PPP	POO → PPO → PPP	OON → ONN → NNN	OON → ONN → NNN
V_{r2}	PPP → PPO→ POO	PPP → PPO → POO	NNN → ONN → OON	NNN → ONN → OON
V_{r3}	OON → ONN→ NNN	POO → PPO → PPP	OON → ONN → NNN	POO → PPO → PPP
V_{r4}	NNN → ONN→ OON	PPP → PPO → POO	NNN → ONN → OON	PPP → PPO → POO

Four clamping modes of the traditional synchronous discontinuous space vector modulation strategy are described in detail below. The A-phase voltage clamping state diagram of SDPWM$_{I}$~SDPWM$_{IV}$ is shown in Figure 4.

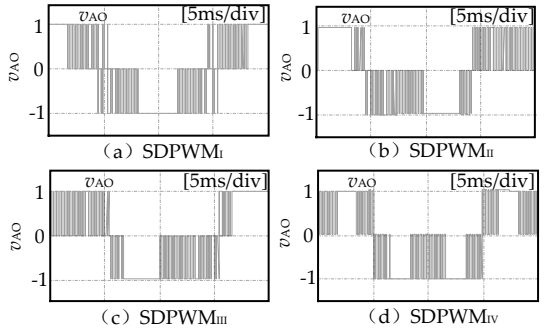

Figure 4. Clamping diagram of traditional synchronous discontinuous modulation strategy.

It can be seen from the switching sequence of the traditional synchronous discontinuous modulation strategy, shown in Table 2, that four kinds of synchronous discontinuous modulation strategies clamp one phase, respectively. It can be seen from Table 2 and the schematic diagram that when a phase is clamped in P state within 2π/3 cycle, that is, S_{A1} and S_{A2} keep 2π/3 cycle inactive; when a phase is clamped in O state in 2π/3 period, that is, S_{A2} and S_{A3} keep 2π/3 period inactive; when a phase is clamped in N state in 2π/3 period, that is, S_{A3} and S_{A4} keep 2π/3 period inactive. In other words, four kinds of discontinuous modulation strategies clamp a certain phase with a width of 2π/3 cycle in the fundamental period. As the switching device does not act in the clamping state, the switching times are reduced in the fundamental period, and then the switching loss of the whole inverter is reduced.

Taking SDPWMII as an example, there is no switching in phase A in sector Z_1, and the switching state is always P, which is defined as the clamping state P. Similarly, in SDPWMIII, there is no switching in phase C in sector Z_1, and the switching state is always N, which is defined as clamping state N. It can be concluded from Table 2 that distributions of clamping states for different modulation strategies are different in each fundamental period.

3. Improved Synchronized Space Vector Modulation Strategy

3.1. Switching Frequency Reduction

3.1.1. Switching Number Analysis of Conventional Modulation Strategy

From Section 1.2, taking $N = 4$ as an example, when the modulation index $m \leq 0.5043$, the switching times of SDPWMI~SDPWMIV in each fundamental period are 5, 5, 5, and 6, respectively.

As shown in Table 2, for SDPWMII and SDPWMIII, there is only one clamping state in each sector, and no additional switching occurs when sampling periods switch from one to another. However, at the boundary of the two sectors, additional switching is required because of the change of the clamping state (for example, when SDPWMIII switches between sector Z_1 and Z_2, the switching state of three-phase bridge arm needs to be changed from OON to OPO or OPN). For SDPWMI and SDPWMIV, the clamping state needs to be changed in each sector, so that there is additional switching (for example, when SDPWMI is switched from clamping state P to clamping state N, the switching state of the three-phase bridge arm is changed from POO to OON).

As shown in Figure 2, zero vector corresponds to three switching states: PPP, NNN, and OOO. Table 2 shows that PPP or NNN are adopted in SDPWMI~SDPWMIV, and OOO is not adopted. In fact, OOO can be used to design the switching sequence to further reduce the switching times of inverters.

3.1.2. Improved Design Method of Switch Sequence for Modulation Strategy

In order to reduce the switching caused by the change of the clamping state, an improved design method of switching sequence is presented.

Taking region ① of sector Z_1 as an example, as shown in Figure 5a, basic vectors V_0, V_7, and V_8 are used to synthesize the reference vector for the conventional modulation method. While in region ② of sector Z_I, the basic vectors V_7, V_8, and V_{13} are used to synthesize the reference vector. For the improved design method proposed in this paper, region I and region II are re-divided into region I and region II with medium vector V_{13} as the boundary. As shown in Figure 5b, when the reference vector is located in region I, the basic vectors V_0, V_7, and V_{13} are used. When the reference vectors are located in region II, the basic vectors V_0, V_8, and V_{13} are used to synthesize the reference vector. In order to further reduce the switching frequency of the inverter, two new principles are added based on Principles 1–4.

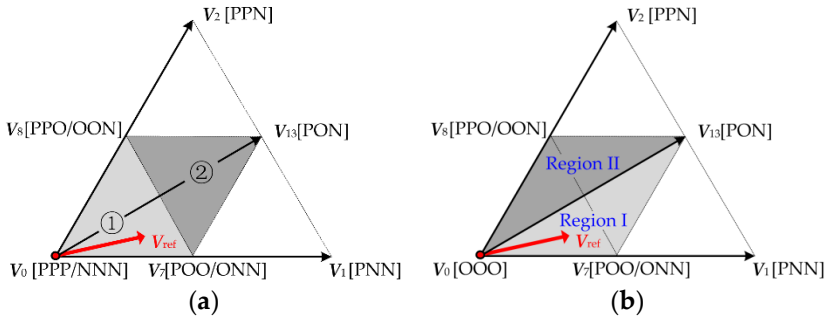

Figure 5. The division of small regions in Sector Z_1. (**a**) Conventional strategy; (**b**) improved strategy.

Principle 5: In each sampling period, the switching sequence need to start or end with the switching state corresponding to zero vectors.

Principle 6: Switching can only occur in one phase leg during each switching state alternation.

According to the parity of N, switching sequence synthesis can be divided into two modes.

Mode 1: When N is even, take sector Z_1 as an example. There is no reference vector in the center of the sector. Switching sequences $V_0 \leftrightarrow V_7 (V_8) \leftrightarrow V_{13}$ are used to synthesize the reference vector. The switching sequence in other sectors can be obtained in the same manner. At the intersection of the two sample periods, the switching state corresponding to zero or medium vector can be used for transition. At the boundary of the two sectors, the switching state corresponding to zero vector can be used for transition. Then, the additional switching action caused by the switching of the sample period, sector, or clamp state can be reduced.

Mode 2: When N is odd, there is a reference vector at the center of the sector, where $\theta = \pi/6$. Except for the reference vector at $\theta = \pi/6$, the switching sequences of other reference vectors V_{r1}~V_{r2} and V_{r4}~V_{r5} are the same as Mode 1, which is $V_0 \leftrightarrow V_7 (V_8) \leftrightarrow V_{13}$. The sequence of the reference vector is $V_7 (V_8) \leftrightarrow V_0 \leftrightarrow V_8 (V_7)$. This is because the starting/terminal switching state of V_{r3} is different from the terminal/starting switching state of V_{r2} and V_{r4}. There will be additional switching actions when the clamp state is changed, which is similar to that of conventional modulation strategies. However, compared with conventional strategies, the additional switching caused by the sector or clamp state switching can still be reduced.

3.2. Common-Mode Voltage Suppression

Common-mode voltage of the three-level inverter is defined as the voltage between load neutral point N and neutral point O of the DC-link capacitor. The relationship between the common-mode voltage and three-phase voltage can be expressed as follows:

$$\begin{cases} v_{AO} = L\dfrac{di_A}{dt} + Ri_A + v_{CM} \\ v_{BO} = L\dfrac{di_B}{dt} + Ri_B + v_{CM} \\ v_{CO} = L\dfrac{di_C}{dt} + Ri_C + v_{CM} \end{cases} \quad (6),$$

where L and R are load inductance and resistance, v_{AO}, v_{BO}, v_{CO}, i_A, i_B, and i_C are three-phase voltage and current, respectively, v_{CM} is common-mode voltage. As the three-phase load is symmetrical, the sum of three-phase current is zero:

$$i_A + i_B + i_C = 0 \quad (7).$$

According to Formulas (6) and (7), common-mode voltage can be expressed as

$$v_{CM} = \frac{v_{AO} + v_{BO} + v_{CO}}{3} = \frac{V_{dc}(S_A + S_B + S_C)}{6} \quad (8),$$

where S_A, S_B, and S_C are three-phase switching states of the inverter. The relationship between S_A, S_B, S_C, and the switching states of each phase switch device S_{x1}~S_{x4} is expressed as follows:

$$\begin{cases} S_A = S_{A1} + S_{A2} - 1 \\ S_B = S_{B1} + S_{B2} - 1 \\ S_C = S_{C1} + S_{C2} - 1 \end{cases} \quad (9).$$

K is defined as sum of switching algebra

$$K = |S_A + S_B + S_C| \quad (10).$$

According to the above analysis, in order to reduce the common-mode voltage, it is necessary to select the switching state with the minimum value of K to design the switching sequence. Thus, a new principle needs to be presented.

Principle 7: Priority should be given to the switching state with the minimum value of K during the design of the switching sequence.

In summary, with Principle 1–7 as constraints, an improved modulation strategy can be designed to reduce the switching loss and common-mode voltage amplitude simultaneously. The flow chart of the design process of the switching sequence is shown in Figure 6.

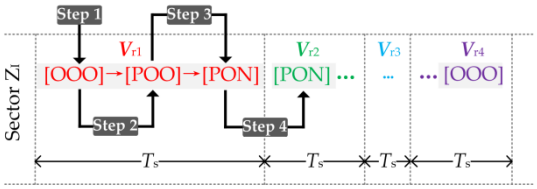

Figure 6. Flow chart of the sequence design of the improved modulation strategy.

From Principle 5 and 7, the starting switch state of V_{r1} is OOO. From Principle 6, the next switching state of V_{r1} is POO. The terminal switching state of V_{r1} is PON according to the region partition shown in Figure 5b. From Principle 4, the starting switch state of V_{r2} is PON, and so on. All switching sequences corresponding to V_{r1}~V_{r4} in Z_1 sector can be obtained, as shown in Table 3. Table 3 shows that there is no switching action in phase B and phase B is always clamped to switching state O.

Table 3. Switching sequence for V_{r1}~V_{r4} of the improved strategy in Sector Z_1.

V_{ref}	Switching State
V_{r1}	OOO → POO → PON
V_{r2}	PON → POO → OOO
V_{r3}	OOO → OON → PON
V_{r4}	PON → OON → OOO

4. Switching Loss and Common Mode Voltage Amplitude Analysis

4.1. Switching Loss Analysis

The power device used in the experiment is Infineon F3L100R07W2E3_B11 series IGBT. According to the datasSheet and the switching sequences of different modulation strategies, the expression of the switching loss can be obtained (11).

$$E = 3m\left[\begin{array}{l}\sum\limits_{j=2,4,6,8,10\ldots} E_{on}\left(\left|I\cos(\theta_{1\_j}-\varphi)\right|\right)+\sum\limits_{j=1,3,5,7,9\ldots} E_{off}\left(\left|I\cos(\theta_{1\_j}-\varphi)\right|\right)\\ +\sum\limits_{k=2,4,6,8,10\ldots} E_{on}\left(\left|I\cos(\theta_{2\_k}-\varphi)\right|\right)+\sum\limits_{k=1,3,5,7,9\ldots} E_{off}\left(\left|I\cos(\theta_{2\_k}-\varphi)\right|\right)\end{array}\right] \quad (11),$$

where I is the rms value of phase current, θ_{i_j} is the switching angle ($0 < \theta_{i\_j} < 2\pi$), i is the order of the switches, j and k are the order of the switching angle of each switch, ϕ is the power factor angle, and $-\pi/2 < \phi < \pi/2$. Since both SDPWM$_{I}$~SDPWM$_{IV}$ and the modulation strategies proposed in this paper satisfy half-wave symmetry or quarter-cycle symmetry, the switching angles of each modulation strategy can be translated from the values in the half-cycle or quarter-cycle to obtain the remaining switching angles in the fundamental cycle.

Taking the improved modulation strategy as an example, when N = 4, the switching angles of switches S_{A1} and S_{A2} in the first quarter of the fundamental period are shown in Table 4. According to Formula (11) and Table 4, the switching loss of the improved modulation strategy can be obtained. The switching losses of SDPWM$_{I}$~SDPWM$_{IV}$ can also be obtained in the same manner. Taking power factor angle $\phi = \pi/4$ as an example, the switching losses of different modulation strategies with the variation of the modulation index are shown in Figure 7. It shows that the switching loss of the improved modulation strategy is lower than that of the four conventional modulation strategies when $0 < m < 0.6$.

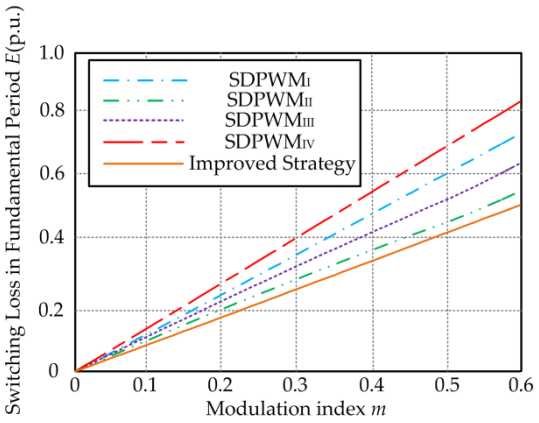

Figure 7. Switching loss figure at $\phi = \pi/4$.

Table 4. Switching angle of S_{A1} and S_{A2} of the upper arm in phase A in the quarter period.

Switching Angles S_{A1}	Switching Angles S_{A2}
θ_{1_1}: 15° [1 + 2m (sin (−52.5°)]	θ_{2_1}: 15° [9 − 2m sin (7.5°)]
θ_{1_2}: 15° [1 − 2m (sin (−37.5°)]	θ_{2_2}: 15° [9 − 2m sin (22.5°)]
θ_{1_3}: 15° [3 − 2m cos (67.5°)]	θ_{2_3}: 15° [11 − 2m sin (37.5°)]
θ_{1_4}: 15° [3 + 2m cos (82.5°)]	θ_{2_4}: 15° [11 + 2m sin (52.5°)]

4.2 Common-Mode Voltage Analysis

Taking SDPWM$_{I}$ and SDPWM$_{III}$ as examples, the switching sequence synthesized $\boldsymbol{V}_{r1}$ for SDPWM$_{I}$ is POO → PPO → PPP. The common-mode voltage generated by POO, PPO, and PPP are $V_{dc}/6$, $V_{dc}/3$, and $V_{dc}/2$. Thus, the common-mode voltage amplitude of sequence POO → PPO → PPP is $V_{dc}/2$. Similarly, the switching sequence synthesized $\boldsymbol{V}_{r1}$ for SDPWM$_{III}$ is OON-ONN-NNN, and the common-mode voltage generated by OON, ONN, and NNN are $-V_{dc}/6$, $-V_{dc}/3$, and $V_{dc}/2$. Thus, the common-mode voltage amplitude of sequence OON → ONN → NNN is $V_{dc}/2$. The common-mode voltage amplitude of SDPWM$_{I}$~SDPWM$_{IV}$ can be deduced by the above method, and the result is $V_{dc}/2$.

For the improved modulation strategy proposed in this paper, the switching sequence OOO → POO → PON is adopted to synthesize $\boldsymbol{V}_{r1}$, and the common-mode voltage generated by the OOO, POO, and PON is 0, $V_{dc}/6$, and 0, respectively. Thus, the common-mode voltage amplitude of sequence OOO → POO → PON is $V_{dc}/6$. The comparison shows that the common-mode voltage amplitude of the conventional modulation strategies is $V_{dc}/2$, and that of the improved modulation strategy is $V_{dc}/6$. The improved modulation strategy proposed in this paper effectively reduces the common-mode voltage amplitude.

5. Analysis of Experimental Results

In order to verify the feasibility and effectiveness of the proposed strategy, dSPACE DS1007 Rapid Prototyping Development System is used as the controller and the Infineon F3L75R07W2E3_B11 IGBT module is used to compose the three-level inverter. The prototype is shown in Figure 8, and the experimental parameters are shown in Table 5.

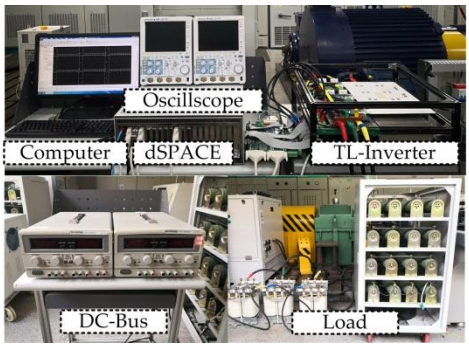

Figure 8. Physical figure of experimental system.

Table 5. Experimental parameters.

Parameters	Unit	Value
DC side voltage V_{dc}	V	100
DC side capacitor C_1, C_2	μF	1000
Load resistance R	Ω	10
Load inductance L	mH	40
Fundamental frequency f	Hz	50

Figures 9 and 10 show the experimental waveforms of phase voltage v_{AO}, line voltage v_{AB}, common-mode voltage v_{CM}, output current i_A, and upper and lower capacitance voltage for SDPWM$_{I}$~SDPWM$_{IV}$ and improved strategy（$N = 4$）under conditions of $m = 0.4$ and $m = 0.6$. As can be seen, compared with the four conventional synchronous discontinuous modulation strategies, when $m = 0.4$, the common-mode voltage amplitude of the improved strategy decreases from $V_{dc}/2$ to $V_{dc}/6$. When $m = 0.6$, the common-mode voltage amplitude of the improved strategy decreases from $V_{dc}/3$ to $V_{dc}/6$.

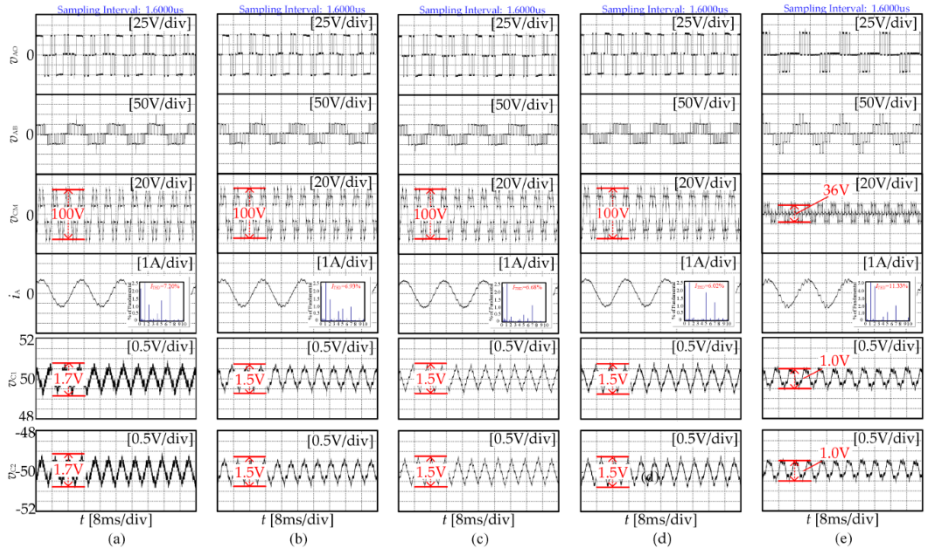

Figure 9. Experimental waveforms of SDPWM$_{I}$~SDPWM$_{IV}$ and the improved strategy at $m = 0.4$. (**a**) SDPWM$_{I}$; (**b**) SDPWM$_{II}$; (**c**) SDPWM$_{III}$; (**d**) SDPWM$_{IV}$; and (**e**) improved strategy.

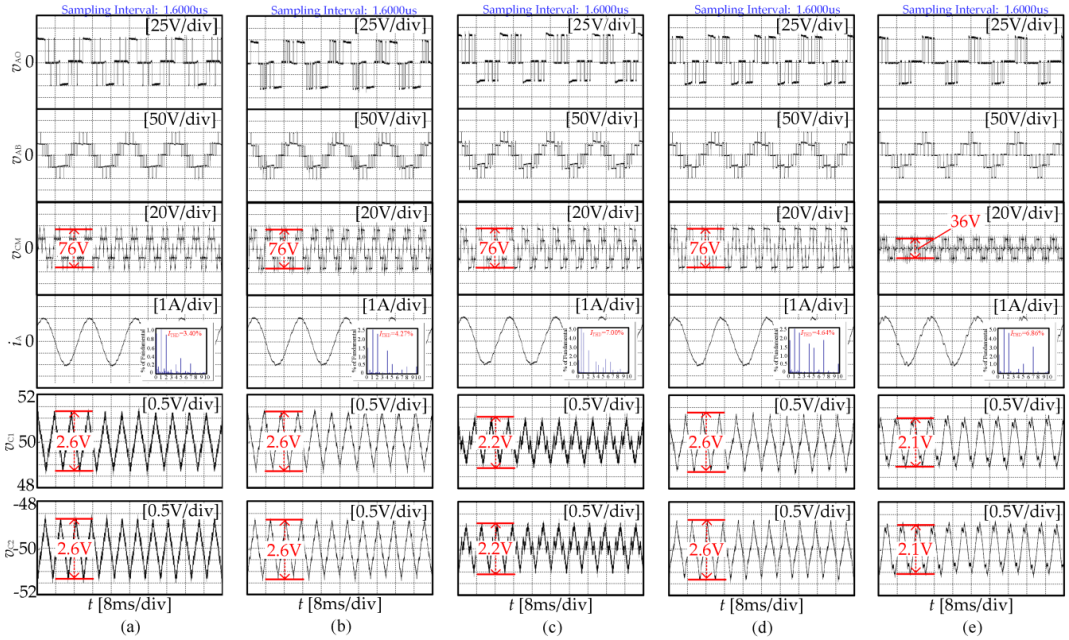

Figure 10. Experimental waveforms of SDPWM$_{I}$~SDPWM$_{IV}$ and the improved strategy at $m = 0.6$ (**a**) SDPWM$_{I}$; (**b**) SDPWM$_{II}$; (**c**) SDPWM$_{III}$; (**d**) SDPWM$_{IV}$; and (**e**) improved strategy.

It can be seen from the voltage waveform of the upper and lower capacitors that the ripple of the neutral point voltage of the modulation strategy proposed in this paper is slightly lower than that of the traditional method. When $m = 0.4$, the capacitance voltage ripple is reduced from 1.5 V–1.7 V of the traditional method to 1.0 V of the proposed strategy, and when $m = 0.6$ the capacitance voltage ripple is reduced from 2.2 V–2.6 V of the traditional method to 2.1 V of the proposed

strategy. It also can be seen that the output current waveform quality of the improved strategy is slightly lower than that of the conventional synchronous discontinuous modulation strategy, and that is because the improved strategy chooses the non-nearest three vectors to synthesize the reference vector.

6. Conclusions

In this paper, an improved synchronous discontinuous space vector modulation strategy for the NPC three-level inverter under a low modulation index condition is proposed. The modulation strategy has the following characteristics:

(1) By re-partitioning the small regions and making full use of the redundant switching state, the extra switching action during the switching between sector and clamp state is avoided. Taking $N = 4$ as an example, compared with SDPWM$_{I}$~SDPWM$_{IV}$, the improved strategy reduces switching times from five or six to four.

(2) The concept of the sum of switching algebra are introduced, and the switching states corresponding to zero and small vectors are selected according to the principle of the minimum sum of the switching algebra. Then, the common-mode voltage amplitude can be effectively reduced. Compared with SDPWMI~SDPWMIV, the common-mode voltage amplitude is reduced from $V_{dc}/2$ to $V_{dc}/6$.

The theoretical and experimental results show that the improved modulation strategy proposed in this paper can effectively reduce the switching loss and common-mode voltage amplitude of the inverter, and improve the efficiency and operational reliability of the inverter. The experimental results also verify that the modulation strategy proposed in this paper can effectively reduce the voltage ripple of the upper and lower capacitors of the NPC three-level inverter.

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