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Cost-Effective 4 GHz VCO Using Only Miniature Spirals Realized in a 0.18 µm CMOS Process for Wireless Sensor Network (WSN) Applications

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Abstract: This paper presents an extremely cost-effective radio-frequency integrated circuit (RFIC) implementation technique by employing a digital logic CMOS process and reducing area occupation for voltage-controlled oscillators (VCOs) using all miniature inductors for wireless sensor network (WSN) applications. The designed VCO operates in the 4.0 GHz band with a power consumption of 1.4 mW and a phase noise of −113.6 dBc/Hz at 1 MHz, occupying a Si area of 0.283 × 0.682 mm^2. In addition, we confirmed that the figure of merit (FOM) of 183.8 in our design is competitive with that of other LC-VCOs that were fabricated using the RF option and designed with conventional inductors.

Keywords: mixed/analog CMOS process; symmetric; helical inductor; voltage-controlled oscillator; VCO; phase noise

1. Introduction

With the rapid proliferation of wireless applications, the demand for power and cost-effective radios has significantly increased [1]. A typical battery-powered wireless sensor node can last only for a few days. Thus, low power consumption is the critical factor to sustain long-term operation. In particular, wireless sensor networks (WSNs) are autonomous devices combining sensing, power, computation, and communication functions into a single system [2]. For this case, saving the unit cost is sometimes more important than extended lifetimes, combined with progress in CMOS and MEMS processing and a minimum number of off-chip components, since a typical sensor network consists of a large number of small, low-cost nodes that use wireless point-to-point communication to construct a self-organized network [3].

From this point of view, to save the cost of a radio-frequency integrated circuit (RFIC) for the WSN unit cell, our design approach was focused on ensuring circuit area minimization and adopting cost-effective CMOS processes, respectively. Miniature spiral inductors clearly have advantages for RFIC fabrication cost because they can consume less silicon area significantly. For example, 3D helical inductors (3HIs) occupy significantly less silicon area than planar spirals because the turn is expanded vertically [4]. For this reason, many miniature voltage-controlled oscillators (VCOs) using asymmetric-helical spirals embedded in core LC tanks or harmonic-rejection filters have been reported [4,5]. In this paper, we expand this concept to create and demonstrate a size-efficient VCO based on only miniature spirals. Moreover, to additionally save design costs of fabrication, our VCO

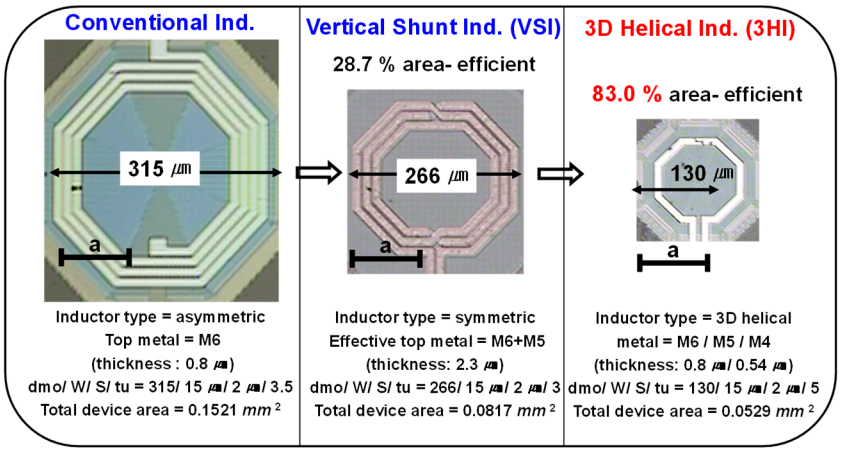
was implemented using a CMOS process for pure digital and analog (1-poly and 6-metal) signals; no process changes were made to improve the high-frequency characteristics of the devices.

2. Extreme Cost-Effective LC-VCO Circuit Design

In LC-VCO design, inductor performance of the LC tank plays a critical role in the phase noise and output signal power, simultaneously. Thus, for a low-cost LC-VCO implemented using a low-cost digital logic CMOS process with a thin top metal thickness (<1.0 um), a vertical-shunt inductor (VSI) was a good candidate as a tank spiral in our design [4].The reason is that the VSI is implemented by the neighboring metal layers that are shunted through arrays, in a mixed-signal CMOS process, and the effective metal thickness of the spiral can be increased up to 2.3 µm, which is comparable to the top metal thickness of the RF CMOS process without any additional cost. Figure 1 shows that the VSI has a size reduction of 28.7% and a higher Q-factor (8.74) at 4 GHz from measurement results compared with the conventional one. In the case of the 3D inductor, such as a helical spiral, the turn is expanded vertically [5]. Thus, 3D helical inductors (3HIs) have the advantage of small area occupation compared with planar inductors. As shown in Figure 1, a size reduction of approximately 83% using 3HI compared with a conventional inductor was achieved in exchange for a Q-factor degradation of 20%, whereas the inductance value of 2.2 nH close to 4 GHz was almost same. It had only a 50 µm radius and a 5 turn ratio, vertically. Thus, when considering a low-cost design such as WSN applications, the use of 3HIs for LC-VCO becomes one of the attractive solutions for saving the Si area effectively, although the use of low-layer metals causes Q-factor degradation and reduces the current handling capability. Additionally, the series inductance (L_s) and Q-factor for 3HIs with radius variation were extracted from the measurement results and are shown in Figure 2:

$$L_s = -Im\ (1/(w^*y_{21})),\ Q\text{-}factor = -Im\ (y_{11})/Re(y_{11}), \quad (1)$$

where w, y_{21}, and y_{11} represent angular frequency and y-parameters of a two-port network, respectively.



(**a**)

Figure 1. *Cont.*

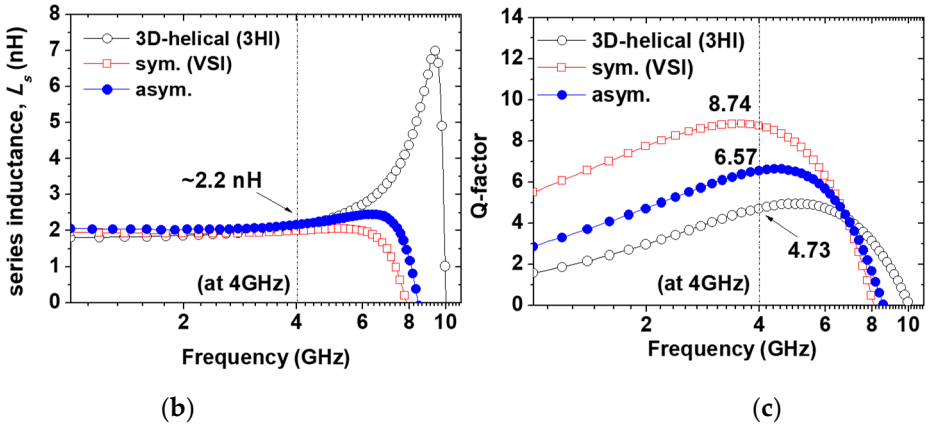


Figure 1. (**a**) Representation of three different types (conventional, VSI, and 3HI) of inductors with same inductance of 2.2 nH. (**b**) Measured series inductance (L_s) and (**c**) their Q-factors at 4 GHz.

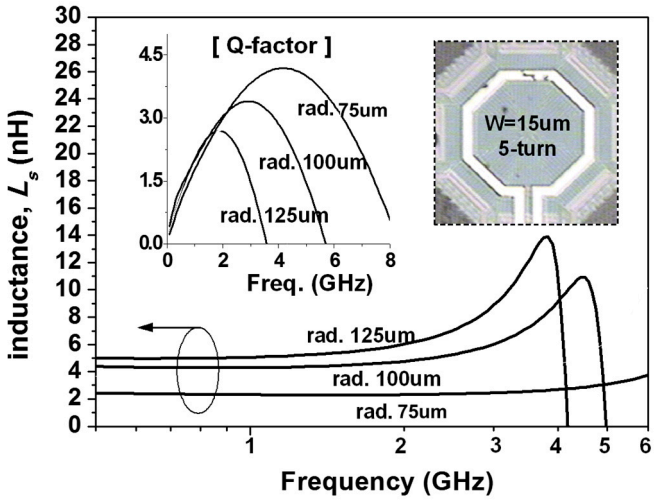
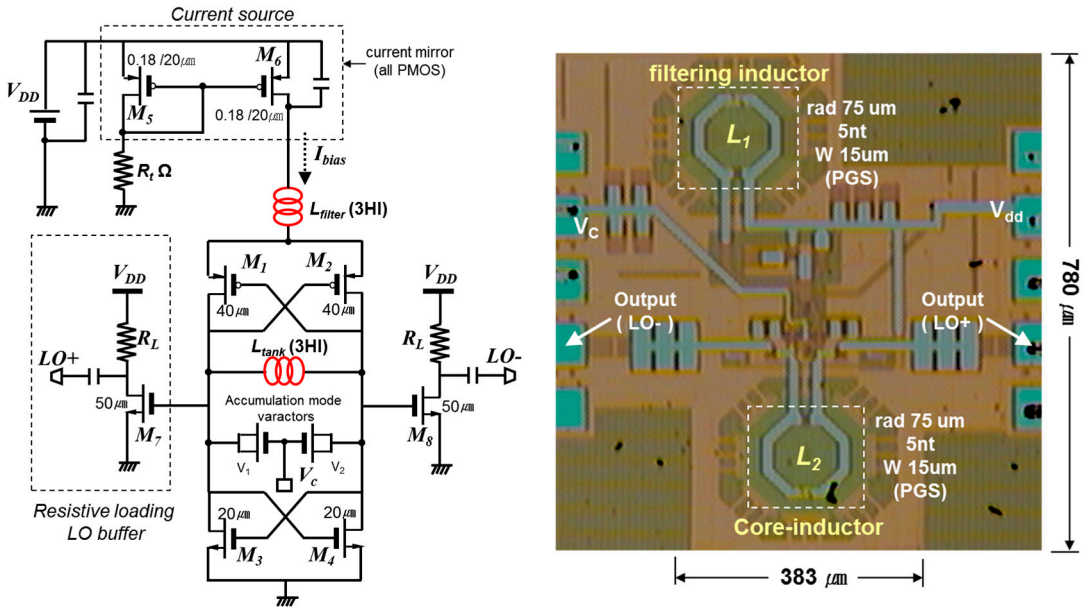


Figure 2. Measured inductance (L_s) and Q-factors of fabricated symmetric helical inductors.

A schematic diagram of the designed VCO is shown in Figure 3a. To achieve a better phase-noise performance based on waveform symmetry and higher amplitude, two symmetric cross-coupled N/PMOS pairs (M_1 to M_4) were employed; their positive feedback effectively compensates for the LC tank loss caused by the 3HI, L_{tank} [5–7]. Additionally, another helical spiral was also used in the filtering technique. L_{filter}, which is in series with the LC tank, encourages a high impedance supply voltage (V_{dd}) at $2\,f_o$.



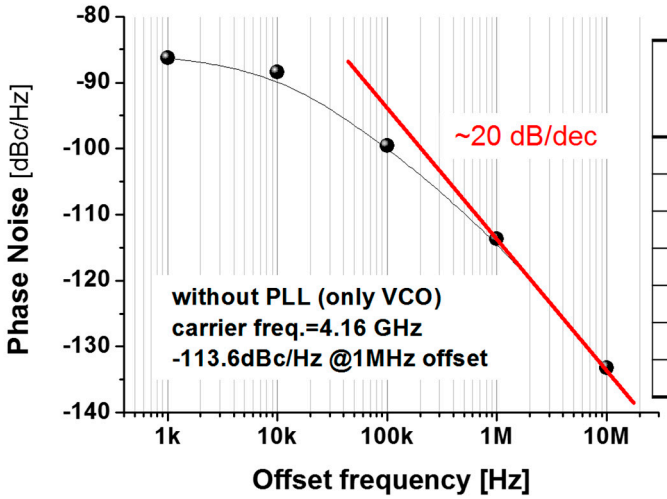
(**a**) (**b**)

Figure 3. (**a**) Designed LC-VCO schematic diagram. (**b**) Chip microphotograph (0.283 × 0.623 mm).

We used a large capacitor, C_x, to short noise frequencies around 2 f_o. The LC tank consisted of one symmetric helical inductor and two MOS varactors (V_1 and V_2). A 2.2 nH differential inductor with a poly-shielded ground was used in the LC tank; it had a Q-factor of 4.2 at 4 GHz. The accumulation-mode MOS varactor with an n+ poly gate in the n-well was used for frequency tuning [8]. The measured capacitance varied from 230 *fF* to 290 *fF* and the varactor's Q-factor was greater than 60. The effective parallel conductance of the LC tank was approximately 3.57 mS at 4.0 GHz. Thus, the required transconductance of NMOS (g_{mn}) and PMOS (g_{mp}) was 10.7 mS; in addition, the VCO bias current should be greater than 1 mA. However, for the definite oscillation and low phase noise within the current limited region, we had to increase the bias current flow in the VCO core; thus, the final DC current of the VCO was determined to be 1.3 mA.

3. Experimental Results

As shown in Figure 3b, the actual circuit area of the fabricated VCO (excluding pads) is 0.283 × 0.623 mm^2. The all-helical-inductor-based VCO has the following key circuit parameters: transistor size M_1 and M_2 (W/L) = 40/0.18 µm, M_3 and M_4 (W/L) = 20/0.18 µm, radius of L_1 and L_2 = 50 µm, with values of 2.2 nH at 4 GHz. Moreover, to suppress substrate loss in the spiral, a poly-patterned ground shield (PGS) was added and grounded metal-1 shields were used underneath the MIM capacitors and RF interconnects [6]. Figure 4 shows the measurement results for phase noise performance with offset frequency. An output power greater than -13 dBm was achieved with 1.4 mW of DC power consumption. The oscillator operated from 4.13 GHz to 4.34 GHz as a function of the tuning voltage (V_c) and therefore had a tuning range of 4.8%. Additionally, the phase noise of the fabricated VCO was found to be −113.6 dBc/Hz at a 1 MHz offset. Figure 5 presents the simulated and measured tuning range that the performed simulation showed under the 3% model error. All measurement testing was performed using an on-wafer system using an Agilent 8565E spectrum analyzer (Santa Rosa, CA 95403-1799, USA), in terms of oscillation frequency, output power, and phase noise.



Offset frequency.	Phase Noise [dBc/Hz] @ 4.16 GHz
100 Hz	-86.8
1 kHz	-86.3
10 kHz	-88.4
100 kHz	-96.6
1 MHz	-113.6
10 MHz	-133.2
100 MHz	-135.9

Figure 4. Measured phase noise with offset frequency.

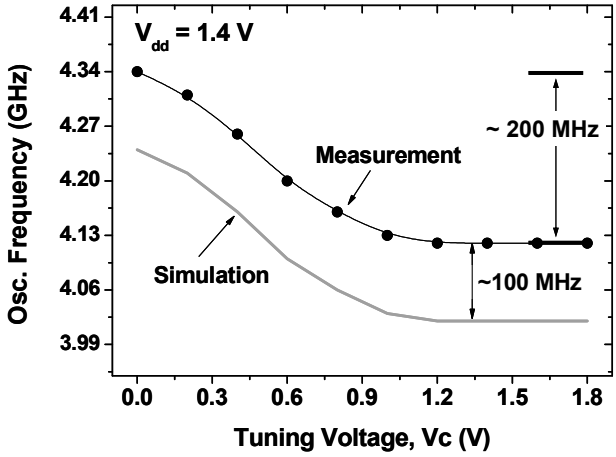


Figure 5. Comparisons between measured and simulated results.

For the performance comparisons of different oscillators, the typical figure of merit (FOM) is used as defined by [9]:

$$FOM = 10 \times \log\left(\left(\frac{f_0}{f_m}\right)^2 \frac{1}{L(f_m) \times P_{dc}}\right), \tag{2}$$

where $L\,(f_m)$ represents the phase noise at an offset frequency from the carrier frequency f_o.

Since a larger Si area is usually required to have a higher Q-factor of inductors, there is a trade-off between the Si occupation and FOM. Thus, the LC-VCO should be evaluated with another FOM (FoMA) that is normalized by area and described by the following equation [10]:

$$FoMA = FoM - 10log\left(\frac{Area}{1mm^2}\right). \tag{3}$$

Table 1 summarizes the measurement results and compares them to those reported in [11–16] that were operated at the 3–5 GHz band. We show that our VCO has a comparable figure of merit and small silicon area occupation with cost-effective advantages.

Table 1. Performance comparisons with reported VCOs.

Ref.	Technology	f_o (GHz)	V_{dd} (V)	Power Diss. (mW)	Phase Noise (dBc/Hz)	Offset Freq. (MHz)	Chip Size (mm^2)	FoM (dB)	FoMA (dB)
This work	CMOS 0.18μm (MS)	4.35	1.4	1.8	−113.6	1.0	0.193	183.8	190.9
[11]	CMOS 0.18μm (RF)	5.20	1.8	9.7	−113.7	1.0	0.350	180.0	184.6
[12]	CMOS 0.18μm (RF)	4.50	1.45	0.9	−117.0	1.0	0.180	184.0	191.4
[13]	CMOS 0.18μm (RF)	4.50	1.5	6.8	−122.5	1.0	0.546	187.0	189.6
[14]	CMOS 0.18μm (RF)	5.30	1.8	13.5	−124.0	1.0	–	187.2	–
[15]	CMOS 0.18μm (RF)	5.80	1.8	8.1	−110.0	1.0	0.806	176.2	177.1
[16]	CMOS 0.18μm (RF)	5.00	1.5	3.0	−120.4	1.0	0.4125	189.6	193.4

4. Conclusions

A cost-effective LC-VCO fabricated using a 0.18 μm digital CMOS process composed of all miniature spirals was proposed. 3HIs have a size reduction of 85% compared with conventional spirals and were applied to the LC tank and harmonic filter of the miniature VCO. The implemented LC-VCO had a power consumption of 1.4 mW and a phase noise of −113.6 dBc/Hz at 1 MHz offset at a 4 GHz frequency band. This work shows that the use of a 3D spiral combined with mixed-signal CMOS technology allows for the low-cost RFIC realization for WSN applications.

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Conflicts of Interest: The authors declare no conflict of interest.

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