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X-Band High-Efficiency Continuous Class B Power Amplifier GaN MMIC Assisted by Input Second-Harmonic Tuning

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Abstract: This paper presents a high-efficiency continuous class B power amplifier MMIC (Monolithic Microwave Integrated Circuit) from 8 GHz to 10.5 GHz, fabricated with 0.25 μm GaN-on-SiC technology. The Pedro load-line method was performed to calculate the optimum load of the GaN field-effect transistor (FET) for efficiency enhancement. Optimized by an output second-harmonic tuned network, fundamental to second-harmonic impedance, mapping was established point-to-point within a broad frequency band, which approached the classic continuous class B mode with an expanded high-efficiency bandwidth. Moreover, the contribution to the output capacitance of the FET was introduced into the output second-harmonic tuned network, which simplified the structure of the output matching network. Assisted by the second-harmonic source-pull technique, the input second-harmonic tuned network was optimized to improve the efficiency of the power amplifier over the operation band. The measurement results showed 51–59% PAE (Power Added Efficiency) and 19.8–21.2 dB power gain with a saturated power of 40.8–42.2 dBm from 8 GHz to 10.5 GHz. The size of the chip was $3.2 \times 2.4 \text{ mm}^2$.

Keywords: GaN; power amplifier; high efficiency

1. Introduction

The efficiencies of transmitters widely applied in radars, communication satellites, and base stations are predominantly determined by the efficiencies of applied power amplifiers (PAs) [1]. The pursuit of high-efficiency wideband PAs is an everlasting challenge.

Traditional harmonic-controlled high-efficiency PAs such as Class F [2,3] and Class J [4,5] modes are limited in bandwidth, due to the difficulty of realizing the required harmonic impedances over a wide bandwidth. Based on the bandwidth limitation of traditional harmonic-controlled PAs, Cripps proposed the continuous class B mode PA according to the method of waveform engineering [6]. By integrating the single transistor and output matching network, a continuous class B PA MMIC was presented by Powell [7]. However, this work did not realize the input matching network in the MMIC, which is important for a complete MMIC. As for the optimum load R_{opt} of PAs, the Cripps load-line model is a commonly used method [8]. However, when the nonlinear characteristics of field-effect transistors (FETs) were taken into consideration, the load-line method proposed by Cripps was not able to predict the FET efficiency [9]. Moreover, some studies showed that input harmonics have an important impact on the efficiency of PAs [10,11]. Furthermore, input harmonics can lead to a decrease

in the efficiency of measurement results with different input harmonics [12–14]. Thus, it is important to deal with input harmonics at the gate node of the FET when a high-efficiency PA is desired.

To deal with the above problems, this paper presents a wideband high-efficiency continuous class B PA MMIC adopting the Pedro load-line method [9] to obtain the R_{opt} for efficiency improvement. The contribution of the output capacitance of the FET is introduced into the output second-harmonic tuned network as a parallel LC tank, which simplifies the structure of the output matching network. Moreover, the optimized output matching network allows the proposed PA to work in continuous class B mode to expand the high-efficiency bandwidth. High-efficiency regions of the second-harmonic source impedance based on continuous class B mode are obtained through a second-harmonic source-pull simulation. To further improve the efficiency and extend the bandwidth of the power amplifier, the value of C in the input second-harmonic tuned network is calculated to achieve the smallest quality factor of the fundamental source impedances when the second-harmonic source impedances are moved into the high-efficiency regions over the operation band.

2. Efficiency Enhancement Methods of Continuous Class B Mode

The normalized waveform of continuous class B mode in the intrinsic drain plane as a function of parameter α [6] is shown in Figure 1a (see Equation (1)).

$$V_{DS}(\theta) = (1 - \sin \theta)(1 - \alpha \cos \theta), \quad -1 < \alpha < 1 \quad (1)$$

Figure 1. (a) The normalized voltage waveforms of continuous class B power amplifiers (PAs) from $\alpha = -1$ to $\alpha = 1$. (b) The desired fundamental and harmonic load impedances at the current source node of the field-effect transistor (FET) in continuous class B mode.

The desired fundamental and harmonic load impedances at the current source node of the FET in continuous class B mode are given as follows (shown in Figure 1b):

$$Z_{L,f} = R_{opt}(1 + j\alpha), \quad (2)$$

$$Z_{L,2f} = R_{opt} \frac{3\pi}{8} (-j\alpha), \quad (3)$$

$$Z_{L,nf} = 0, \quad n \geq 3, \quad (4)$$

where R_{opt} is the optimum load of continuous class B mode. It is noted that the desired impedances of continuous class B have many solutions which can expand the bandwidth of PAs. The efficiency of a continuous class B mode PA in all solutions is 78.5%, which is the same as class B mode.

2.1. The Choice of R_{opt} for Efficiency Enhancement

The Cripps load-line method, known as $R_{opt} = 2(V_{DD} - V_{knee})/I_{max}$, is commonly used in Class J and continuous class B power amplifier designs [5]. The R_{opt} obtained using this method is chosen for maximum output power. On the other hand, the R_{opt} obtained using the Pedro load-line method [9] for efficiency enhancement is given below.

$$P_{out} = \frac{1}{2} \frac{R_L}{(R_L + 2R_{ON})^2} V_{DD}^2, \quad (5)$$

$$I_{dq} = \beta \frac{1}{2K_x} \ln(2), \quad (6)$$

$$\eta(R_L) = \frac{\pi}{4} \frac{V_{DD}}{R_L + 2R_{ON}} \cdot \frac{V_{DD}}{V_{DD} + \frac{\pi}{2} X(I_{dq})(R_L + 2R_{ON})}, \quad (7)$$

$$X(I_{dq}) = I_{dq}^2 / \left(\frac{V_{DD}}{R_L + 2R_{ON}} + I_{dq} \right), \quad (8)$$

where R_L is the load of the transistor which sets the reactance component to zero, V_{DD} is the drain bias voltage, and β is the peak of the transistor's transconductance. As for the nonlinear parameter of the transistor, R_{on} is the turn-on resistance in the ohmic region, and K_x determines the soft turn-on characteristic of the FET. Using an $8 \times 100 \mu\text{m}$ GaN FET in class B operation as an example, the knee voltage V_{knee} and maximum drain current I_{Dmax} are 5 V and 0.8 A, β is 0.29 S, K_x is 9.5 V^{-1} , R_{on} is 6.25Ω , and V_{DD} is 28 V. An R_{opt} of 57.5Ω can be calculated using the Cripps method. The efficiency and output power deduced using the Pedro load-line method are shown in Figure 2. As is shown in Figure 2, the maximum efficiency of 74% is achieved at 260Ω , while the efficiency is below 64% at the R_{opt} of 57.5Ω . As seen in Figure 2, although the output power at $R_L = 57.5 \Omega$ is larger, the efficiency is nearly 10% less than the maximum efficiency of the FET achieved using Pedro's method.

Figure 2. (a) Drain efficiency and (b) output power of the $8 \times 100 \mu\text{m}$ FET calculated using the Pedro load-line method.

2.2. Input Second Harmonic Tuned in Continuous Class B Mode For Efficiency Enhancement

The input voltage V_{gs} of the FET at the gate node becomes distorted when the FET is under large-signal operation, which has a negative effect on the efficiency of the FET [11]. It is necessary to optimize the input harmonics to shape the waveform of V_{gs} and improve the efficiency of the FET. The input second harmonic is predominant in the distortion of V_{gs} , and the third and higher input harmonics can be ignored under large-signal operation [10].

Figure 3 shows the input second-harmonic source-pull results based on continuous class B mode when $\alpha = 0$ and $\alpha = 1$ at 10.5 GHz, when the fundamental source impedance is conjugation-matched. As shown in Figure 3a, when $\alpha = 0$, the maximum efficiency in the input second-harmonic source-pull

PAE contour is 70%. The second-harmonic source impedance of the maximum efficiency region is from $-j \times 18 \Omega$ to $-j \times 4.3 \Omega$. Moreover, the impedance of $(0.5 + j \times 3.5) \Omega$ leads to the lowest efficiency of 48%. Figure 3b shows the maximum efficiency of 70%, with impedance from $-j \times 6 \Omega$ to $-j \times 0.15 \Omega$ when $\alpha = 1$. The impedance of $(0.5 + j \times 9.5) \Omega$ leads to the worst efficiency of 54%. As shown in Figure 3, a suitable second-harmonic source impedance of the FET can improve the efficiency, and it is necessary to avoid the second-harmonic source impedance with the worst efficiency.

Figure 3. Input second-harmonic source-pull simulation results of $8 \times 100 \mu\text{m}$ FET with continuous class B mode at 10.5 GHz: (a) $\alpha = 0$; (b) $\alpha = 1$.

3. Circuit Design

The schematic of the proposed PA MMIC is shown in Figure 4. The presented high-efficiency X-band power amplifier consisting of a two-stage structure was fabricated using $0.25\text{-}\mu\text{m}$ GaN HEMT technology. The drain voltage of 28 V and quiescent current I_{dq} of $\sim 5\%$ of I_{Dmax} were set as the bias point. The output stage combined four $8 \times 100 \mu\text{m}$ FETs, and an $8 \times 100 \mu\text{m}$ FET was utilized in the drive stage. To ensure unconditional stability of the power amplifier, an RC parallel circuit and a shunt LRC circuit were inserted at the gate of each FET in the output and drive stages, respectively. According to Figure 2, $R_{opt} = 100 \Omega$ for each $8 \times 100 \mu\text{m}$ FET was chosen due to the tradeoff between efficiency and output power. The drain-source output capacitance C_{DS} and parasitic inductance L_D of the $8 \times 100 \mu\text{m}$ FET were 0.32 pF and 18.5 pH, respectively, extracted from the PDK (Process Design Kit) provided by the foundry. Because the dissipation of the drive stage was much lower than output stage, this design focused on the output stage to improve the efficiency of the proposed PA.

Figure 4. The schematic of the presented high-efficiency power amplifier.

Figure 5a shows the schematic of the output matching network containing the second-harmonic tuned network. Figure 5b shows the responses of second-harmonic load impedance versus L_{04} and C_{01} . As shown in Figure 6, the parallel LC circuit consisted of L_{04} and C_{DS_4} . C_{DS_4} was a constant representing the output capacitance of the FET. Because L_{DS_4} and L_{01} were much smaller than L_{04} , the resonant frequency of the parallel LC circuit was determined by L_{04} . As shown in Figure 5b, comparing curve A with curve B, the resonant frequency of the LC circuit varied with L_{04} . When L_{04} was increased, the resonant frequency of the LC circuit decreased, and the second-harmonic frequency shifted away from the resonant frequency. This brought the second-harmonic reactance of the output matching network at 16 GHz closer to the short point.

Figure 5. (a) The schematic of the output matching network; (b) the responses of second-harmonic load impedance versus L_{04} and C_{01}

Figure 6. The simplified output second-harmonic tuned network when L_{04} is analyzed.

As shown in Figure 7, the network composed of L_{03} , C_{02} , C_{03} , and 50Ω provided the resistive component in the second-harmonic frequency. The network and C_{01} were in parallel. As shown in Figure 5b, comparing curve A with curve C, when C_{01} became larger, the reactance of C_{01} moved closer to the short point, and the network composed of L_{03} , C_{02} , C_{03} , and 50Ω had less influence on the second-harmonic load impedance. This reduced the size of the resistive component of the second-harmonic load impedance, and the second-harmonic load impedance at 16 GHz shifted closer to the circle of $\Gamma = 1$ as C_{01} became larger.

Figure 7. The simplified output matching network when C_{01} is analyzed.

Utilizing the characteristics of L_{04} and C_{01} analyzed above, the second-harmonic load impedances from 16 GHz to 21 GHz were adjusted to curve D, and other elements in Figure 5a were optimized to meet the required impedance of continuous class B mode within the fundamental frequency band, where $L_{01} = 21$ pH, $L_{02} = 500$ pH, $L_{04} = 250$ pH, and $C_{01} = 540$ f F.

As shown in Figure 8, the response of the simulated output matching network conformed to the theoretical impedance of continuous Class B mode from $\alpha = 0$ to $\alpha = 0.5$, as illustrated in Figure 1b.

Figure 8. The simulated response of the output matching network from 8 GHz to 21 GHz.

Figure 9 shows the LC series resonant network and planes of $Z_1(\omega)$, $Z_2(\omega)$, and $Z_3(\omega)$. In this design, an LC series resonant circuit was inserted between the FET and interstage matching network to tune the second-harmonic source impedance of the FET. $Z_1(\omega) = A + j \times B$ was the input impedance of the FET. $Z_2(\omega)$ was the source impedance of the FET. $Z_3(\omega)$ was the source impedance of the FET with an LC series resonant network. The impedance of the series LC resonant network $X_{LC}(\omega)$ can be calculated as follows:

$$X_{LC}(\omega) = -j \cdot \frac{1 - \omega^2 / 4\omega_0^2}{\omega C}, \quad (9)$$

$$\omega_0 = \frac{1}{2\pi \sqrt{LC}}, \quad (10)$$

where ω_0 is the resonant frequency of the LC series resonant network, and Q_s is the quality factor of the $Z_3(\omega)$. Q_s can be calculated as follows:

$$Q_s = \frac{|Im(Z_3(\omega))|}{Re(Z_3(\omega))} = \left| \frac{B}{A} \right| + \frac{\omega \cdot A^2 \cdot C + \omega \cdot B^2 \cdot C}{A(1 - \frac{\omega^2}{4\omega_0^2})}. \quad (11)$$

Figure 9. The LC series resonant network and the planes of $Z_1(\omega)$, $Z_2(\omega)$, and $Z_3(\omega)$.

Figure 10 shows the high-efficiency second-harmonic source impedance regions in the operation band. The LC series resonant network and interstage matching network were in parallel. In the second-harmonic frequency, $Z_2(\omega)$ was mainly determined by $X_{LC}(\omega)$ and $Z_2(\omega) \approx X_{LC}(\omega)$, because $Z_3(\omega) \gg X_{LC}(\omega)$. According to Equation (9), $X_{LC}(\omega)$ at 21 GHz was closer to the area of inductive reactance than 16 GHz. In general design, the resonant frequency ω_0 is the center frequency of the second-harmonic frequency, which removes $X_{LC}(\omega)$ from the high-efficiency region at 21 GHz and worsens the efficiency of the power amplifier. In this design, to move $X_{LC}(\omega)$ into the operation band into the high-efficiency region, $X_{LC}(\omega)$ of 21 GHz was moved to the inductive side of the high-efficiency region, which was the short point in the Smith chart, and ω_0 was set as 21 GHz.

Figure 10. High-efficiency second-harmonic source impedance regions in the operation band, and the response of the second harmonic source impedance of the FET.

According to Equation (9), $X_{LC}(\omega)$ moved closer to the inductive region in the Smith chart as C became larger. Therefore, $X_{LC}(\omega)$ at 16 GHz was moved into the high-efficiency region when C was increased. According to Equation (11), an increase in C would result in Q_s becoming larger, leading to the deterioration of the bandwidth. In this design, $X_{LC}(\omega)$ at 16 GHz was moved to the boundary of the high-efficiency region by adjusting the value of C . Then, the lowest Q_s was achieved when the high-efficiency performance of the power amplifier was assured. The reactance in the boundary of the high-efficiency region was $-j \times 28 \Omega$ in Figure 10. According to Equations (9) and (10), $L = 0.16$ nH and $C = 0.35$ pF were obtained.

Figure 11 shows the stability of the proposed PA under small-signal and large-signal conditions. As shown in Figure 11a, the stability factors of the FETs in both stages were larger than the unit, revealing that the PA is stable under small-signal operation. The large-signal stability result of the proposed PA from 8 GHz to 10.5 GHz was determined using STAN software according to the pole-zero identification method [15], as shown in Figure 11b. As shown in Figure 11b, there were no unstable poles in the right half of the plane, which shows that the proposed PA is stable under large-signal operation.

Figure 11. (a) Small-signal stability factor of the output stage and driver stage in the proposed PA; (b) large-signal stability results for the proposed PA using the pole-zero identification method.

4. Measurement Results

The photograph of the proposed PA MMIC is shown in Figure 12. The chip dimension was $3.2 \times 2.4 \text{ mm}^2$. The proposed PA was measured under the pulse condition with a 100- μs pulse width and a duty cycle of 10%. The simulated and measured performances are summarized in Figure 13. As shown in Figure 13a, the measured saturated output power was within 40.8–42.2 dBm and 19.8–21.2 dB gain was achieved from 8 GHz to 10.5 GHz. The measured PAE at the saturated output power was 51.7–59% from 8 GHz to 10.5 GHz. As for the performance with a small signal, shown in Figure 13b, S_{21} ranged from 23.6 dB to 25.6 dB and S_{11} was lower than -10 dB from 8 GHz to 10.5 GHz. The difference between the measured $|S_{21}|$ and simulated $|S_{21}|$ was due to the increase in threshold voltage in the PA MMIC tapering out. Table 1 shows a comparison with recent reported state-of-the-art X-band PAs, which reveals that the proposed PA performs competitively in terms of efficiency and operation bandwidth. The presented PA in Reference [16] had an excellent performance in terms of PAE because it utilized an output second- and third-harmonic tuned method, which sacrificed performance in terms of operation bandwidth. Compared with the traditional harmonic controlled PA, the proposed PA has a wider operation bandwidth at the same level of efficiency.

Figure 12. Photograph of the proposed X-band power amplifier.

Figure 13. (a) Simulated and measured Pout, PAE, and gain versus frequency from 7.5 GHz to 11.5 GHz; (b) simulated and measured S-parameter versus frequency from 7.5 GHz to 11.5 GHz; (c) simulated and measured gain versus input power at 10 GHz.

Table 1. Comparison with recent reported state-of-the-art X-band power amplifier (PA) MMICs.

Reference	Technology	Operation Mode	Frequency (GHz)	P _{out} (dBm)	PAE (%)	G _p (dB)	Pulse/Duty (μs, %)
[16]	0.15 μm GaN	Class AB, output 2nd and 3rd harmonic tuned	10–10.5	40	45–61	19	Continuous Wave
[17]	0.25 μm GaN	Class AB	8.8–10.4	40–41	38–44	17–18	50, 15
[18]	0.25 μm GaN	Class AB, 3rd harmonic tuned	8.5–10.5	43.2–44.7	35–37	16–19.1	100, 10
[19]	0.25 μm GaN	Class AB, input and output 2nd harmonic tuned	7.8–8.8	43.5	50–52	18.5	Continuous Wave
[20]	0.25 μm GaN	Class AB	8.5–11	43–46.5	33–52	13–16.5	20, 10
This work	0.25 μm GaN	Continuous class B, input 2nd harmonic tuned	8–10.5	40.8–42.2	51.7–59	19.8–21.2	100, 10

5. Conclusions

This work presented an X-band high-efficiency power amplifier MMIC implemented in 0.25-μm GaN technology. The high-efficiency operation bandwidth of the proposed PA was extended with continuous class B mode utilizing an optimized output second-harmonic tuned network. Meanwhile, the efficiency of the proposed PA was improved through optimum second-harmonic source impedance and R_{opt} derived using the Pedro load-line method. The optimum second-harmonic impedance was tuned into the high-efficiency region utilizing an LC series circuit in the operation band. The quality factor of the fundamental source impedances was taken into consideration to determine the values of L and C in the LC series circuit. The method mentioned above was well verified in the presented PA, and excellent performance with a bandwidth of 27% and an efficiency of 59% was achieved.

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