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A Regulated Charge Pump with Extremely Low Output Ripple

Mir Mohammad Navidi and David W. Graham *

Lane Department of Computer Science and Electrical Engineering, West Virginia University, Morgantown, WV 26506, USA; minavidi@mix.wvu.edu

* Correspondence: david.graham@mail.wvu.edu

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Abstract: In this paper, we present a regulated charge pump with extremely low output ripple (<1 mV) that can be used for accurate programming of nonvolatile memory. We present a technique to include a low-drop-out regulator inside the charge-pump regulation loop to reduce the ripple. This charge pump was fabricated in a 0.35 μm standard CMOS process. The die area of this charge pump is 0.163 mm^2. While operating from a 2.5 V supply, this charge pump generates regulated voltages up to 10 V.

Keywords: charge pump; dc–dc converter; variable-frequency regulation; floating-gate transistor; analog nonvolatile memory

1. Introduction

Charge-pump (CP) circuits are used to multiply the supply voltage (V_{dd}) to generate a high-voltage DC output. These circuits have a wide range of applications including liquid-crystal display (LCD) drivers, micro electro-mechanical systems (MEMS), power-supply generation, and the programming of nonvolatile memory ([1–4]). Since charge pumps use switched-capacitor techniques to generate elevated voltages, the output of the charge pumps typically have significant ripple. However, in some applications, significant ripple cannot be tolerated.

In [5], we presented a high-voltage charge pump that was able to achieve relatively low output ripple by using a variable-frequency regulation technique. In this paper, we extend our previous results in [5] to achieve extremely low ripple in the output voltage. Specifically, our new objective was to be able to generate output voltages that are 2–4 times the supply voltage while maintaining an output ripple less than 1 mV. In this paper, we present a method to reduce output ripple in high-voltage charge pumps by adding a high power-supply-rejection ratio (PSRR) low-drop-out regulator (LDO) inside the regulation loop of the charge pump. In [6], we presented early results of such a circuit, and here we present an improved version that has significantly better line/load regulation and a more detailed stability analysis. We also use a feed-forward compensation technique to improve the phase margin of the LDO. The new charge pump was fabricated in a standard 0.35 μm CMOS process. While operating from a 2.5 V supply, the charge pump generates regulated voltages up to 10 V. The maximum efficiency of the charge pump is 25.7% for 48 μA of load current and an output voltage of 10 V. The output ripple is less than 1 mV for a wide range of load currents and output voltages.

In the remainder of this paper, we describe the development of this regulated charge pump. Section 2 describes the background of high-voltage charge pumps. Section 3 presents the details of the proposed charge pump and LDO, along with a stability analysis. The experimental results of the proposed charge pump are presented in Section 4, and conclusions are presented in Section 5.

2. Charge-Pump Background

A simplified version of a charge pump is shown in Figure 1a. By using alternating clock phases, ϕ_1 and ϕ_2, a large voltage at the output can be generated, where each charge-pump stage adds an additional V_{dd} to the output. The resulting output voltage is

$$V_{out} = (N+1)V_{dd} - N\frac{I_L}{C_p f}, \tag{1}$$

where N is the number of stages, I_L is the load current, C_p is the size of the pumping capacitor, and f is the frequency of the clock. Between clock phases, the load current discharges the output voltage, which results in a ripple in the output voltage given by

$$\Delta V = \frac{I_L \Delta t}{C_L}, \tag{2}$$

where C_L is the capacitance loading the output node and Δt is the period of the ripple, which is established by the clock frequency. Depending on the load current, the size of the capacitors, and the clock frequency, this ripple can be significant.

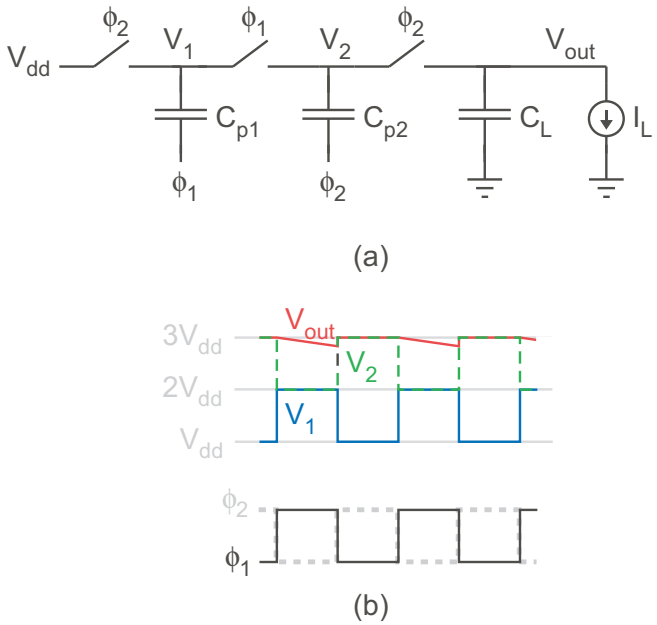

Figure 1. (**a**) Ideal charge pump. (**b**) Operation of the ideal charge pump.

From Equation (2), increasing the load capacitance can reduce the ripple, but doing so comes at the expense of a longer rise time and a significant increase in the area consumed by the circuit. Often, a large off-chip capacitor is used to ensure a low-ripple output (e.g., [7]). A number of designs have been introduced to help reduce the amount of ripple at the output while remaining fully integrated on-chip, with many of these designs focused on providing a low supply voltage for energy-harvesting applications [8,9]. The work in [10] showed that, for high-voltage charge pumps (e.g., $V_{out} > 2V_{dd}$), the output ripple and efficiency of a charge pump can be improved by using complementary charge-pump structures, and simulated ripples of 65–73 mV were achieved. The charge pumps of [11,12] leveraged closed-loop structures to achieve ripple voltages in the tens-of-millivolts range; however, closed-loop operation does not guarantee low ripple voltages [13,14].

In [5], we described a method to create a closed-loop charge pump that uses frequency regulation to help reduce the output ripple and still provide high output voltages. The circuit of [5] is shown in

Figure 2. Due to the frequency regulation in the closed-loop structure, the output ripple value can be established by setting capacitor values, as described by

$$\Delta V = \frac{C_p}{2NC_L}\left[(N+1)\,V_{dd} - V_{out}\right]. \tag{3}$$

This structure was able to provide ripple voltages down to the tens-of-millivolt range for reasonably sized on-chip load capacitances [5]. However, Equation (3) shows that improving the ripple is inversely proportional to C_L. Therefore, to achieve very low output ripple (e.g., <1 mV), the load capacitance would become too large to integrate on-chip. For example, the charge pump of [5] would require $C_L \gg 1$ nF for a ripple of 1mV, which would consume a considerable amount of chip real estate.

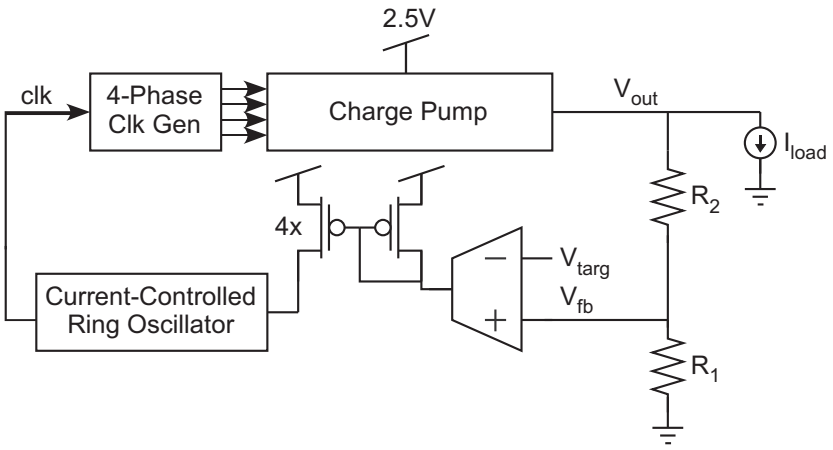

Figure 2. Block diagram of the variable-frequency charge pump we presented in [5].

Our application of this low-ripple charge pump is to precisely program analog nonvolatile memory elements. Programming floating-gate (FG) transistors, which are the core elements in many nonvolatile memory arrays, requires elevated voltages to enable Fowler–Nordheim tunneling and hot-electron injection to modify the charge on the "floating" gate voltage [15]. The amount of ripple provided by our charge-pump in [5] was acceptable for the global erasure mechanism (Fowler–Nordheim tunneling), since precise programming in the erasure mode is not necessary. However, to accurately program FG devices to an exact amount of charge, the hot-electron injection voltages must be controlled extremely precisely [16]. A key criteria for accurate programming of FG devices to a desired analog value is a precise voltage between the drain and the source. Using conventional programming techniques for analog floating-gate memories, such as [15–17], this criteria results in the need of a very precise supply voltage for the FG devices with extremely low ripple (less than 1 mV).

One common method to reduce variation in a supply voltage is to use a voltage-regulator circuit. Since we are using the charge pump to create an elevated supply voltage that enables hot-electron injection, a voltage regulator after the charge pump should be able to attenuate the ripple significantly.

As a result, a voltage regulator could follow a simple open-loop charge pump (which has a very large output ripple). This technique has two major problems. First, it is hard to achieve ultra-low output ripple (less than 1 mV), because the ripple at the output of the charge-pump is so large and because the output voltage of an open-loop charge pump is highly dependent upon the load current, as shown in Equation (1). Second, to be able to supply large-enough load currents, the output of an open-loop charge pump would have to be significantly high. Based upon simulations, in the case of our application, the charge-pump output voltage would need to be on the order of 20 V. This high voltage has a significant potential problem of stressing the devices in the voltage regulator, where high voltages across a single device can damage the junctions of the transistor.

Likewise, a closed-loop charge pump like Figure 2 could be used to generate relatively low output ripple, and it can then be combined with a voltage regulator to further reduce the output ripple. The voltage regulator could either follow the closed-loop charge pump or be placed within the feedback loop of the charge pump. Regardless, the stability and phase margin of the voltage regulator are critical factors in ensuring that the overall output voltage meets the needs of programming analog nonvolatile memory. If the high voltage produced by the resulting circuit ever overshoots its final value, that excess voltage could significantly affect the accuracy of programming. Since the hot-electron injection process depends exponentially upon the drain-to-source voltage [15], even a temporary overshoot of the desired supply voltage can result in drastic inaccuracies of programming analog nonvolatile memory. Since the elevated voltage for programming floating-gate transistors is only enabled when programming, the startup transients—particularly overshoot—are of critical importance.

In this paper, we present a circuit in which a low-drop-out regulator is inserted inside the feedback loop of a closed-loop, variable-frequency charge pump. The block diagram of the proposed charge pump is shown in Figure 3. This circuit is able to provide extremely low output ripple, and it can also be designed so that there is no possibility of overshoot of the output voltage, which will be discussed further in the frequency-stability discussion. Additionally, we present a method to self-bias a cascoded pass transistor in the voltage regulator, which helps improve the ripple suppression at the output.

Additional design considerations for the application of programming floating-gate transistors via hot-electron injection for analog applications are as follows. The exact voltage needed for hot-electron injection depends on the FG device being programmed. For a typical ~7 nm gate-oxide device (i.e., 3.3 V device), which is the minimum oxide thickness required for long-term charge retention on an FG [5], a source-to-drain voltage of approximately >5 V is required for reasonably fast programming via hot-electron injection [6,16]. However, the programming support circuitry in many floating-gate programming systems for analog applications requires additional voltage overhead, so the charge pump must be able to accommodate higher output voltages. In the system of [18], a voltage of 6.5 V is typically used. The required output current of the charge pump is modest, but it needs to be able to handle changing current values as the devices are programmed. In the programming system of [18], the charge pump needs to supply the programming support circuitry in addition to the FG transistors, themselves, and the maximum current is approximately 20 µA. Of note, the elevated voltages are only needed on an infrequent basis. Since the purpose of many programmable analog systems is for trimming, offset removal, bias current generation, and other values that require a static amount of charge on the floating gate [19], the charge pump used for providing injection voltages will only be turned on "as needed" for programming, which is likely an infrequent occurrence (e.g., daily, monthly, or yearly) and for a short period of time (approximately one second). Accordingly, high efficiency is not a critical need for this particular charge-pump application.

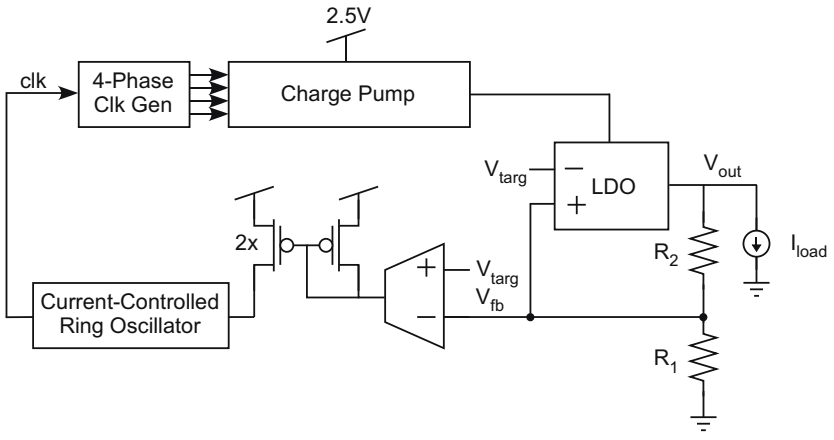

Figure 3. Block diagram of the proposed low-output-ripple charge pump.

3. Low-Output-Ripple Charge Pump

3.1. Closed-Loop Variable-Frequency Regulation

Figure 2 contains a block diagram of the high-voltage charge pump with variable-frequency regulation that we introduced in [5]. The operation of this circuit is as follows. Starting from the output node, a voltage divider shifts the output voltage down by a factor of $R_1/(R_1 + R_2)$ so that the feedback voltage (V_{fb}) is between ground and V_{dd}. The difference between V_{fb} and the target voltage (V_{targ}) is converted into a current through the combination of an operational transconductance amplifier followed by a rectifying current mirror, and this resulting current modulates the frequency of a current-controlled ring oscillator. After being split into a 4-phase clock, the modulated clock signal is used to generate the pumping voltages in the charge-pump block, which generates a high voltage. Due to the negative feedback, the output settles on a voltage of $1 + \frac{R_2}{R_1}$. Equation (3) provides a designable equation that can be used to reduce the ripple of the output voltage, but when using reasonably sized on-chip capacitors, this ripple can still result in a value that is too large for some applications, such as precise programming of floating-gate transistors.

To further suppress the ripple voltage at the output node, we introduce a low-drop-out regulator (LDO) inside the feedback loop, as depicted in Figure 4. The design considerations of this LDO are presented next to ensure that (1) all transistors operate in saturation for good ripple suppression and that (2) the system remains stable and does not have any overshoot of the final voltage value.

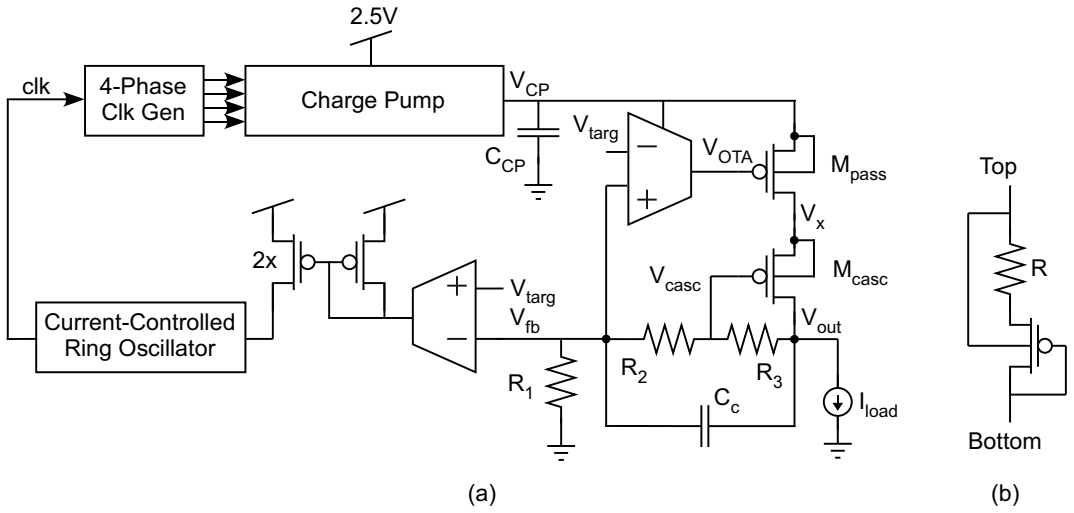

Figure 4. (**a**) Circuit diagram of the proposed injection charge pump with a low-drop-out regulator (LDO) in the loop. (**b**) Resistor divider cell.

3.2. Low-Drop-Out Regulator

A schematic of the LDO used in this charge pump is shown in Figure 5. Instead of using a single pass transistor, as is common in many LDO designs, we used a composite pass transistor composed of a series connection of two p-channel MOSFET (pFET) transistors in order to achieve extremely low output ripple. This LDO is based upon the high-PSRR LDO that was presented in [20]. The output impedance of the composite pass transistor ($M_{pass} + M_{casc}$) is much higher than that of a single transistor. Additionally, this cascode structure permits smaller device sizes ($M_{pass} + M_{casc}$) than would be required for a single pass transistor, which leads to smaller gate capacitance associated with the pass transistor. This reduced capacitance is an advantage because the parasitic capacitor that needs to be driven by the operational transconductance amplifier (OTA) is smaller, thereby relaxing the LDO compensation [20]. Since transistors M_{pass} and M_{casc} can be exposed to large voltages, these two transistors have been composed of thick-oxide I/O devices.

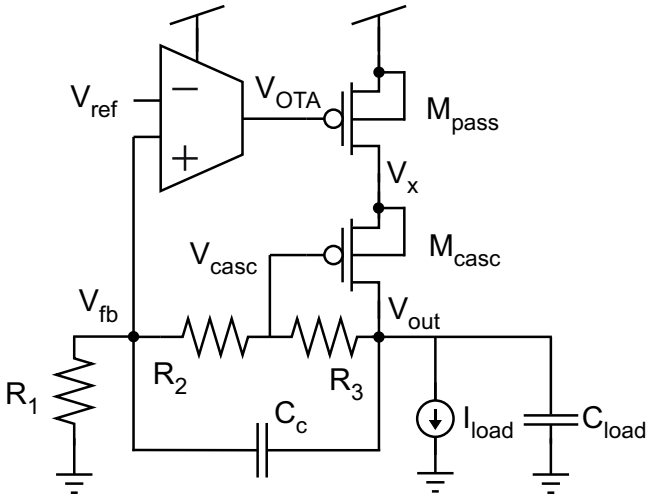

Figure 5. Circuit structure of the proposed LDO.

Providing a correct bias voltage to the gate of M_{casc} is a challenging task, particularly because the required voltage in steady-state is above the typical supply rail, and also during startup, the cascode bias needs to adapt to the rising voltages. This issue has not been covered in [20]. M_{casc} requires a voltage at V_{casc} to always keep this transistor in the above-threshold saturation region when the charge pump is enabled. Thus, V_{casc} must change adaptively with the output voltage during the initial startup transient. Designing a separate voltage source to provide V_{casc} would add more area and power overhead, particularly since $V_{casc} > V_{dd}$ in steady-state conditions, meaning that another charge pump would likely be needed just to generate this bias voltage.

In the proposed circuit, we use a simple technique to provide a suitable voltage for V_{casc}. A fraction of the output voltage is always available through the resistive divider. By using the resistive divider $(R_1 + R_2)/(R_1 + R_2 + R_3)$ from V_{out} to V_{casc} with $R_1 = R_2/3 = R_3$, we establish $V_{casc} = 4V_{out}/5$ at the gate of M_{casc} to bias this transistor in the correct region. Therefore, the maximum allowable voltage at V_{out} must be

$$V_{out} < 5|V_{Th,casc}| \tag{4}$$

to ensure saturated operation of M_{casc}, where $V_{Th,casc}$ is the threshold voltage of M_{casc} and the "*Th*" denotes the parameter of a thick-oxide transistor. Accordingly, the condition to keep M_{pass} in saturation is

$$V_{CP} > \frac{4V_{out}}{5} + V_{Th,casc} + \sqrt{\frac{2I_L}{K_{pass}}} + \sqrt{\frac{2I_L}{K_{casc}}}, \tag{5}$$

where V_{CP} is the output of the charge pump (i.e., input/supply voltage for the LDO) and $K_i = \mu C_{ox}(W/L)_i$. Equation (5) shows that M_{pass} can be biased in saturation for a given V_{out} and I_L by a correct choice of the W/L ratios of M_{pass} and M_{casc} and also by careful selection of the charge-pump parameters that set V_{CP}—specifically, the number of charge transfer stages (N) and the size of the pumping capacitors—as given by V_{out} in Equation (1). Note that the frequency of the charge pump from Equation (1) is dependent upon the load current and output voltage when placed in a closed loop.

Unlike our early results in [6] where the body of M_{casc} was tied to the output of the open-loop charge pump (V_{CP}), a body-source connected cascode device (M_{casc}) is used to minimize the threshold voltage for M_{casc}. Thus, the necessary V_{CP} in Equation (5) becomes smaller, which relaxes the design of the open-loop charge pump.

3.3. Stability Analysis of the LDO

A feed-forward capacitor, C_C, inside the LDO loop is employed to improve the loop stability of the LDO, as shown in Figure 5. The frequency analysis of the proposed LDO, including the feed-forward capacitor, is performed in this section. The first pole is at the gate of the pass transistor (M_{pass}). This pole can be expressed as

$$P_1 = \frac{1}{R_{OA}C_{pass}}, \tag{6}$$

where R_{OA} is the output impedance of the OTA, and C_{pass} is the parasitic gate capacitance. The output impedance of the OTA is high. However, the capacitance seen at the gate of the pass transistor is very small due to the cascode structure permitting a smaller pass transistor to be used than in a conventional LDO utilizing a single pass transistor. Thus, this pole resides at very-high frequencies. The compensation network adds one zero and one pole, which can be given by [21]

$$P_2 = \frac{5}{(R_2 + R_3)C_C} = \frac{5}{4R_{cell}C_C}, \tag{7}$$

$$Z_1 = \frac{1}{(R_2 + R_3)C_C} = \frac{1}{4R_{cell}C_C}, \tag{8}$$

where C_C is the compensation capacitor and R_{cell} is the single resistive cell expressed by Equation (12) and discussed in the next subsection. V_x is a low-resistance node, and the resistance seen from this node at low frequencies can be expressed as

$$R_x = \frac{1}{g_{m,casc}} + \frac{5R_{cell}}{g_{m,casc}r_{ds,casc}}, \tag{9}$$

where $g_{m,casc}$ is the transconductance of the cascode transistor and $r_{ds,casc}$ is the output impedance of the cascode transistor. Thus, the pole generated at this node resides at very-high frequencies. Finally, the last pole is at the output of the LDO. Assuming that C_L is the load capacitor and that the output resistance of this LDO is R_{out} as given by

$$R_{out} = \frac{10R_{cell}r_{ds,casc} + 5R_{cell}r_{ds}^2}{2r_{ds,casc} + 5R_{cell} + (A+4)R_{cell}r_{ds}g_{m,casc} + g_{m,casc}r_{ds}^2 + Ag_{m,pass}g_{m,casc}R_{cell}r_{ds}^2}, \tag{10}$$

then the output pole can be expressed as

$$P_{out} = \frac{1}{R_{out}C_L}. \tag{11}$$

As just described, the LDO presented in Figure 5 has four poles and one zero. P_1 and P_x are at very-high frequencies and are negligible. The other two poles (P_2 and P_{out}) and the zero (Z_1) are at lower frequencies and contribute significantly to the stability of the LDO. P_{out} is the dominant pole of this system. Z_1 compensates the effect of the other poles and improves the phase margin of the LDO regulator. The ratio of $P_2/Z_1 = 5$, and, therefore, the phase boost gained from the feed-forward compensation is observed between Z_1 and P_2, which is a narrow range. We set this range to be around the unity-gain bandwidth of the system for both no-load and 50 µA load currents. This frequency range and the peak phase boost are visible in the loop-gain simulations shown in Figure 6 for both no-load and 50 µA load conditions. Consequently, the phase margin can be made large enough so that there will be no significant overshoot. The phase margin for the no-load and 50 µA load-current conditions are 73 and 67 degrees, respectively, which indicates that the LDO will not undergo significant overshoot in startup conditions. The supply voltage that we used for the LDO in this simulation was 8 V, and the load capacitor was 80 pF, which are typical values for our application.

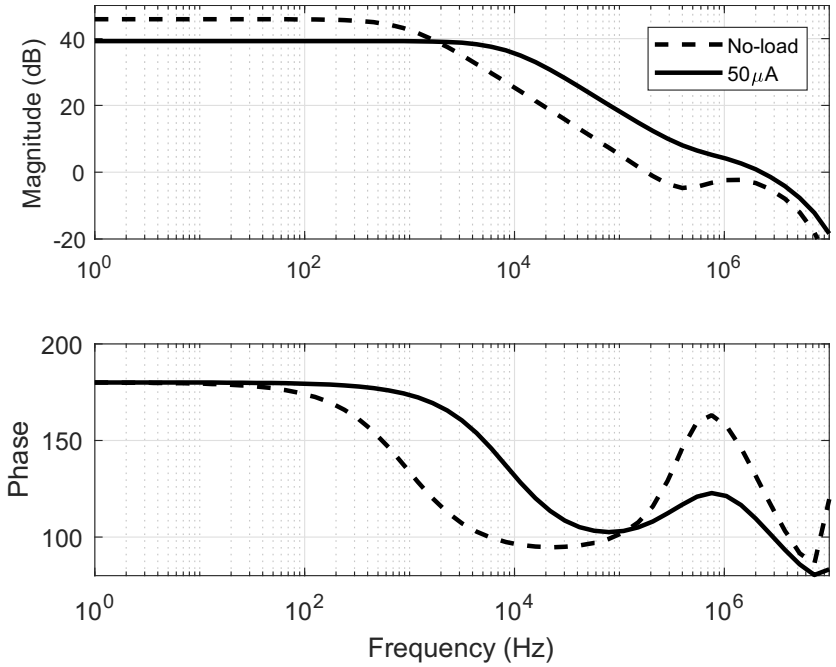

Figure 6. Simulated loop gain of the proposed LDO under no-load and 50 µA load.

In the complete charge-pump circuit, the current consumed by the amplifier is directly drawn from the open-loop charge pump. Increasing this current will directly affect the actual load current limit of the charge-pump circuit. To reduce this current to the minimum level, we have used a simple 5-transistor OTA as our amplifier. This simple OTA will limit the loop-gain of the system, however. Therefore, there is a trade-off between the current consumption of the OTA and the maximum achievable loop gain to improve the PSRR of this system.

3.4. Complete Charge Pump

Figure 4a shows the block diagram of the entire low-output-ripple charge pump, including the LDO. The charge-pump block is constructed from a cascade of seven charge transfer stages (CTS). Seven stages were needed so that V_{CP}, which is the output of the charge-pump block, is able to meet the criteria of Equation (5) for the desired V_{out}, I_L, and the transistor sizes needed in the LDO pass transistors.

The schematic of the CTS block is given in Figure 7. A brief synopsis of the CTS is as follows, and a detailed description of the CTS is provided in [5]. The CTS blocks leverage a 4-phase non-overlapping clock, as shown in Figure 7b, that allows the parallel upper/lower paths of the CTS to operate in opposite phases, thereby helping to reduce the overall ripple. Two switches in series (e.g., M_{sw1} and M_{sw3}) are used to limit the voltage drop across any single transistor to only V_{dd} so that the transistors do not undergo significant stress. Active-well biasing (M_{bb} transistors) is used to ensure that the wells of the switch transistors (M_{sw} transistors) are always biased to the highest potential encountered by the switch transistors.

To reduce the area required for each resistor in the LDO feedback loop, we used the resistive elements shown in Figure 4b. Each resistive element is composed of a series combination of a drawn resistor (98 kΩ) and a pFET, both in a single well. The diode connection of the transistor provides a current-level-based voltage drop across the transistor. Additionally, using the voltage at the top of the resistor to bias the well potential of the pFET increases the effective threshold voltage of the transistor, further increasing the voltage drop across the transistor for a given current level. As a result, the voltage dropped over the entire resistive element for a given current (i.e., a resistance) is increased. The pFETs are much smaller than typical drawn resistors, so significant real estate may be saved by using a smaller drawn size of the resistor. Since these resistive elements are used in a

resistive divider, only the ratio of the resistances affects performance of the charge pump; therefore, any current-level-based voltage drops due to the transistors will cancel out. Each resistive element has a resistance given by

$$R_{cell} = \frac{(g_m + g_{mb})R + \frac{R}{r_o} + 1}{g_m + \frac{1}{r_o}} \approx \left(1 + \frac{g_{mb}}{g_m}\right) R + \frac{1}{g_m}. \tag{12}$$

$R_1 = R_3$ are each composed of a single resistive element. R_2 is composed of three of the resistive elements in series for a total resistance that is three times that of R_1 and R_3. The effective R_{cell} used in our design is 195 kΩ. Thus, the total resistive divider section has an effective resistance of 975 kΩ.

Figure 4a shows the schematic of the complete charge pump with an LDO in the loop, and the operation of this entire circuit is as follows. Starting from the output node, a voltage divider shifts the output voltage down by a factor of $R_1/(R_1 + R_2 + R_3) = 1/5$, where $R_1 = R_2/3 = R_3$. Accordingly, the feedback voltage (V_{fb}) is between ground and V_{dd} and can be measured by the circuitry that is powered by the nominal V_{dd}. The difference between V_{fb} and the target voltage (V_{targ}) is converted into a current through the combination of an OTA followed by a rectifying current mirror. This resulting current modulates the frequency of a current-controlled ring oscillator, which has a frequency range from approximately 200 Hz to above 50 MHz. After being split into a 4-phase clock, the modulated clock signal is used to generate the pumping voltages in the charge-pump block, which generates a high voltage. The LDO structure then suppresses the ripple of the charge-pump output, and the resistive divider ensures that the output voltage is regulated to $V_{out} = 5V_{targ}$ with a very small output ripple.

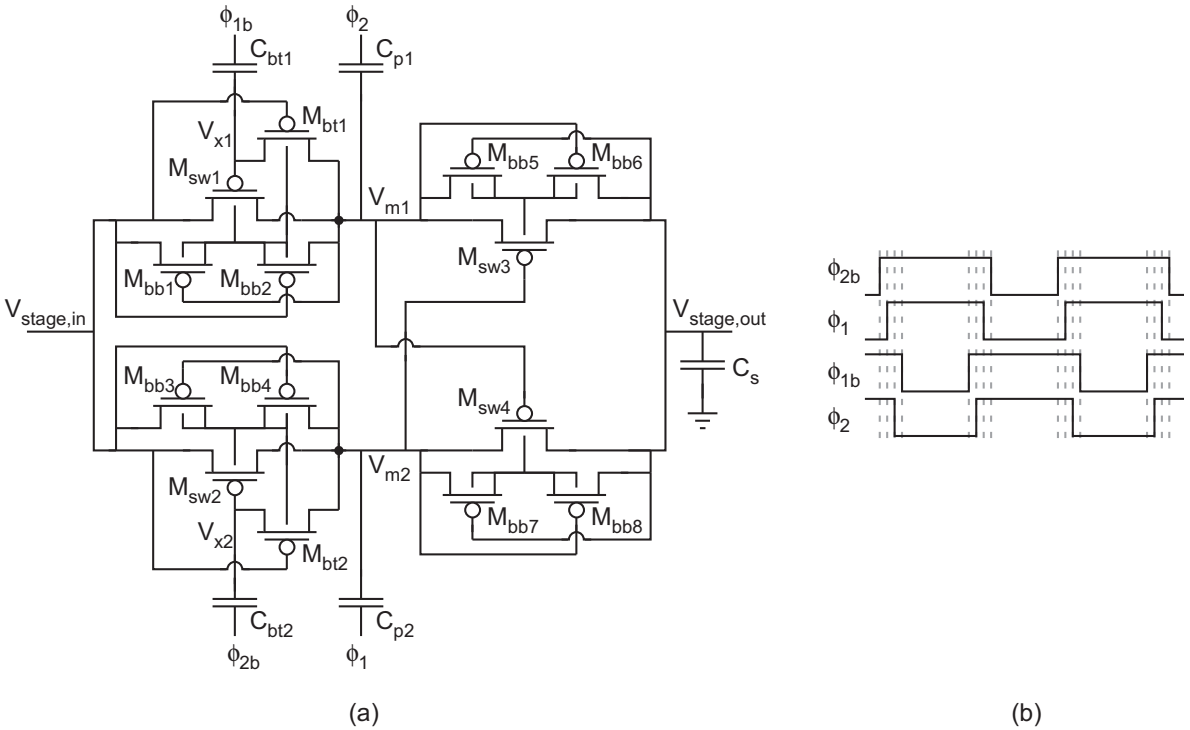

Figure 7. (**a**) The charge transfer switch (CTS). (**b**) Non-overlapping clock signals necessary for the charge-pump stages.

4. Measurement Results

The complete charge pump was designed and fabricated in a 0.35 µm standard CMOS process with device sizes given in Table 1. The rated supply voltage for this process is 3.3 V, and the chip supply voltage is regulated down to 2.5 V for the operation of the charge pump (as well as the floating-gate transistors and their supporting circuitry). The die area of this circuit is 504 µm × 324 µm. The die

photo of the proposed charge pump is shown in Figure 8. Both differential amplifiers used in this circuit are conventional 5-transistor OTAs.

Table 1. Charge pump specifications.

Element	Value
Technology	0.35 µm CMOS
V_{dd}	2.5 V
# Stages	7
C_{bt}	110 fF
C_p	2.36 pF
C_{CP}	3.93 pF
C_C	787 fF
M_{bb}	3 µm × 0.35 µm
M_{bt}	3 µm × 0.35 µm
M_{sw}	5 µm × 0.35 µm
M_{pass}	20 µm × 0.5 µm
M_{casc}	10 µm × 5 µm
$R_1 = R_2/3 = R_3$	195 kΩ

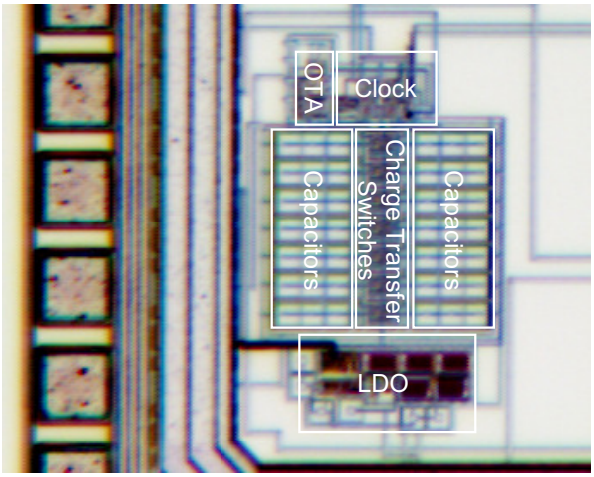

Figure 8. Die photo of the proposed charge pump.

A Tektronix MSO4054 Mixed-Signal Oscilloscope (500 MHz) was used to measure the output voltage. The supply voltage and the target voltage were provided by an Agilent E3631A Programmable DC Power Supply. The load current was set by a custom off-chip current sink and was verified by a Keithley 6485 Picoammeter.

Figure 9a shows the measured transfer curve from V_{targ} to V_{out}. The slope of this curve is 5, which shows that the charge pump can generate a high voltage equal to $5V_{targ}$. Deviation from the ideal line at the low voltages is because the input transistors of the OTAs drop out of saturation with low V_{targ}; however, since the charge pump only needs to supply voltages greater than the supply voltage, the transfer characteristic does not need to follow the ideal slope of $5V_{targ}$ for $V_{targ} < 0.5$ V, thereby significantly relaxing the requirements of the OTA designs. Deviation at high voltages is caused by the limitations imposed on the cascode transistors described by Equations (4) and (5). Figure 9b shows the closed-loop load regulation of the proposed charge pump for multiple output voltages, which were set by changing the value of V_{targ}. The hot-electron injection process of floating-gate transistors requires that the voltage generating the injection conditions be constant with a range of load currents [16,18], and Figure 9b indicates that this circuit is capable of providing a consistent output voltage under varying load currents.

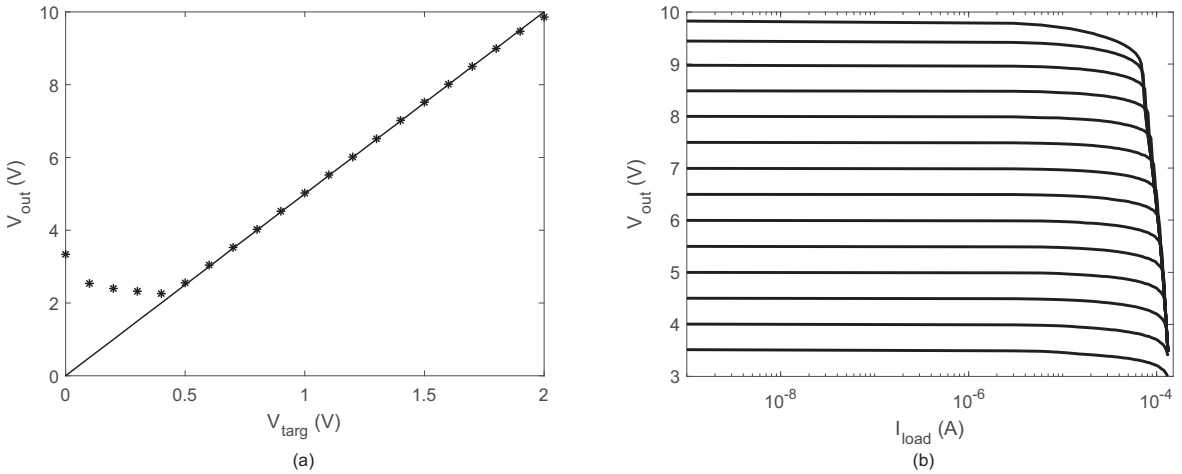

Figure 9. (**a**) Measured transfer curve from V_{targ} to V_{out}. (**b**) Measured load regulation of the charge pump.

A typical value for an injection voltage in a 0.35 µm standard CMOS process is 6.5 V [6]. Figure 10 shows the measured transient response for a typical programming pulse. The charge pump is enabled and disabled, with a steady-state output voltage of 6.5 V while loaded with a 40 µA load current and an approximately 80 pF load capacitance. The output reaches steady-state conditions in less than 0.2 ms. According to our measurements, the output voltage of the proposed charge pump under different load currents converges to $5V_{targ}$ with a behavior that is between critically damped and over-damped, meaning that there is no overshoot. Preventing overshoot is critical in floating-gate programming applications where a small change in the voltage can seriously impact the accuracy of programming.

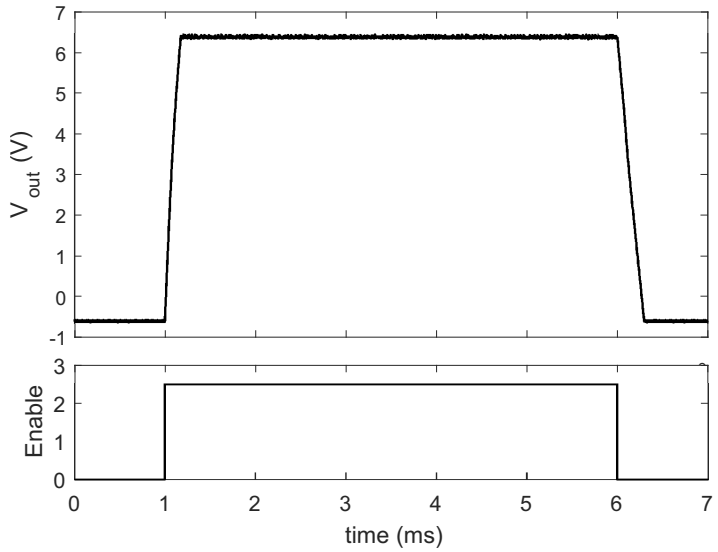

Figure 10. Measured transient response of the proposed closed-loop charge pump under 40 µA load.

The current consumption of the proposed charge pump is 0.73 mA and 1.2 mA for no load and 100 µA of load, respectively. The efficiency of a charge-pump is the ratio of the power delivered by the charge pump to the power supplied to the charge pump, as described by

$$\gamma = \frac{V_{out} I_L}{V_{dd} I_{vdd}}. \tag{13}$$

The measured efficiency of this circuit is shown in Figure 11a for output voltages of 6.5, 9, and 10 V and varying load currents. The maximum efficiency is 25.7% and is for the 10 V output case.

The measured efficiency is also shown for various step-up ratios (V_{out}/V_{dd}) and load currents in Figure 11b. As also indicated by Figure 11, the charge pump provides better efficiency for higher step-up ratios. However, a low efficiency number is not an issue in the charge pumps used for floating-gate programming because the charge pump is only enabled for a short period of time while programming the floating-gate transistors; otherwise, the charge pump is disabled.

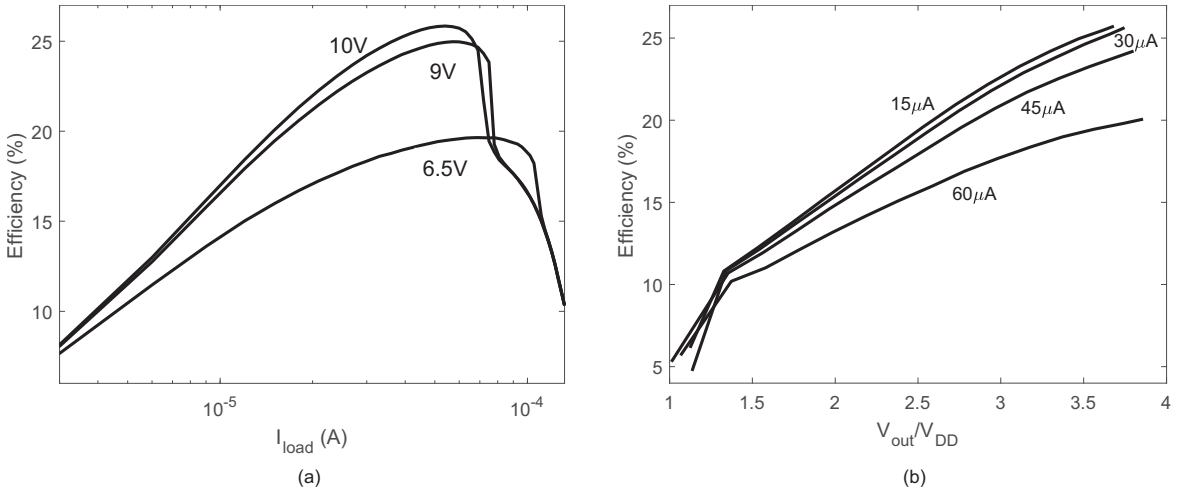

Figure 11. (**a**) Measured efficiency of the proposed charge pump vs. I_L. (**b**) Measured efficiency of the proposed charge pump vs. V_{out}/V_{dd}.

The output impedance of the proposed charge pump with $I_L = 50$ µA for different output voltages is shown in Figure 12. The output resistance (R_{out}) stays under 4 kΩ for a wide range of output voltages. R_{out} begins to increase when $V_{out} > 9$ V because the loop gain of the system reduces with very-high output voltages.

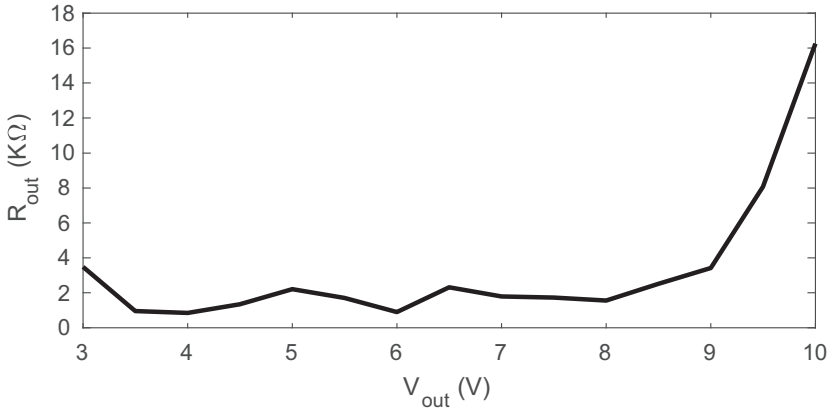

Figure 12. Measured output resistance.

The amount of ripple at the output can have a significant impact on the accuracy of programming floating-gate transistors. As can be seen from Figure 10, the ripple on the output voltage is very small. Because the ripple was smaller than the limits of our measurement equipment (i.e., within the quantization noise), we leveraged RC-extracted simulations under similar conditions as our experimental setup of Figure 10 to determine the amount of ripple. The RC-extracted simulation results are shown in Figure 13 with $V_{out} = 6.5$ V, $C_L = 80$ pF, and $I_L = 1$ µA. Figure 13 shows that the output ripple was approximately 1mV, which is sufficiently low for our analog nonvolatile memory programming application. Of note, this load capacitance is small enough that it can easily be integrated on-chip, and even larger integrated capacitances could be used to further reduce the ripple. Furthermore, these results show the effectiveness of the charge-pump-LDO loop combination; even

the relatively low output ripple of the variable-frequency charge pump of [5] would have required $C_L \gg 1$ nF to achieve sub 1mV ripple, which is far too large to integrate on-chip in most applications. The LDO in the loop reduces the necessary load capacitance by several orders of magnitude.

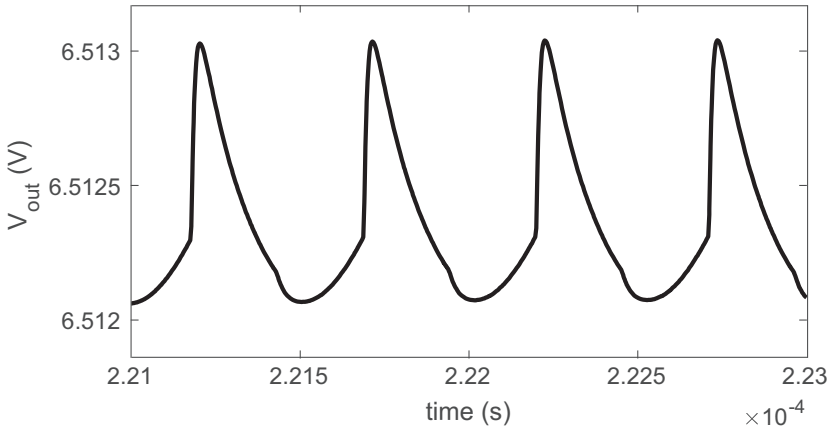

Figure 13. Simulated output ripple for 1 µA load.

Table 2 shows a comparison of the proposed charge pump with other published charge pumps. Specifically, we included other regulated charge pumps in this table that (1) were fabricated, (2) provide $V_{out} > 2V_{dd}$ for the process, (3) do not utilize a large off-chip capacitor to reduce the ripple, and (4) have a reported ripple voltage less than 100 mV. Of the reported charge pumps that meet the above criteria as shown in Table 2, our proposed charge pump is capable of the lowest ripple.

Table 2. Comparison of low-ripple charge pumps.

	This Work	**Rumberg** [5]	**Tseng** [11]	**Tsai** [12]	**Zhu** [22]	**Mahmoud** [23]
CMOS Process	0.35 µm	0.35 µm	0.18 µm	0.18 µm	0.13 µm	65 nm
V_{in} (V)	2.5	2.5	1.2	1	1.5	0.55–0.7
V_{out} (V)	2.5–10	7.5–16	6	3–6	2.7–12	3.3
# Stages	7	6	3	6 + 9 interleaved	3–10	1–4
$C_{p,total}$ (pF)	33	18	18	-	-	160
C_L (pF)	80	80	-	54	20	400
Size (mm^2)	0.163	0.069	4	0.5	0.026	0.17
Max I_L (µA)	80	40	700	240	0.6	34
Max Efficiency (%)	25.7	34	-	58	49	66
Ripple (mV)	<1 *	18	30	39	36	50–70

* Simulated results due to measurement limitations.

Comparing this new charge pump to our previous work [5], approximately half of the increase in size is due to the larger pumping capacitors that were used to increase the current-driving capabilities. The rest of the area was due to the size of the LDO and the resistive divider, which included drawn resistors instead of only diode-connected pFETs as in [5]. This new charge pump is capable of an order-of-magnitude lower ripple voltages. However, the inclusion of the LDO prevents the entire circuit from generating as high voltages as in [5]; the circuit of [5] was specifically designed to be able to achieve high voltages without subjecting any transistor to voltage drops greater than V_{dd} and ensuring that no junction undergoes a breakdown voltage. However, the OTA in the LDO limits the output voltage to 10 V.

Both [11,12] would be capable of providing the voltages necessary for programming FG transistors via hot-electron injection if no significant voltage overhead is required for the programming circuitry, and they both provide larger current-driving capabilities than the proposed charge pump. However, their ripple is larger, and they consume considerably larger real estate. The circuit of [22], on the other hand, is very compact. However, while it is able to produce a voltage that is large-enough for

injection, the maximum load current is quite small and would likely be limiting to FG programming applications. Even though the circuit of [23] was fabricated in a 65 nm process with a significantly reduced supply voltage, FG devices require a gate oxide of ∼7 nm for long-term retention [5], which sets the voltages necessary for inducing hot-electron injection. The maximum voltage of [23] is not sufficient for FG programming.

In summary, of the circuits listed in Table 2, the proposed charge pump is the best suited to meeting the needs of precision programming of analog components via hot-electron injection. If the floating-gate transistors were instead being used for digital memory, many other high-voltage charge pumps would be capable of providing the elevated voltages needed; since the charge on the FG of a digital device does not need to be as precisely controlled, charge pumps with larger ripples would suffice [14,24,25], and even open-loop charge pumps with output voltages that are much more dependent on the load current (see Equation (1)) could be used [26–28]. The high accuracy needs of the analog memory necessitates more-stringent requirements of the charge pump.

5. Conclusions

In this paper, we presented a high-voltage regulated charge pump that is capable of providing the voltages necessary for hot-electron injection programming of floating-gate transistors while maintaining extremely low output ripple. To reduce the ripple voltage, an LDO is incorporated inside the charge-pump loop. This charge pump is able to provide voltages up to 10 V with ripple voltages less than 1 mV while only being 0.163 mm^2 in size. This charge pump is also a good candidate for use in other applications that have sensitive nodes that require elevated voltages.

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