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A New Rail-to-Rail Second Generation Voltage Conveyor

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Abstract: In this paper, a novel low voltage low power CMOS second generation voltage conveyor (VCII) with an improved voltage range at both the X and Z terminals is presented. The proposed VCII is formed by a current buffer based on a class AB regulated common-gate stage and a modified rail-to-rail voltage buffer. Spice simulation results using LFoundry 0.15 µm low-Vth CMOS technology with a ±0.9 V supply voltage are provided to demonstrate the validity of the designed circuit. Thanks to the class AB behavior, from a bias current of 10 µA, the proposed VCII is capable of driving 0.5 mA on the X terminal, with a total power consumption of 120 µW. The allowed voltage swing on the Z terminal is at least equal to ±0.83 V, while on the X terminals it is ±0.72 V. Both DC and AC voltage and current gains are provided, and time domain simulations, where the voltage conveyor is used as a transimpedance amplifier (TIA), are also presented. A final table that summarizes the main features of the circuit, comparing them with the literature, is also given.

Keywords: low voltage; low power; voltage conveyor; VCII; rail to rail

1. Introduction

Since the introduction of current conveyors in 1968 [1], the well-known operational amplifiers (Op-Amps) have started to be replaced in several applications [2–4]. Generally, current conveyors take inherent advantages of current mode signal processing and, in comparison to conventional Op-Amp based circuits, those employing current conveyors exhibit better frequency performance and simpler circuitry [5,6]. A literature survey shows that, in current conveyor families, second generation current conveyors (CCIIs) [7–12] are the most widely used. However, as the CCII lacks a low impedance voltage output port, it is not suitable for applications requiring output signal in the voltage form because, in these cases, an extra voltage buffer is needed to provide low output impedance, which results in higher power consumption and higher chip area.

In [13], the idea of voltage conveyors (VCs) as the dual circuit of the current conveyors (CCs) was introduced. Based on this concept, the dual circuits of CCIIs have been called second generation voltage conveyors (VCIIs). In particular, VCIIs show a low impedance voltage output port. This feature makes VCIIs a highly suitable candidate to replace CCIIs in applications requiring voltage output because they alleviate the need for an extra voltage buffer. Recently, VCIIs have attracted the attention of researchers, and their applications in implementing filters, gyrators, oscillators, inverting and non-inverting voltage amplifiers, current to voltage converters, differentiators and integrators, and readout circuits have been reported [13–20].

The low voltage low power restrictions imposed by advanced technologies necessitate the design of a high performance VCII circuit that is able to operate under low supply voltages and to provide an appropriate voltage swing at the voltage output port. Since previous implementations of VCIIs have

suffered from limited voltage swing at the voltage output port [14–16], in this paper, we propose a new low voltage low power VCII with improved voltage range (rail-to-rail, (RtR)) characteristic at the output of terminal Z, but also at the input of terminal X. This will fully take advantage of its inherent transimpedance amplifier (TIA) behavior, making it suitable in applications where information has to be converted from the current to the voltage domain [21,22]. The proposed VCII has been developed with low-Vth CMOS technology (LFoundry 0.15 µm), with a supply voltage of ±0.9 V, showing a voltage swing at least equal to 80% of the supply voltage range. The manuscript is organized as follows: Section 2 gives a short overview on the highlights of second generation voltage conveyors; Section 3 shows and analyzes the proposed rail-to-rail VCII; Section 4 shows the simulation results of the proposed circuit, together with a table that compares them to some other relevant works available in the literature. Finally, Section 5 draws conclusions.

2. VCII Short Review

Figure 1 shows the internal structure (a) and symbol (b) of the second-generation voltage conveyor (VCII) as a dual circuit of the second-generation current conveyor (CCII). It consists of a current buffer between the Y and X terminals and a voltage buffer between the X and Z terminals. Unlike the CCII, the Y terminal of the VCII is a low impedance current input port with an ideal value of zero, X is a high impedance current output port with an ideal value of infinite, and Z is a low impedance voltage output port with an ideal value of zero. The relationship between port voltages and currents are expressed as:

$$\begin{bmatrix} i_x \\ V_z \end{bmatrix} = \begin{bmatrix} \pm\beta & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} i_y \\ V_x \end{bmatrix} \quad (1)$$

where VCII+ and VCII- are identified by +β and −β, respectively (where β should be close to 1). Ideally, the value of α is unity. Since the Y terminal has an extremely low input impedance, it can be considered as a virtual ground node. The main features of VCII can be summarized in three key points. Firstly, unlike other active blocks, current summing operation can be easily performed at the current input low impedance Y port. Secondly, having a low impedance voltage output Z port allows the flawless employment of the VCII in a voltage mode workflow, giving the flexibility to easily perform current mode operations to the designer. Finally, positive and negative voltage gains are simply obtained by employing VCII+ and VCII-, respectively.

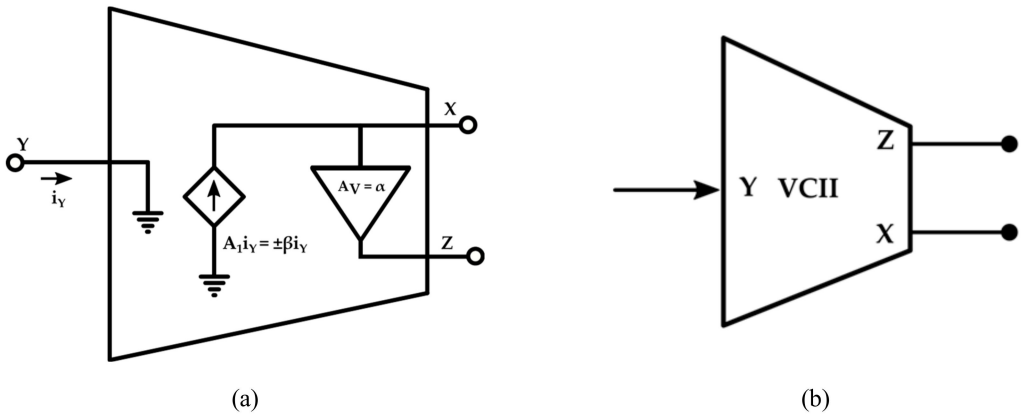

Figure 1. Second generation voltage conveyor (VCII): (**a**) Internal structure; (**b**) Symbol.

3. The Proposed RtR VCII

The proposed RtR-VCII is composed of a class AB current buffer between the Y and X terminals and an RtR modified voltage buffer between the X and Z terminals. Figure 2 shows the designed current buffer. It is formed by transistors M_1–M_7 and the current sources I_{b1}–I_{b3}. Transistor M_3 in the common-gate configuration is biased by a voltage that is regulated by the negative feedback

loop established by M_1–M_2, providing the virtual ground at the Y terminal and further reducing its impedance. The voltage buffer implementation is based on a modified version of the standard class AB voltage follower (see Figure 3a,b) [23]. PMOS M_{L1}–M_{L2} and NMOS M_{H1}–M_{H2} differential pairs drive a switching circuit that, based on the reference voltages V_{HIGH} and V_{LOW}, activate the correct portion of the buffer that is the standard voltage follower M_{n1}, M_{n2}, M_{p1}, M_{p2}, or the RtR pair M_{H7} and M_{L7}. The working principle is explained in depth in [23].

The complete schematic of the proposed VCII is shown in Figure 4. M_8 and I_{b3} fix the voltage at the drain of M_6. Then, it is possible to choose the gate voltage of M_8 (V_{bias}) to accurately tune the bias current of the Y and therefore the X terminals. Capacitors C_1 and C_2 are used to dampen the α parameter transfer function, ensuring the stability of the system. The impedances are derived using the small signal equivalent model depicted in Figure 5. The impedance at the Y terminal is given by:

$$Z_Y \approx \frac{1}{gm_{M3}gm_{M1}(rds_{M1}//ro_{IB1})}. \tag{2}$$

Transistors M_4–M_7 have the task of copying the input current (at Y) to the X terminal. Since the current flowing at Y is mirrored on the class AB-biased branch formed M_5 and M_7, the voltage swing allowed at the X terminal is very wid, even for high currents. Precisely, it is given by:

$$Vss + Vds_{M5} \leq V_X \leq Vdd - Vsd_{M7}. \tag{3}$$

The total input impedance at the X terminal can be approximated as follows:

$$Z_X = Rds_{M5}//Rds_{M7}. \tag{4}$$

Concerning the voltage output Z terminal, the allowed voltage swing can be evaluated as:

$$Vss + Vds, sat_{ML7} \leq V_Z \leq Vdd - Vsd, sat_{MH7}. \tag{5}$$

Since the output stage changes shape according to the voltage level at the X port, the output impedance can be evaluated as [23]:

$$Z_Z \cong \begin{cases} \dfrac{Rds_{Mn3}Rds_{Mp3}}{Rds_{Mn3} + Rds_{Mp3} + \left(R_{k1}gm_{Mp3}Rds_{Mp3} + R_{k2}gm_{Mn3}Rds_{Mn3}\right)} \; if \; V_{LOW} < V_X < V_{HIGH} \\ \dfrac{1}{gm_{Mn3}gm_{mp2}Rds_{Mp2}} \; if \; V_X > V_{HIGH} \\ \dfrac{1}{gm_{Mp3}gm_{mn2}Rds_{Mn2}} \; if \; V_X < V_{LOW} \end{cases} \tag{6}$$

where R_{k1} and R_{k2} are equal to $\left(gm_{Mn2}Rds_{Mn2}Rds_{Mp3}//Rds_{MH5}\right)$ and $\left(gm_{Mp2}Rds_{Mp2}Rds_{Mn3}//Rds_{ML5}\right)$, respectively.

The topology of the designed VCII allows it to be employed as a transimpedance amplifier. In fact, taking advantage of the high drive capability at X, together with the RtR behavior on X and Z, it is possible to achieve high gain conversion, even for large currents. A VCII used as a TIA is shown in Figure 6. The conversion gain can be easily set by a simple resistance value according to the following ideal equation:

$$V_{out} \cong V_X = I_Y R_{gain} \tag{7}$$

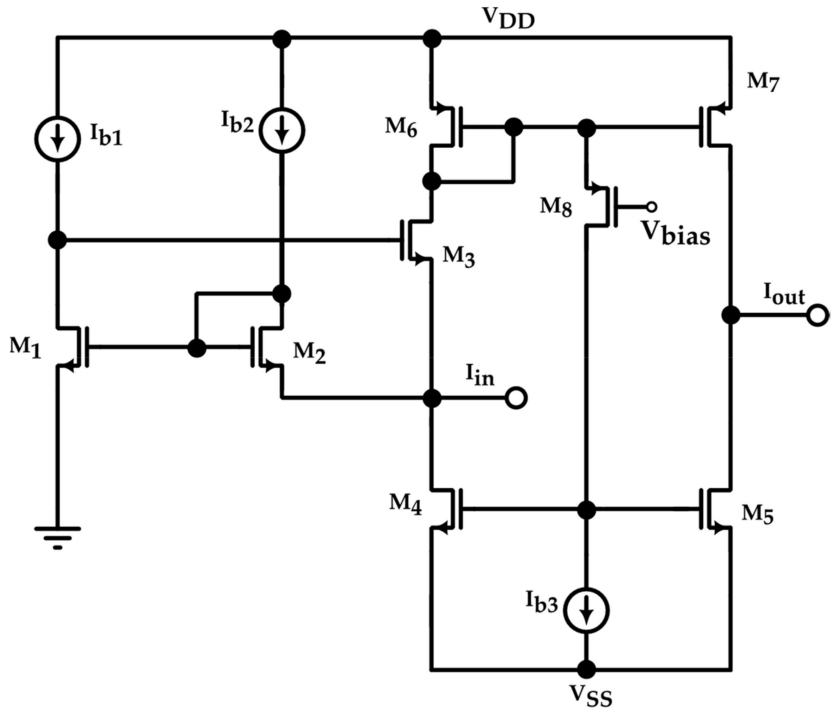

Figure 2. The proposed class AB current buffer stage.

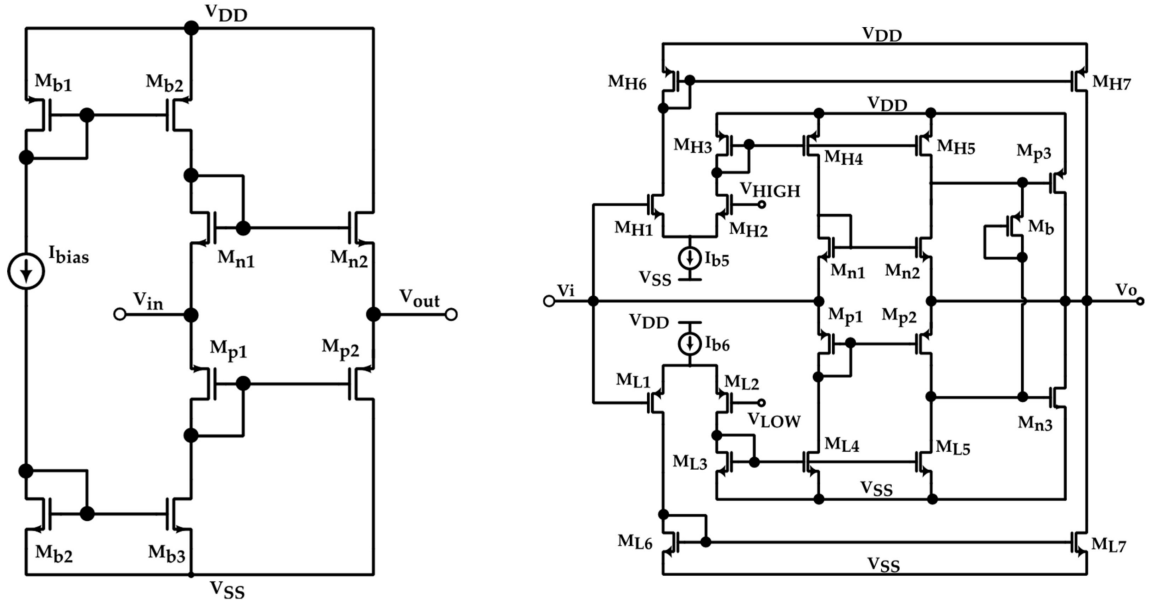

Figure 3. (**a**) Simple voltage follower, (**b**) Modified rail-to-rail (RtR) voltage follower [23].

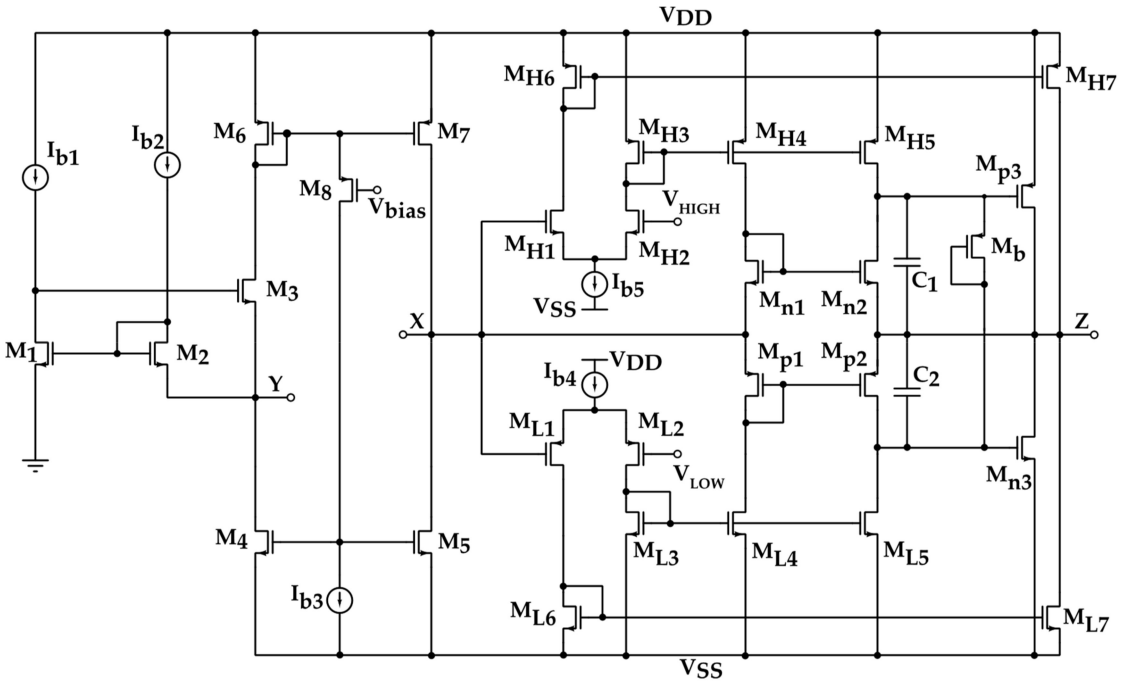

Figure 4. The proposed VCII with Rail to Rail feature.

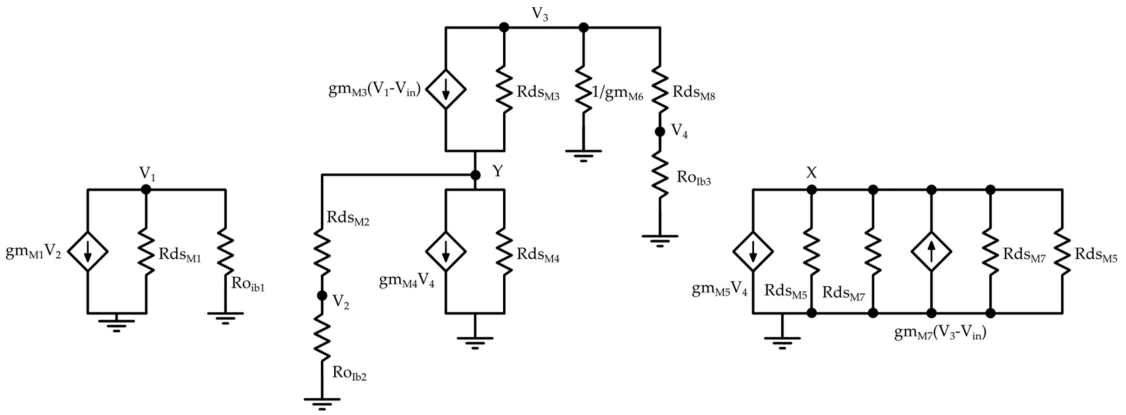

Figure 5. Small signal equivalent model of the X and Y terminals.

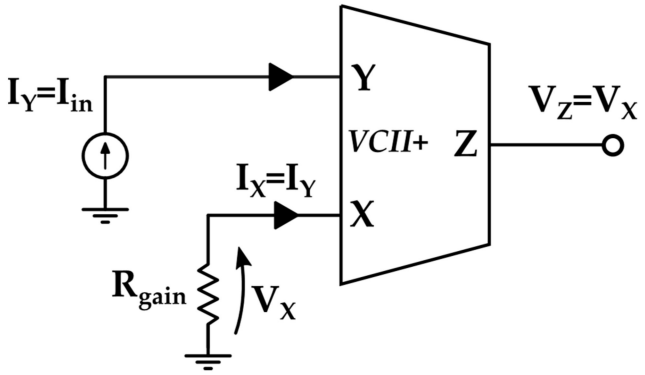

Figure 6. Transimpedance amplifier (TIA) implementation using a VCII+.

4. Simulation Results

Simulations were performed employing 0.15 µm CMOS technology from LFoundry through the Spice simulator. Current sources were implemented by means of simple current mirrors designed to provide a current of 5 µA. Transistor dimensions are shown in Table 1. For the proposed VCII, the two input voltages V_{HIGH} and V_{LOW} at the differential amplifiers of the voltage buffer stage were set to +0.3 V and −0.35 V, respectively, while supply voltages were ±0.9 V. The voltage V_{bias} was set to −0.3 V in order to ensure a 10 µA bias current through the Y and X branches. M_b dimensions were regulated so as to have 10 µA flowing through M_{p3} and M_{n3}. In order to guarantee a high driving capability for the X node, the W/L ratio of M_4–M_5 and M_6–M_7 was set to 100 and 200, respectively.

Table 1. Transistor dimensions and parameter values.

Transistor	Dimensions (W, L)
M_1, M_2, M_8	1.8 µm, 0.3 µm
M_3	2.4 µm, 0.3 µm
M_4, M_5, M_{H7}	30 µm, 0.3 µm
M_6, M_7, M_{L7}	60 µm, 0.3 µm
M_{H1}, M_{H2}	7.2 µm, 0.3 µm
M_{H3}, M_{H4}, M_{H5}, M_{H6}	3.6 µm, 0.3 µm
M_{L1}, M_{L2}	14.4 µm, 0.3 µm
M_{L3}, M_{L4}, M_{L5}, M_{L6}	2.85 µm, 0.9 µm
M_{p1}, M_{p2}	8.75 µm, 0.75 µm
M_{n1}, M_{n2}	2.85 µm, 0.75 µm
M_{p3}	4.5 µm, 0.75 µm
M_{n3}	1.35 µm, 0.75 µm
M_b	0.3 µm, 0.6 µm
Parameter	**Value**
I_{b1}, I_{b2}, I_{b3}, I_{b4}, I_{b5}	5 µA
V_{HIGH}	300 mV
V_{LOW}	−350 mV
V_{bias}	−300 mV
C_1, C_2	250 fF

The rail-to-rail capabilities of this circuit are shown in Figures 7 and 8, where the DC performances of α and β are shown. To evaluate the former parameter, an input voltage at the X terminal, swinging from negative supply voltage to positive supply voltage, was applied, while the output voltage at the Z port was determined at different load levels (50 kΩ, 20 kΩ, 10 kΩ). As can be seen, α always remains greater than 0.95 for input voltages greater than ±0.8 V. Analogously, the performance of the β parameter was investigated by applying a current at the Y port and monitoring the current at the X port for different load levels. Figure 8 acknowledges both the good driving capability of currents of 0.5 mA (50 times greater than the X branch bias current) and the good voltage swing at X, which reaches ±0.72 V with a current of ±0.5 mA over a load of 2 kΩ.

Frequency performances of the voltage conveyor are presented in Figures 9 and 10. The bandwidth for the α parameter, evaluated with a 1 pF load connected at the output Z node, was equal to 55 MHz (Figure 9). The β transfer function is shown in Figure 10. The bandwidth was equal to 165 MHz.

Terminal impedance values were also evaluated. The resulting values (see Figure 11) are 522 kΩ, 23 Ω, and 160 Ω at X, Y, and Z, respectively. To investigate the time domain behavior of the VCII, a 1 MHz sine wave with a 0.8 V peak amplitude was applied to the X terminal. The total harmonic distortion (THD) at the output (Z terminal) with a 1 pF, 10 kΩ parallel load, considering 10 harmonics, was equal to 2.4% (−32.4 dB). The same analysis was repeated, applying a 1 MHz sine wave with a 0.5 mA peak amplitude at the Y port. The X terminal was connected to a 100 Ω load. The THD was equal to 1.1% (−39 dB).

To show the benefit of the dual input-output rail-to-rail stages, the circuit was tested in a transimpedance amplifier configuration. A sinusoidal current on the input terminal Y, with an amplitude of 0.5 mV, was imposed and the output voltage at the X node was determined. The output was connected to a 1 pF capacitor in parallel to a 10 kΩ resistor. The gain resistor was set equal to 500 Ω and 1.5 kΩ to take advantage of the full X branch dynamic. Results are shown in Figure 12, acknowledging the capability of the circuit to reach a dynamic of 80% of the supply voltage without distortions.

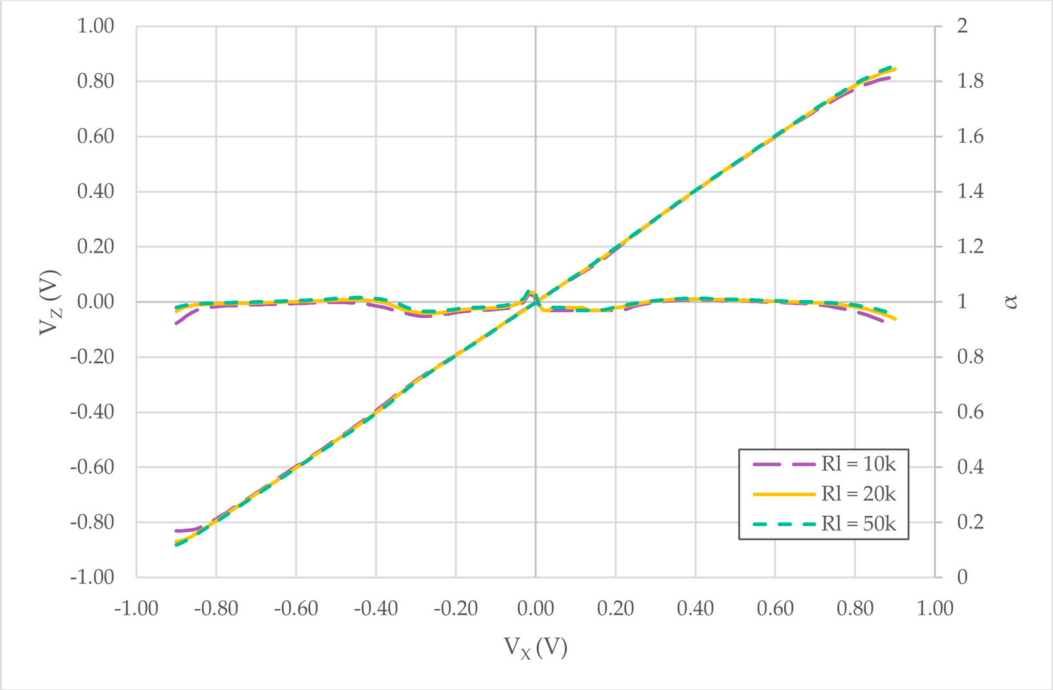

Figure 7. DC performances of the α parameter at different load levels connected to the Z node.

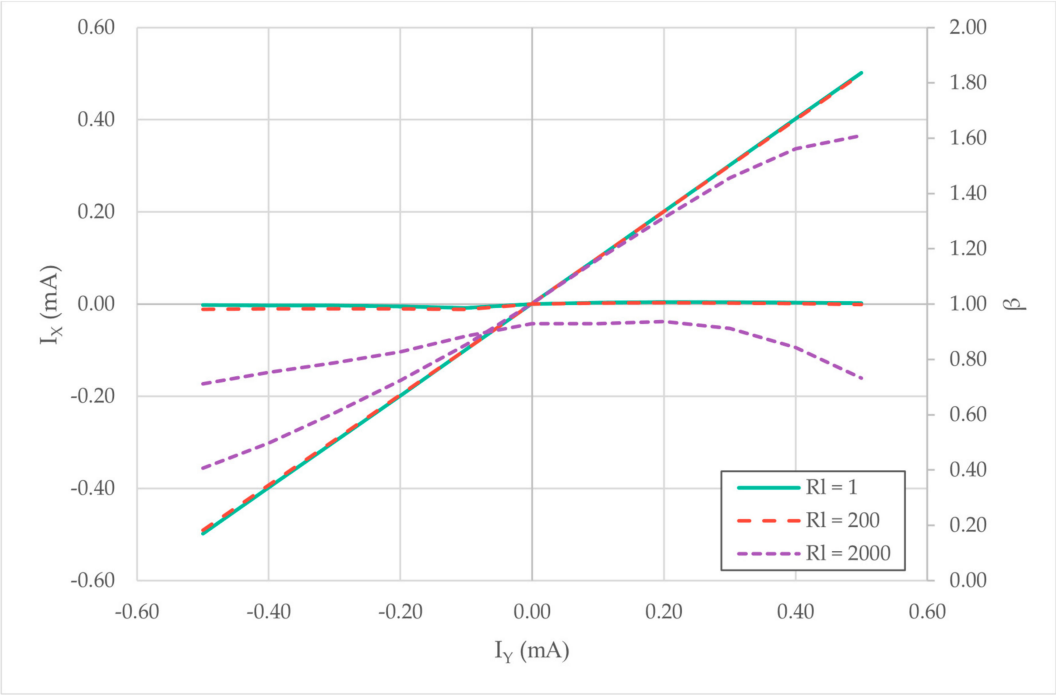

Figure 8. DC performances of the β parameter at different load levels connected to the X node.

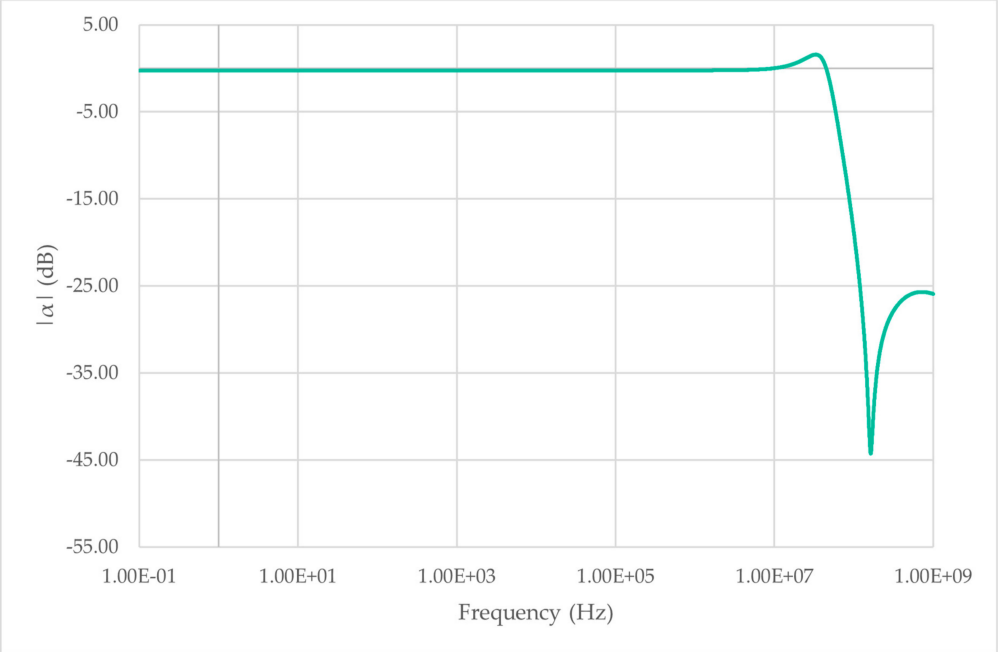

Figure 9. AC performances of the α parameter with a 1 pF capacitor connected to the Z node.

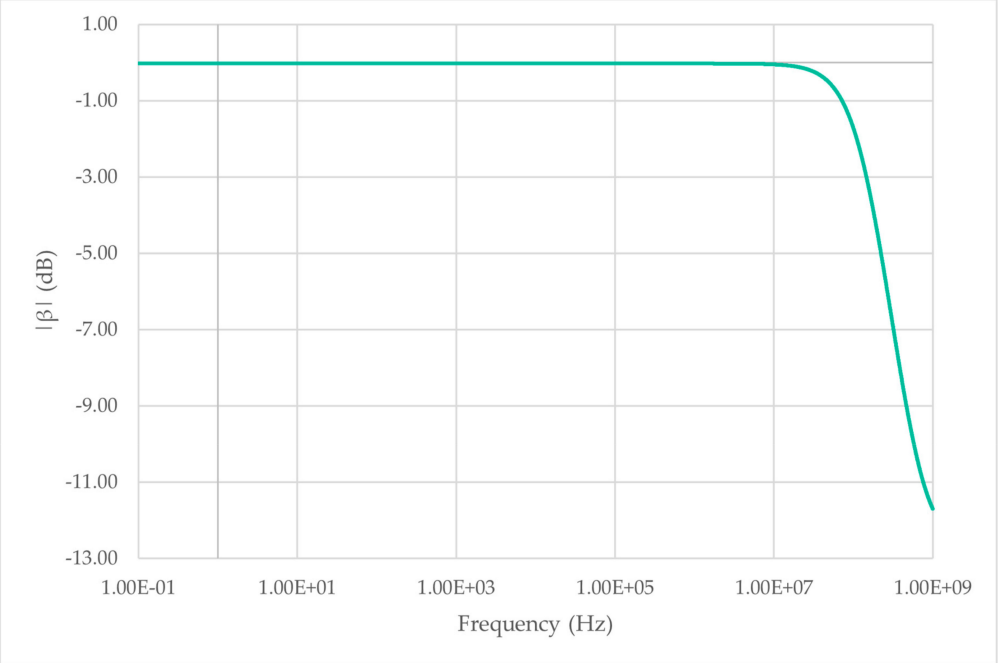

Figure 10. AC performances of the β parameter.

Table 2 summarizes the circuit performance parameters, comparing them with other relevant manuscripts from the literature. The presented topology manages to achieve overall comparable performances with respect to the other circuits, while greatly improving the dynamic range of the voltage conveyor, as well as reducing its power consumption, as acknowledged by the figure of merit (FOM) (in this case, lower is better) parameter in the same table. In this regard, the parameter is calculated as [24]:

$$FOM = \frac{V_{DD} + |V_{SS}|}{V_{in,pp\_max}} I[\mu A] \quad (8)$$

where V_{in,pp_max} represents the maximum input peak-to-peak voltage that still allows it to achieve acceptable linearity levels and is extracted from the THD evaluations. The parameter, I, expressed in μA, introduces the FOM of the power consumption of the circuit, decoupling it from the actual supply voltage.

As can be seen from Table 2, the proposed topology links the current driving capabilities (at the Y terminal) of [16] to the extended input dynamic range (at the X and Z terminals). Moreover, unlike [17], where the authors make use of a universal voltage conveyor, the presented architecture uniquely implements a second generation voltage conveyor, thereby largely reducing the overall power consumption.

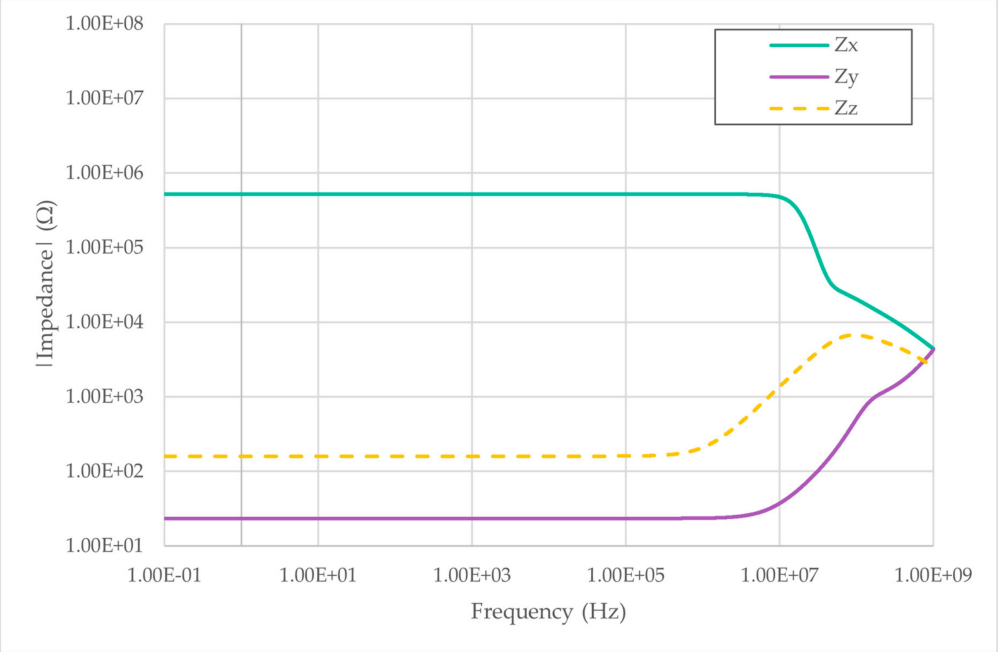

Figure 11. Proposed VCII terminal impedances.

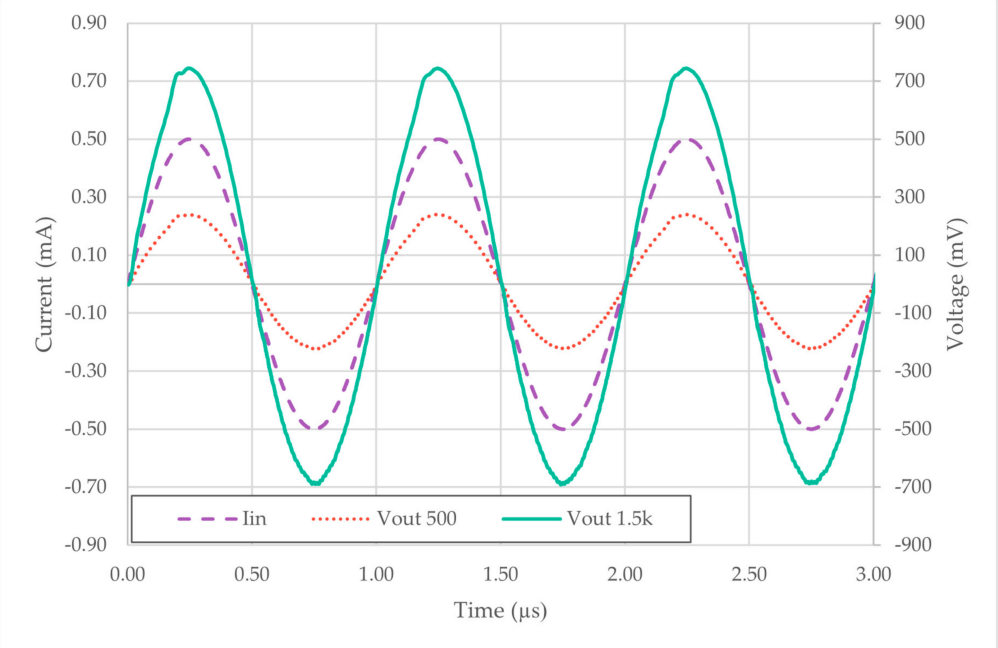

Figure 12. VCII used as a TIA.

Table 2. The Proposed VCII Performance Parameters.

Parameter	This Work	[14]	[16]	[17,25]	[15,18]
Technology	LFoundry 0.15 µm	AMS 0.35 µm	AMS 0.35 µm	TSMC 0.35 µm	AMS 0.35 µm
Supply voltage	±0.9 V	±1.65 V	±1.65 V	±1.65 V	±1.65 V
Impedance at X node	522 kΩ (@100 MHz)	1.2 MΩ	370 kΩ	240 kΩ	802 kΩ
Impedance at Y node	23 Ω (@100 MHz)	6.7 Ω	2 mΩ	650 mΩ	49 mΩ
Impedance at Z node	160 Ω (@100 MHz)	0.7 Ω	2 mΩ	1.4 Ω	79 mΩ
α	−0.24 dB (@100 kHz)	−0.03 dB	−0.07 dB	0.32 dB	−0.04 dB
β	−0.03 dB (@100 kHz)	−0.1 dB	−0.115 dB		−0.04 dB
α bandwidth	55 MHz (1 pF load at Z)	217 MHz (unloaded)	220 MHz (unloaded)	74 MHz	340 MHz (unloaded)
β bandwidth	165 MHz	200 MHz	22.4 MHz	64 MHz	14 MHz
V_Z THD	2.4% (−32.4 dB) (V_X = 1.6 V_{pp}; @1 MHz; 10 harm)	0.068% (−63 dB) (V_X = 1 V_{pp}; @1 MHz; 10 harm)	2.48% (V_X = 1 V_{pp}; @1 MHz; 10 harm)	2.7% (V_X = 1 V_{pp})	N.A.
I_X THD	1.1% (−39 dB) (I_Y = 1 mA_{pp}; @1 MHz; 10 harm)	0.1% (−59 dB) (I_Y = 20 μA_{pp}; @1 MHz; 10 harm)	3.36% (I_Y = 1 mA_{pp}; @1 MHz; 10 harm)	N.A.	N.A.
Static Power Cons.	120 µW	330 µW	320 µW	≅5 mW	700 µW
figure of merit (FOM)	85	330	320	4950	874

5. Conclusions

We have here presented a new CMOS VCII, showing RtR voltage swing at the X and Z ports. The dynamic biasing of the Y and X branches ensures a high driving capability at the X terminal with a low quiescent current. These two features, together, allow it to achieve high transimpedance conversion gains even for relatively large currents. Simulation results have been given, effectively acknowledging the predicted behavior. A possible application scenario has been proposed for a transimpedance amplifier configuration.

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